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RECOGNISING ACHIEVEMENT

GCE

# Electronics

Advanced GCE **A2 7826**

Advanced Subsidiary GCE **AS 3826**

# Report on the Units

# June 2007

**3826/7826/MS/R/07**

Oxford Cambridge and RSA Examinations

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## PE's report to centres on 2526 (June 2007)

### General Comments

This year's paper performed similarly to previous ones, with some candidates able to earn all of the marks, and very few unable to earn many at all. Candidates were given a variety of opportunities to demonstrate their understanding. As always, they found this easier to do for the digital aspects of the course. The written explanations required for some parts of the questions about analogue electronics proved beyond the abilities of many weak candidates. However, 'show that' calculations were explained better than in previous years, with more candidates writing down the formula, substituting values with correct powers of ten and giving the answer to at least one more decimal place than given in the question stem. Drawing of circuit diagrams and sketching of graphs lost marks too often because candidates did not take enough care over them.

### Comments on Individual Questions

1. This year's paper started with a question about combining logic gates. The majority of candidates earned most of the marks available, suggesting that this aspect of the course is delivered well by all centres. If candidates did lose marks, it was for failing to notice that the last row of the truth table in (b)(i) was incomplete, drawing poor symbols for their NOR gates (NOT gates were popular) or omitting to include enough columns in their truth table.

2. This question sought to probe candidates' understanding of power supplies. As in previous years, it resulted in a wide spread of marks. For (a) candidates were required to describe the function of three parts of a power supply. Few were able to gain full marks for this, suggesting that they needed more practice in the correct use of the words voltage and current, as well as a deeper understanding of how a power supply works at component level. However, the circuit diagram of (b) and the calculations of (c) (i) and (ii) often earned full marks. The graph of (c) (iii) discriminated well, with many candidates unable to draw a ripple of only 0.5 V. Many candidates did not know how to calculate the capacitor value required in (c) (iv).

3. This question was about zener diodes. Most candidates knew that the current direction in the diode was from +12 V to 0 V. Their descriptions of the current-voltage characteristic required in (a) (ii) were, in general, poor. Apart from incorrect use of terminology (such as 'voltage flowing'), candidates gave very muddled answers. Few took a logical approach, stating what happens to the current as it is gradually increased from zero to above the breakdown voltage. Perhaps centres should consider testing candidates' ability to describe the transfer characteristics of systems and components in words as well as algebra and graphs. Although most candidates were able to calculate the maximum safe current in the diode for (b), many did not know that the diode would be damaged by overheating if that current was exceeded - they just thought that it would break down. Part (c) was well done by many candidates, with only a minority unable to obtain a correct value for the resistor. The graph of (d) proved, as expected, too difficult for many candidates, with only a minority realising that the output voltage tracked the input voltage until the zener diode reached its breakdown point, and thereafter remained at a constant value.

4. This question was about a NAND gate bistable. Very few candidates were unable to identify the LED in (a) (i) or correctly complete the truth table in (c) (i). The timing diagram of (d) was often poorly drawn, with many candidates clearly unaware of the latching property of a bistable. Error-carried-forward had to be invoked often in the calculation of (a) (iii) because many candidates simply did not know a typical value for the voltage drop across a forward biased LED - 0.7 V was a popular wrong answer. As expected, many candidates used their answer of (a) (ii) directly in the calculation, rather than working out the voltage drop across the series resistor and using that instead. For (c) (ii), too many

candidates omitted to use the labels provided in the circuit diagram and consequently lost marks because it was not clear which gate they were referring to. Unexpectedly, (b) was possibly the worst-answered question of the whole paper. Candidates not only needed a firm grasp of the meaning of the terms 'voltage' and 'current', they also had to know that the current at the input of a logic gate is negligible, leading to no voltage drop across the pullup resistor when the switch is open.

5. This question required candidates to analyse a fairly complicated circuit involving a number of separate sub-systems. The voltage divider calculation of (a) proved to be straightforward for most candidates, as was the identification of the thermistor in (b) (i). However, providing a coherent written explanation for the variation in output voltage of a voltage divider containing a thermistor proved to be difficult for most candidates. Most knew that the resistance decreased with increasing temperature, but then failed to mention that this resulted in an increase of current, requiring an increase in voltage across the fixed resistor. It is not enough for candidates to be able to calculate voltages for a voltage divider; they need to understand its behaviour at component level as well. Similarly, few candidates earned full marks for (b) (iii), where they were required to explain why a change in the output for a change at the input. They either omitted to explain the consequent behaviour of one or more of the five stages (voltage dividers, op-amp, relay and motor) or (for weaker candidates) did not provide enough detail. For example, 'the op-amp output goes high' earned no marks, whereas 'the op-amp output saturates at +13 V' earned a mark. Only a minority of candidates realised that the relay of part (c) was required to boost the current output of the op-amp; many assumed it was there for safety, providing electrical isolation or because the op-amp couldn't supply enough voltage. (Although the latter answer is plausible, the difference between 13 V and 15 V is not going to make much difference to a motor, whereas an op-amp's ability to only supply a few milliamps is.) The final part of the question completely floored many weak candidates. Having decided erroneously that the diode in series with the relay coil protected the op-amp from voltage surges, they were at a complete loss to provide any reason for the second diode in parallel with the coil.

6. The vast majority of candidates fared much better with the truth table of (a), with many earning full marks. Their explanation of what happens in (b) when all four switches are left open tended to be too brief, often omitting to mention that the inputs to the logic system were low under these conditions. Many weak candidates assumed that because D was also low, this meant that Q must also be low. Finally, in (c) too many candidates failed to arrange three of the switches so that D was high **before** pressing the last switch to provide a clock pulse for the flip-flop.

7. This question was intended to provide an easy path towards the end of the paper for tired candidates. In practice, it proved to be difficult for candidates to correctly identify the circuit of (a) as a non-inverting amplifier. Those who did so correctly were then often confused by the choice of resistor values to insert into the gain formula. Too many used the values for the input impedance resistor instead of the pull-down resistor in the feedback loop in (b), losing a mark. Error-carried-forward was applied to their sketch of the transfer characteristic of (c), preventing candidates who had already lost many marks from necessarily losing any more. Nevertheless, careless drawing of the graph lost many candidates a mark or two.

8. Few candidates had any difficulty correctly calculating the time constant of the circuit of (a), with only a minority unable to get the powers of ten correct. Similarly, many candidates earned the majority of marks in the sequencing exercise of (b), showing that they could certainly analyse the behaviour of the system given this level of scaffolding, whereas their earlier attempts at analysing other systems in the paper suggested that they would have been far less successful without it.

## SIGNAL PROCESSING CIRCUITS (2527)

### June 2007

The majority of the nine hundred and fifty or so candidates were able to demonstrate that they had mastered at least some aspects of their chosen subject. Indeed, question 4, on a logic system with three inputs, was nearly always very well answered.

However, the examiners all felt that many marks were lost due to book learning not having been reinforced by appropriate practical work. For example, many candidates could draw the characteristic graph of a Schmitt trigger in question 5 but could not draw a circuit diagram of it in question 7. Even more surprising was question 3 on filters where most candidates made a decent attempt at design in part (b) but were lost in part (c) for an explanation of how to plot filter characteristics. It was fairly evident that a large number of candidates had never performed any experiments to extract the necessary data to answer the question (a surprising observation in view of the importance of the topic).

One further question which should be highlighted is 1(b), which asked for the purpose of the resistor in series with the LED. Quite a number of candidates answered with a bald statement that "this resistor is to protect the LED" (from what?). For this they were awarded no marks. Many candidates answered that this resistor was to limit the voltage and for this the examiners also decided to award no marks. This is because <u>any</u> resistor in series with an LED (as far as an "ideal", exam board, LED is concerned) will limit the voltage to (say) 2V but not all resistors would be suitable. For example, from a 5V power supply, a 1Ω resistor will "limit the voltage" and ruin the LED (with a 3A current). From the same 5V power supply, a 1MΩ resistor will "limit the voltage" and render the LED useless (with a 3μA current). The answer sought was that the purpose of the series resistor is to limit the <u>current</u> in the LED.

### Question 1

(a) Most candidates were able to state (for at least one marking point) the purpose of the resistors labelled $R_2$. The examiners accepted any sensible answer such as pull down resistors, avoiding inputs floating, holding inputs at 0V or avoiding short circuits across the power supply.

(b) Many candidates were penalised for too woolly an answer as explained above in the introduction.

(c) Most candidates scored all three marks for Boolean expressions for X, Y and Z.

(d) Most candidates were able to provide the Boolean expression for M.

(e) Most candidates scored all three marks for the truth table.

(f) Quite a large proportion of candidates were penalised one of the two available marks for a slack answer of "the LED comes on if 2 switches are pushed" without any further indication that it will not come on if the third switch is pushed at the same time.

**Question 2**

(a) The majority of candidates found this question to be too difficult and were unable even to answer this opening "easy" part of naming the circuit as an integrator or ramp generator.

(b) Only the higher grade candidates were able to calculate the ±7.6 $Vs^{-1}$ ramping rate from the ±5V input.

(c) While some candidates realised the integrator should produce a linear ramp, most were unable to draw the correct answer where the output oscillates between -13V and +2V.

(d) Very few candidates correctly stated that with a +5V / 0V pulse input, the output would saturate at -13V on the first pulse and thereafter stay there.

**Question 3**

(a) A surprisingly large number of candidates did not realise that the frequency response was that of a bass boost filter.

(b) Almost all candidates were awarded at least some marks for their circuit and calculations of the filter circuit. Even the quotation of a formula resulted in an award. Errors in the position of the capacitor were marked sympathetically and with consequent error carried forward in its calculation.

(c) The examiners were very surprised at how few scripts were awarded full marks for this question (despite the marking scheme only looking for basic minimum points). A signal generator as an input and an oscilloscope to measure the amplitude of the input and (unsaturated) output voltages are required. Voltmeters would have been acceptable instead of an oscilloscope but only if they were identified as a.c. voltmeters. Many stated that they would "compare" the output and input (whatever that meant) instead of clearly stating that the voltage gain would be measured by dividing one voltage by the other. Only about half the candidates even bothered to write that they would take their measurements over a wide range of frequencies.

**Question 4**

(a) Almost all candidates scored at least one of the two available marks for their explanation of a logic signal.

(b) Almost all candidates correctly filled in the truth table for the logic system described and then made a reasonable stab at producing a Boolean statement and circuit diagram for it.

**Question 5**

(a) Most candidates correctly identified the resistor arrangement as a potential divider.

(b) While most candidates were able to show the current in the series resistors to be 12.5mA and the voltage across the LDR to be 5V there was an occasional fudge where the V = IR calculation in part (ii) was simply transferred back to part (i) as exactly the same formula rearranged as I = V / R. This was not acceptable.

(c) The majority of candidates knew the basic hysteresis shape of a Schmitt trigger characteristic but only a minority correctly realised why such a circuit would be better than a simple comparator for counting the days in the year. The comparator, of course, would produce multiple pulses from varying light levels during any particular day.

**Question 6**

(a) A large proportion of candidates failed to score both available marks for their explanation of the toggling flip-flop. Many failed to highlight the action on the rising edge of the clock pulse.

(b) The clock pulse timing diagram was generally well answered apart from failures to realise that A changes state on the rising edges of the clock while B and C change state on the falling edges of A and B respectively.

(c) Most candidates were able to state and explain why the maximum number of output states of a 3-bit counter is 8.

(d) Most candidates were able to explain why 9 D-types would be required to count to 365 although there were many errors presented in the conversion to the binary equivalent.

(e) A majority of candidates knew how to link the output of an AND gate to the reset pin but many of them made silly / careless mistakes (even with error carried forward) in their linking the binary counter outputs to the AND inputs.

**Question 7**

(a) While some candidates made a reasonable effort to draw a non-inverting Schmitt trigger circuit the majority of them failed to spot the absence of a zero volt line in the diagram. They were expected to include in their diagram either a 0V line or its creation with two equal resistors across the ±15V lines.

(b) This was a very poorly answered question and very few candidates were awarded full marks for their efforts. There are, of course, several ways to generate the +5V / 0V from the ±13V op-amp output but most methods were found to be in error somewhere.

**Report on the Module 2528 June 2007**

Once again this year, the range and quality of projects undertaken at this level was huge. Although the coursework element of this specification amounts to a process, a few candidates attempted projects which were a little too simple and unchallenging. The bare minimum project should have at least 3 active subsystems.

Although attention to the specification has improved recently, some candidates are still giving it scant consideration. It is without doubt one of the most important aspects of the project and must be given due respect in the design process and written up clearly within the report. A good report will contain referenced evidence of relevant research and a very clear and concise specification. A good 'test' for the specification is to ask the question, 'could a competent electronics designer make the project?' It must also be borne in mind that to gain high marks for the specification, some reference to equipment available must be noted in the specification.

Understanding of the project is marked in criterion C and moderators look for understanding at a basic level (qualitative) and at a higher level (quantitative). High marks are achieved for this section when good understanding is shown at component level and that the reason for using a particular subsystem, and how it fits in with the project as a whole, is reported. A few reports simply consisted of long prose on how the project and subsystems should behave, but did not consider the testing and analysis of the final circuit and subsystems.

The attention to testing and analysis has also improved but some candidates are not considering this in sufficient detail. Moreover, moderators are looking for real evidence of testing within the report and if not found, a high mark awarded for criterion D will be reduced. Testing must be real and simulations of a subsystem, whilst useful, do not count as evidence of real testing. Evidence may be provided in the form of actual oscilloscope traces (photographs showing both time and voltage settings), Picoscope traces, photographs of LED indicators, etc. It is the responsibility of the candidate to decide how the actual testing is to be shown.

Criterion E goes hand in hand with criterion D and looks at the analysis of the test results. It is impossible to award high marks for this section if there is no evidence of real testing in the report. Likewise, a shallow analysis will not score highly either. The analysis section is usually the least well done of all sections. The testing of all subsystems and the final circuit must be fully analysed and related back to the specification in order score high marks.

It cannot be over-stressed the importance of providing evidence of testing. Many candidates submitted reports in which it was not clear whether the project actually worked, and the mark for criterion F was sometimes reduced. The report must contain evidence that the project worked or not so that the degree to which the specification has been achieved can be assessed.

It is the responsibility of all centres to ensure that A4 size colour photographs are presented in the report to assess the circuit build. Black and white photographs, or very small photographs are not suitable. Some centres were a little generous in the mark given for the circuit build. A high scoring build will have neat subsystems, colour coding between subsystems and also for the supply of power, and wiring which has been cut to length with no wires crossing (if at all possible) and no wires going over components/chips.

Criterion H is found difficult to mark by some centres. To score highly in this section, candidates must show that signal degradation does not significantly result when one subsystem is connected to another subsystem, or, for example, an output device (display, LED, etc).

Finally, the report must contain a circuit diagram of the project which should be A4 in size. It has been noticed by moderators that certain schematic diagram packages produce very small circuit

diagrams. Whilst these may be neat and the circuit correct, their very small size often negates a mark of 3/3 being awarded for section M.

## PE's report to centres on 2529 (June 2007)

### General Comments

The paper provided a better spread of marks than last year, making it easier to distinguish between the performance of candidates performing at A and E. In general, candidates were able to provide responses to all of the questions (not always earning the marks), and there was no evidence that any of them ran out of time.

As in previous years, each question introduces candidates to a system and invites them to demonstrate their understanding of its function and behaviour. Some of these questions are very easy, but they need to be balanced by others that are much harder. In order for the latter to not discourage weaker candidates, they are often disguised as Trojan Horses, with a hard centre surrounded by a soft exterior. So one or two marks out of several will require a high level of response, with the rest allowed for low level responses. For example, a calculation of current in a resistor may require a voltage drop to be calculated first. Weak candidates often rush in with the first voltage value to hand, losing one mark without being aware of it. Similarly, in written explanations, some of the marks are reserved for the mention of fine details which weak candidates often omit. The only problem with this approach to differentiation is that some good candidates stop writing when they have come to the end of the space provided, rather than when they have run out of things to say. There is plenty of blank space provided on most pages; candidates should make use of it when necessary.

Too many candidates needlessly lose marks for Quality of Written Communication by omitting to have capital letters at the start of sentences and full stops at the end.

### Comments on Individual Questions

1. This question assessed candidates' understanding of a MOSFET configured as an ac amplifier. Almost all candidates were able to identify the input and output for (a) and correctly calculate the voltage at the gate for (b) (i). A variety of answers were acceptable, ranging from use of the voltage divider formula to consideration of the ratio of the resistors. Candidates who used the latter method often failed to start their exposition with a statement of the rule they were using (the ratio of the resistances is the ratio of the voltage drops for a voltage divider), losing a mark. Only a minority of candidates earned both marks for (b) (i). Although most correctly placed the drain halfway between the supply rails, most omitted to give enough detail in their justification. The second marks required them to mention the need to avoid clipping distortion in large output amplitude signals. The calculation of (c) (i) was performed better than in previous years, with fewer candidates unable to make any progress at all with it, although too many got lost towards the end and forgot that the voltage drop across the drain resistor is not the same as the voltage at the drain. Only a minority of candidates were able to earn both marks for (c) (ii), requiring them to make correct use of the terms current and voltage applied to the gate and the drain. The final gain calculation of (c) (iii) was, as expected, beyond the majority of candidates. Although the question expected candidates to recalculate the drain voltage for a different gate voltage and then calculate the voltage gain from the changes in input and output voltages, answers using the formula $G = -g_m R_D$ (which is not on the specification) could earn full marks provided candidates made it clear how they had calculated the transconductance from the graph.

2. This question was about a flash analogue-to-digital converter, testing candidates' understanding of both analogue and digital electronics. It was mostly synoptic, testing candidates' ability to use AS electronics in an A2 context. For (a) (i), candidates were expected to state more than the obvious to earn both marks. Many omitted to mention that the diodes were in forward bias (or conducting), so that their voltage drop was 0.7 V, and some failed to write down that $0.7 \times 3 = 2.1$ V. Part (a) (ii) was a 'show that' calculation. To

earn full marks in this type of question, candidates have to provide a formula, substitute values with correct powers of ten and give an answer to at least one more decimal place than the one provided in the question. The presence of more than one component confused many weak candidates, who often multiplied the correct answer by three. The calculation of (a) (iii) was a Trojan Horse: many candidates forgot to calculate the voltage drop across the resistor before calculating its current, losing just one mark through the use of error-carried-forward. Few candidates understood the use of clamp diodes well enough to earn all of the marks in (b), but the vast majority were able to complete the truth table correctly. It was pleasing to find that most candidates were able to use Boolean Algebra correctly in (c) (ii) and could draw correct circuits to fit their expressions in (c) (iii). They were not required to simplify their expressions and any circuit which had the correct truth table could earn full marks.

3. This question was the first one of the paper to probe candidate's understanding of the principles behind modern electronic communication systems. They were required to do a lot of writing, and weak candidates often omitted to provide enough detail in their answers. Thus for (a) (i), candidates were asked to give two advantages of sending information in digital format and justify them. Too often, candidates ignored the latter, losing marks accordingly. For (a) (ii), too many candidates were unable to think of two advantages of using analogue signals, and many suggested erroneously that they would be quicker to transmit as they needed less processing. Part (b) (i) required candidates to explain their calculation, so if they simply showed calculations with no supporting sentences they could only earn one mark out of the three. As expected, the bandwidth calculation of (b) (ii) proved to be difficult for the majority of candidates who forgot that the bandwidth is half of the maximum bit rate. It was pleasing to find that many candidates could earn full marks for (b) (iii), although they had to qualify each of their suggestions to earn a mark. For example, 'make the picture smaller' only earned a mark if it was accompanied by 'reducing the number of bits to be sent'.

4. This question tested candidates' understanding of frequency modulation. For (a), many candidates were vague about what aspect of the signal fixed the frequency of the carrier. Too many candidates thought it was the amplitude of the signal, rather than its instantaneous voltage. Similarly, for (b) many candidates said that the Schmitt trigger 'cleaned up' the signal, instead of providing a higher level response such as 'converts analogue sine wave into a digital square wave'. It was good to find that the majority of candidates could correctly draw a circuit for a monostable, although only a small minority realised that the output needed inverting to match the behaviour of the monostable described in the question. Some candidates lost marks because they didn't use the $T = 0.7RC$ rule to calculate the component values. Part (d) was synoptic, requiring candidates to design a treble cut filter. Many candidates earned full marks, with weak candidates either putting the capacitor in the wrong place, using resistor values outside the range 1 kΩ to 1 MΩ, or forgetting to have the feedback resistor ten times the value of the input resistor.

5. This question was about amplitude modulation. Unlike previous years, the majority of candidates used spikes instead of bell curves to complete the frequency spectrum of the amplitude modulated signal in (a) (i), mostly in the correct places. Only a minority of candidates were unable to correctly calculate a bandwidth of 300 kHz for part (a) (ii). Part (b) was less well answered, either because candidates didn't know the correct arrangement of components (having the capacitor in series with the diode and resistor was the most popular incorrect answer) or because they didn't chose an appropriate break frequency for the filter. Candidates should know that this needs to be above the maximum expected signal frequency, but well below the carrier frequency. Too many chose either of the values stated in the question (150 kHz or 4.5 MHz) directly. The latter value lost them a mark.

6. This short question on registers discriminated well between candidates. For part (a), too many candidates lost marks through careless omission of labels on their circuit diagram. As always, some drew a counter arrangement instead of a register one. Candidates' responses to part (b) suggested a significant weakness in their understanding of the principles behind serial transmission of binary words. Although all of them knew that the different voltage levels at the start and end of a word were the stop and start bits (no marks), few of them mentioned that these were required by the receiver (not just the system) to indicate the start of a fresh word. Too many candidates seem to think that the stop bit tells the receiver when a word has ended.

7. This question was about the use of an NPN transistor as a driver. Many candidates earned lots of marks for this series to calculations, although many lost one or more marks in each part due to careless omission of intermediate steps. Thus in (b), weak candidates often used 9 V instead of 9 - 1.2 = 7.8 V as the voltage drop across the resistor. Similarly, in (c) (ii), they would often forget to take account of the base-emitter voltage drop of 0.7 V in calculating the value of the base resistor.

8. This final question returned to amplitude modulation. For part (a), many candidates were able to correctly draw the circuit for an oscillator and calculate appropriate values. Although the question required the use of an oscillator which ran continuously, candidates often drew one with enable inputs - these were ignored in the mark scheme. As always, candidates who could correctly quote the formula for the resonant frequency of a tuned circuit ($f_0 = \frac{1}{2\pi\sqrt{LC}}$) were not able to calculate a value for $C$ given values for $L$ and $f_0$. Perhaps centres should consider encouraging candidates to learn an additional alternative formula ($\frac{1}{2\pi f_0 C} = 2\pi f_0 L$) which is easier for them to manipulate? The final part of the question proved straightforward for the majority of candidates. In part (c) (ii), any attempt at showing a high frequency carrier earned the mark, although most candidates drew this as shading, indicating that they had seen this type of signal in their practical work on radio receivers.

## 2530 CONTROL CIRCUITS

### June 2007

This session there were a few candidates who were clearly out of their depth and more than a few who did not appear sufficiently prepared for its demands. However, the majority of candidates did make a decent attempt at every question and a select few scored almost full marks.

### Question 1

(f) The majority of candidates were awarded some of the available six marks for explaining what Subroutines and Interrupts are and why they are useful but there were very many woolly answers and the examiners repeatedly had to agonise over whether or not to award a mark through BOD (benefit of doubt).

(b) The description of microprocessor behaviour when it detects an interrupt was generally well-done and although many candidates failed to state that on detecting an Interrupt the µP will finish its current fetch-execute cycle, they did correctly point out that important registers (especially the program counter) are stored on the Stack. A significant number failed to state that the Stack is an area of memory and this omission cost them a mark.

### Question 2

(c) While almost all candidates knew that the component was a Triac and that terminal A was the Gate only about half knew that B and C were called Main Terminal 2 and Main Terminal 1 respectively. The examiners, however, were very forgiving in marking this identification and awarded the available mark even if the 1 and 2 were the wrong way round or even if the candidate wrote MT2 and MT1 or just Terminal 1 and Terminal 2. The description of Triac behaviour was generally well-known although many candidates were seriously confused over current and voltage; for example, many wrote to the effect that when no current is applied to the gate there will be no voltage in the triac (not true, there could be over 300V across the triac). What they should have said is that until it is fired, there will be no <u>current</u> in the triac (between B and C).

(b) Only a minority of candidates scored full marks for their explanation of a pulse transformer. They were expected to make a brief comment on transformer action and how it allows a pulse to be transmitted while the two circuits remain isolated and then some comment on how isolation is a good thing between the mains and a potentiometer.

(c) A large proportion of candidates scored full marks for their sketch graph of the voltage across the lamp. They clearly related it back to their description of triac behaviour in part (a).

(d) Most candidates scored all the available marks for their calculations of the r.m.s. and peak currents in the lamp.

**Question 3**

(c) It was the exception for a candidate to score full marks for this question and there were many mistakes made and many impossible circuits drawn. The examiners were happy to accept the master and slave wipers as inputs to a summing or to a difference amplifier as long as their potentiometers were powered appropriately. Many drew an integrator between the output of the summing/difference amp and the unity gain power amp and this was penalised because it is mistaking a circuit to provide speed stabilisation with one to provide position stabilisation.

(d) It was the equally the exception for a candidate to score full marks for their explanation of the operation of the circuit and most omitted to say that the amplifier gain of the circuit must be kept low to avoid overshoot and oscillations.

**Question 4**

(a) Most candidates produced very woolly answers to the meaning of the fetch-execute cycle. Many found it impossible to avoid using the words "fetch" and "execute" and this caused the examiners to be confused over the level of their understanding of the term.

(b) Although nearly all candidates scored some marks for their block diagram of a simple microprocessor system many were penalised for poor drawings with, for example, boxes floating with no connections or failure to add a control bus or CPUs from which emerged lots of seemingly different data buses and address buses.

**Question 5**

(a) Only about half the candidates knew the abbreviation BCD meant Binary Coded Decimal despite this being a term mentioned in the final page of the Electronics specifications. Moreover, of those who did know its meaning, very few correctly explained that it was a way of representing a decimal number by a 4-bit binary number.

(b) Only a minority of candidates scored full marks for their drawing of how to connect four BCD to 7-segment decoder drivers to the microprocessor output.
Four of the eight output lines should be a common data bus to which every BCD-7segment display driver is directly connected. One could easily connect sixteen such 7-segment displays to this common bus and then organise an addressing system using sixteen 4-input NAND gates connected to the remaining four output lines - the output of each NAND gate would then drive the common cathode of each individual 7-segment display. However, it was not necessary to draw anything so complicated because the question only asked how to drive four of these displays so the remaining four outputs of the port can simply be connected directly to the common pins W, X, Y and Z.

(c) Very few candidates scored full marks for their explanation of the sequence of output states necessary to show 1234. A common error was to forget that the 7-segment displays are common cathode so the points W, X, Y and Z are active low, not high as most assumed. The microprocessor should output the states E1 D2 B3 and 74 so that each BCD number is activated in sequence from the common data bus. The sequence must be repeated at a reasonably fast rate so that the eye cannot see them being lit up one after another.

**Question 6**

(a) Almost all candidates scored at least two of the three available marks for their description of the behaviour of a D-type flip-flop.

(b) While most candidates correctly realised the chain of four inverters produce a short time delay, fewer explained that this was to allow the counter outputs to be latched before the counters were reset.

(c) For many candidates, the microprocessor program proved to be more demanding than they thought because they wrote at length but failed to score many marks. Clearly, from the stem of the question and the diagram of Fig.6.1, the system converts the analogue input into a two-digit number on the 7-segment displays but many seemed to be just guessing at how it did this. As in previous years, a large number simply used the instruction set to restate the program in simple mnemonics, line by individual line, and for this effort they were unrewarded. To score marks, they had to explain what was going on. The answer should have been as follows:

Output 00 to unfreeze the D-type and make DAC comparator output zero.
Clear the X register contents to 00.
Wait for the switch T to be pushed.
Output +1 to the DAC ramp and a counter high pulse.
Preserve output of +1 to the DAC ramp but pull counter pulse low.
Save the current ramp contents in the X register.
Test the comparator output
If low then jump back to increase the ramp output and apply another counter pulse.
If high then DAC output has just exceeded/reached analogue input level.

(d) In this section, candidates were meant to start at address 40 and move 01 into the accumulator then output it (to latch the counters, reset the D-type and, after the brief time delay, reset the counters). Finally, an absolute jump back to the beginning.

(e) This was perhaps the most difficult question in the paper and very few candidates got it right. The maximum number of steps in the DAC and thus the maximum number of clocking pulses is $2^6 - 1 = 63$.

(f) To score full marks, candidates were expected to point out that after T has been pressed, the microprocessor outputs an ever increasing ramp voltage with a counter pulse being produced for each step of the ramp. When the ramp just exceeds the analogue input, the count reached on the counter is a measure of the analogue input.

**2531 Report-June 2007**

The quality of projects at this level continues to impress with many candidates opting to attempt projects which reflect the work done at Advanced Level. Serial transmitters using radio or wire links are common examples. This is to be encouraged as the experience gained from these projects does help candidates with work from the specification.
Moderators this year reported that the raw marking of the reports was well done and there very few downward adjustments. It is a requirement of the syllabus that reports are annotated to show where marks have been awarded. The easiest way to achieve this is to put red marks in the report indicating the criterion achieved.

The common problems that moderators reported on were as follows:

Specifications can still be weak with many candidates not devoting enough time to do relevant research on a given project. Specifications should be concise but contain the information needed for a full evaluation of the final circuit. Equipment available should also be stated. Alternative circuits (criterion B) were sometimes scantily attempted. Alternatives to 2 subsystems can be done (in addition, of course, to the entire circuit but this is often difficult to achieve). A high scoring alternative would have, as a minimum, a full circuit diagram, a complete description of circuit behaviour, and valid reasons why it was not chosen. Some candidates offered alternatives which were shallow and too brief.

The testing and analysis of subsystems and the final circuit is still problematic for some candidates. It is the responsibility of the candidate to decide how a subsystem is to be tested and how the evidence of the test is to be presented in the report. Simulations are not acceptable as evidence of a test. The building and testing of subsystems satisfies criterion D. The analysis of the test results satisfies criterion E. The two must not be confused. It was quite common to see annotated notes in a report suggesting that a valid test (criterion D) also satisfied some of the criteria descriptors for the analysis section (criterion E). This is not the case and candidates must actually analyse test results in the light of specifications in order to score marks for criterion E.

It is also the responsibility of the candidate to provide evidence that the project actually worked. One would read a report and find little or no evidence that the project actually worked.

There were also discrepancies in the marks awarded for the circuit build. Some centres would award 6/7 marks for a circuit build which would only have scored 4/5 at another centre. For high marks, look for neat positioning of subsystems with a recognisable colour coding, and wires cut to length and not crossing (if at all possible). Remember, an A4 size colour photograph must be included in the report of every candidate so that the circuit build can be clearly seen.

Criterion H is still causing problems for some centres with high marks awarded unjustifiably. To score high marks for this section, candidates must show that little signal degradation takes place when subsystems are connected – this includes the connection of output devices (displays, etc.).

Finally, many candidates did not acknowledge the help of any teaching staff for criterion O – is this possible that no help at all was received by the candidate?

A guide to coursework is available at
www.ocr.org.uk/qualifications/AS_ALevelGCEElectronics.html

**Advanced GCE Electronics (3826, 7826)**
**2007 Assessment Series**

Unit Threshold Marks

| Unit | | Maximum Mark | a | b | c | d | e | u |
|---|---|---|---|---|---|---|---|---|
| **2526** | Raw | 120 | 86 | 77 | 68 | 60 | 52 | 0 |
| | UMS | 120 | 96 | 84 | 72 | 60 | 48 | 0 |
| **2527** | Raw | 90 | 68 | 60 | 53 | 46 | 39 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2528** | Raw | 78 | 62 | 55 | 48 | 41 | 34 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2529** | Raw | 120 | 95 | 85 | 75 | 65 | 56 | 0 |
| | UMS | 120 | 96 | 84 | 72 | 60 | 48 | 0 |
| **2530** | Raw | 90 | 65 | 57 | 49 | 42 | 35 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |
| **2531** | Raw | 90 | 70 | 64 | 58 | 52 | 46 | 0 |
| | UMS | 90 | 72 | 63 | 54 | 45 | 36 | 0 |

Specification Aggregation Results

Overall threshold marks in UMS (i.e. after conversion of raw marks to uniform marks)

| | Maximum Mark | A | B | C | D | E | U |
|---|---|---|---|---|---|---|---|
| **3826** | 300 | 240 | 210 | 180 | 150 | 120 | 0 |
| **7826** | 600 | 480 | 420 | 360 | 300 | 2400 | 0 |

The cumulative percentage of candidates awarded each grade was as follows:

| | A | B | C | D | E | U | Total Number of Candidates |
|---|---|---|---|---|---|---|---|
| **3826** | 22.90 | 37.52 | 55.10 | 68.69 | 82.57 | 100 | 723 |
| **7826** | 31.54 | 51.35 | 70.17 | 83.86 | 96.09 | 100 | 417 |

1140 candidates aggregated this series

For a description of how UMS marks are calculated see;
http://www.ocr.org.uk/exam_system/understand_ums.html

Statistics are correct at the time of publication

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