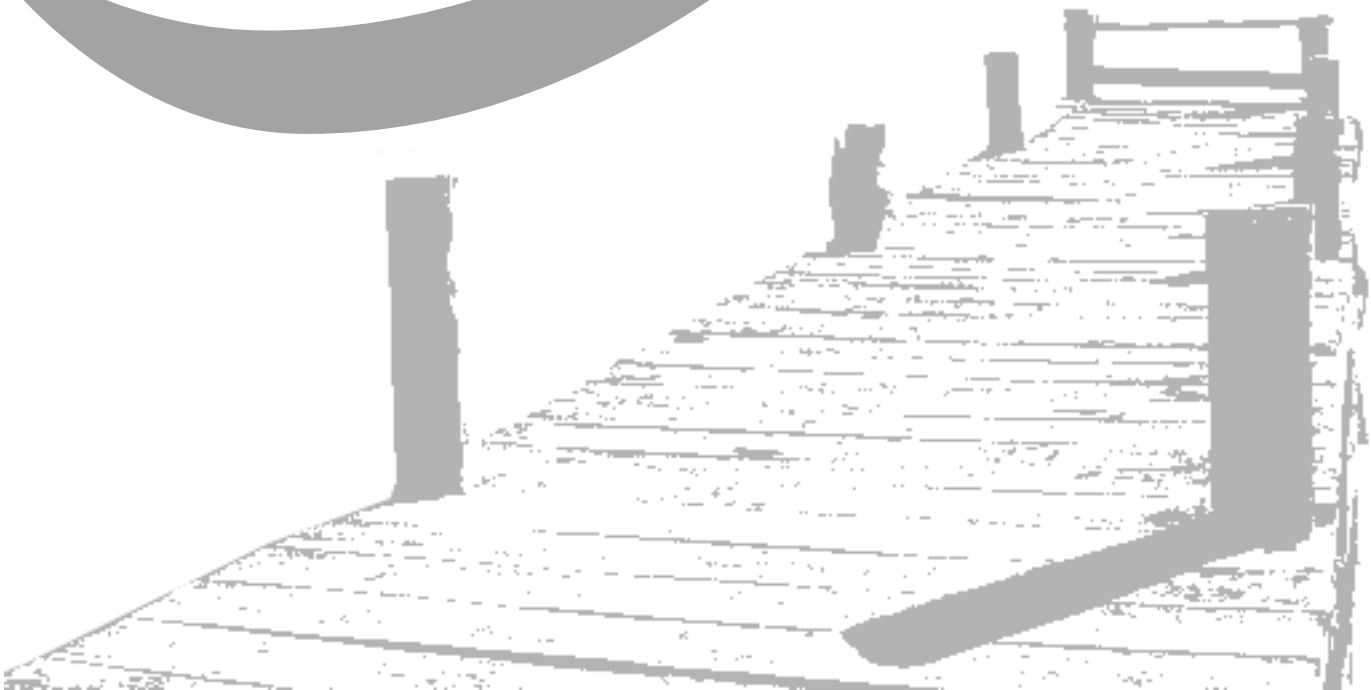
GCE
AS and A Level

# Electronics

AS exams 2009 onwards
A2 exams 2010 onwards

## Unit 2: ELEC2
## Specimen mark scheme

Version 1.1



The specimen assessment materials are provided to give centres a reasonable idea of the general shape and character of the planned question papers and mark schemes in advance of the first operational exams.

For operational papers, mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. The mark scheme includes any amendments made at the standardisation meeting attended by all examiners and is the scheme which was used by them in this examination. The standardisation meeting ensures that the mark scheme covers the candidates' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for the standardisation meeting each examiner analyses a number of candidates' scripts: alternative answers not already covered by the mark scheme are discussed at the meeting and legislated for. If, after this meeting, examiners encounter unusual answers which have not been discussed at the meeting they are required to refer these to the Principal Examiner.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of candidates' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.



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## Mark Scheme

1 (a) A decreasing signal, ✓
takes trigger to less that 1/3 of the $V_s$ etc ✓ *(2 marks)*

(b) Once triggered, the output goes high, ✓
Discharge switches off, ✓
The capacitor charges through the 10kΩ resistor, ✓
Until the voltage across the capacitor is 2/3 $V_s$ ✓
Output goes low, Discharge switches on ✓ *(5 marks)*

(c) $\mathbf{T = 1.1\ R\ C} = 1.1 \times 10^4 \times 10^{-8} = 0.11\text{ms}$ ✓ ✓ *(2 marks)*

*(question total 9 marks)*

2 (a) Differential voltage gain = $\mathbf{R_f / R_1}$ ✓
$\Rightarrow G_v = 10^6/10^5 = 10$ ✓ ✓ *(3 marks)*

(b) $\mathbf{V_{out} = (V_+ - V_-) \times R_f / R_1} = -0.2 \times 10 = -2\text{V}$ ✓ ✓ *(2 marks)*

(c) Signal 2 is subtracted from Signal 1 by the difference amplifier ✓
The noise is common to both signals and so will be reduced (disappear) ✓
The two microphone signals will also be subtracted but since signal 2 is the inverse of signal 1, the output will be twice signal 1 (or 2) ✓ ✓ *(4 marks)*

*(question total 9 marks)*

3 (a) D connected to $\overline{\mathbf{Q}}$ ✓
CK connected to previous $\overline{\mathbf{Q}}$ ✓
All resets connected together ✓
Output of AND gate connected to reset ✓
Output C to AND gate ✓
Output D to AND gate ✓ *(max 5 marks)*

(b)

| Hours | D | C | B | A |
|---|---|---|---|---|
| first | 0 | 0 | 0 | 0 |
| second | 0 | 0 | 0 | 1 |
| third | 0 | 0 | 1 | 0 |
| tenth | 1 | 0 | 0 | 1 |
| last | 1 | 0 | 1 | 1 |

(minus 1 per error) ✓ ✓ ✓ ✓ *(4 marks)*

*(question total 9 marks)*

4 (a) summing amplifier, mixer etc ✓ *(1 mark)*

(b) (i) Voltage gain of 5

(ii) Increase feedback resistor by a factor of 5 to 500kΩ ✓ ✓ *(3 marks)*

(c) (i) Additional resistor added ✓
To inverting input ✓

(ii) It needs four times the gain of the others ✓
calculation ✓
=>resistor value = 25kΩ ✓ *(5 marks)*

*(question total 9 marks)*

5 (a) On each rising edge of the clock pulse ✓
Q becomes equal to D ✓ *(2 marks)*

(b) On each rising edge of the clock pulse ✓
The logic state of each flip-flop is moved to the next flip-flop along ✓
The logic state of D of the first flip-flop is transferred to Q of the first flip-flop ✓ *(3 marks)*

(c)

| $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | D input of first flip-flop |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |

✓ ✓ ✓ ✓ *(4 marks)*

*(question total 9 marks)*

6 (a) 0 to ½$V_s$ ✓ *(1 mark)*

(b) **T = 0.69 x R x C** = 0.69 x $10^4$ x $10^{-7}$ = 0.69ms ✓ ✓ *(2 marks)*

(c) (i) Voltage follower, buffer etc ✓

(ii) To prevent the output circuit altering the charging rate of the capacitor ✓ *(2 marks)*

(d) (i) The NOT gate switches at half of the supply voltage ✓
0.7ms is the time taken for the capacitor to charge to this value ✓

(ii) The curve shows the way in which the capacitor voltage changes with time (or exponential charge curve) ✓
The vertical line is when the MOSFET rapidly discharges the capacitor ✓ *(4 marks)*

*(question total 9 marks)*

7 (a) Non-inverting amplifier ✓
$\mathbf{G_v = 1 + R_f / R_1} = 1 + 2200/10 = 221$ ✓ *(2 marks)*

(b) $10^6 = 221 \times f$ ✓
$\Rightarrow f = 10^6 / 221 = 4.525\text{kHz}$ ✓ *(2 marks)*

(c) (i) Cross over distortion ✓

(ii) Apply a bias voltage to each MOSFET ✓
So that each MOSFET is just conducting ✓
There is a quiescent current ✓
Use voltage divider. diodes etc to produce the bias voltage ✓
etc *(3 marks)*

(d) Output voltage trying to exceed the supply voltage ✓
Output clipped to the supply voltage ✓
Gain of amplifier set too high ✓
etc *(3 marks)*

(e) $\mathbf{P = V_s^2 / (2 \times R)} = 12^2/(2 \times 8) = 144 / 16 = 9\text{W}$ ✓ ✓ ✓ *(3 marks)*

*(question total 13 marks)*

**Paper = 67**