AQA

AS
ELECTRONICS

ELEC2 Further Electronics
Mark scheme

2430
June 2016

Version: 1.0 Final

Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts. Alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

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Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
1	(a)	(i)	Input to + input and output from output ✓, link from output to – input ✓	2	
1	(a)	(ii)	1 or +1 or 'one' or 'unity' (not -1 or 'unit')	1	
1	(a)	(iii)	Voltage follower acts as a buffer or has a very large input resistance Reference to situation e.g. matches output resistance of microphone to input of amplifier - To ensure that most of the output voltage from the microphone is not lost across its internal resistance / or does not draw current from mic	1 1	
1	(b)		Resistor from Vin1 to + input, resistor from Vin2 to - input, feedback resistor from - input to output, resistor from + input to 0V	4	
1	(c)		Substitution into formula, Vout = Vin x gain Correct answer 2V	1 1	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
2	(a)	(i)	resistor from +Vs to discharge ✓, threshold and trigger connected ✓, resistor between discharge and trigger/threshold ✓, capacitor between trigger/threshold and 0V ✓	4	
2	(b)	(i)	Correct substitution in $t_l=0.7R_bC$ ✓, $R_b = 70 \times 10^{-3} / (0.7 \times 10 \times 10^{-6}) = 10k$✓	2	
2	(b)	(ii)	Correct substitution in $t_h=0.7C(R_a+R_b)$✓, $(0.43/(0.7 \times 10 \times 10^{-6})) – (10 \times 10^{3})$ $=51.4k\Omega$ ✓	2	
2	(c)		+ of buzzer to $+V_s$ ✓, other connection to V_{out} ✓	2	**Allow any valid driver**
2	(d)		replace R_a with a variable resistor.✓	1	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
3	(a)		B ✓	1	
3	(b)		Q to following D ✓, All Rs connected together ✓, All CKs connected together ✓, D_0 labelled as (serial) input ✓	4	
3	(c)	(i)	flip-flop reset / Q=0 / Q'=1 ✓	1	
3	(c)	(ii)	All off / Sign not illuminated ✓	1	
3	(d)	(i)	A new LED will light and stay lit on each clock pulse ✓, from left to right / Q0 to Q3✓	2	
3	(d)	(ii)	LEDs switch off and stay off on each clock pulse (going from left to right / Q0 to Q3) ✓, until serial input is logic 1 again and process repeats ✓	2	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
4	(a)		D to Q' ✓, all Rs connected and connected to AND gate output ✓,CK to previous Q' ✓,Q1 and Q3 to AND gate input ✓, clock input labelled ✓	5	
4	(b)		Multiple input signals (bounce) ✓, each time the contacts close ✓	2	
4	(c)	(i)	Only one input pulse can be produced ✓ Capacitor discharges instantly on first contact to 0V ✓ Capacitor holds the input low ✓ (during switch bounce) Capacitor takes time to charge through R✓	2 (max)	
4	(c)	(ii)	Value of T from oscilloscope trace ✓(e.g. between 0.1s and 1.2s) Use of T=RC or $T^1/_2$=0.69RC ✓ Leading to realistic value of capacitor ✓ (e.g. C between 10µF and 180µF)	3	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
5	(a)	(i)	-5 V ✓	1	
5	(a)	(ii)	100kHz ✓	1	
5	(a)	(iii)	realisation that the input resistance of amplifier is 10kΩ ✓, use of V=IR to calculate current correctly ✓	2	
5	(a)	(iv)	current passes through input resistor✓ through feedback resistor ✓ NOT into the input terminal of the op-amp✓	2 (max)	
5	(b)	(i)	Use of 50V and 1uA in R=V/I✓ to calculate resistance of 50MΩ ✓	2	
5	(b)	(ii)	1uA current through feedback resistor ✓, use of V=IR ✓ , -10V ✓ Or use of amplifier voltage gain formula Vout = -Rf/Ri x Vin ✓= -10M/50M x 50V ✓= -10V✓	3	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
6	(a)		Use of inverting amplifier formula ✓, to give a gain of -4.7 ✓, assuming gain of source follower is 1 (0.6 to 1)✓	3	
6	(b)		Biases the MOSFETs ✓(into conduction), to reduce cross-over distortion ✓	2	
6	(c)	(i)	summing amplifier	1	
6	(c)	(ii)	Gain = -10 so 2V x-10=-20V ✓ But amplifier saturates so output = -10V to -12V ✓	2	
6	(c)	(iii)	motor continues to rotate / voltage from B continues to decrease ✓ amplifier stops being saturated / V_{out} becomes smaller magnitude✓ when voltage at B is about -1V ✓ motor slows down ✓ and comes to a stop when voltage at B is {almost} -2V or V_{out} is almost 0V✓ Reference to overshoot / hunting ✓	3 (max)	