AQA

AS
ELECTRONICS
ELEC1

INTRODUCTORY ELECTRONICS

Mark scheme
June 2016

Version: 1.0 Final

Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts. Alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

Further copies of this mark scheme are available from aqa.org.uk

<table>
<tr><th>Question</th><th>Part</th><th>Sub-part</th><th>Answer</th><th>Mark</th><th>Comments/ Guidance</th></tr>
<tr><td>1</td><td>(a)</td><td></td><td>
<table>
<tr><th>B</th><th>A</th><th></th><th>C</th><th>D</th><th>E</th><th>F</th><th></th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td></td><td>1</td><td>1</td><td>0</td><td>0</td><td></td><td>0</td></tr>
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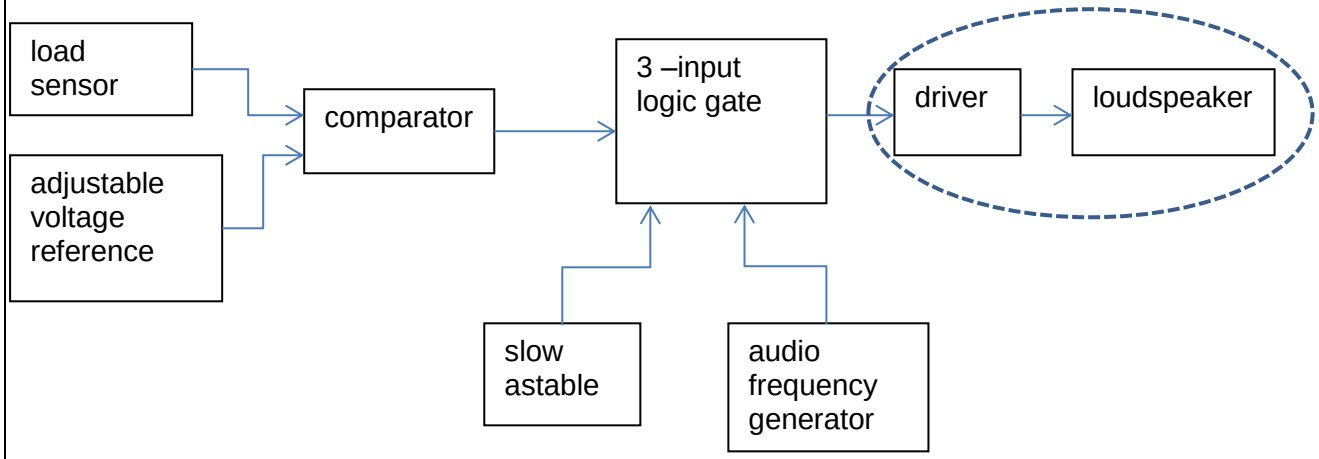
<tr><td>1</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>0</td></tr>
</table>
</td><td>5</td><td>One mark per column</td></tr>
<tr><td>1</td><td>(b)</td><td>(i)</td><td>E = $\overline{A}$. B</td><td>1</td><td></td></tr>
<tr><td>1</td><td>(b)</td><td>(ii)</td><td>F = $A . \overline{B}$</td><td>1</td><td></td></tr>
<tr><td>1</td><td>(b)</td><td>(iii)</td><td>Q = $\overline{A}$B + A$\overline{B}$ / also accept A $\oplus$ B</td><td>1
1</td><td>Correct terms /
OR gate</td></tr>
<tr><td>1</td><td>(c)</td><td></td><td>AND EXOR NOR NAND OR</td><td>1</td><td></td></tr>
</table>

2	**(a)**			**7**	

2	**(b)**	**(i)**	driver	**1**	

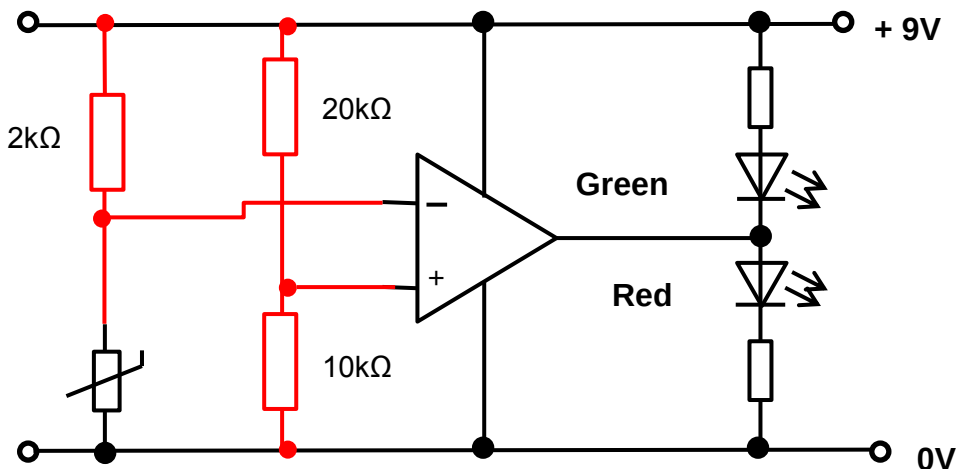
2	**(b)**	**(ii)**	adjustable voltage reference	**1**	

2	**(b)**	**(iii)**	comparator (also accept - audio frequency generator/slow astable)	**1**	

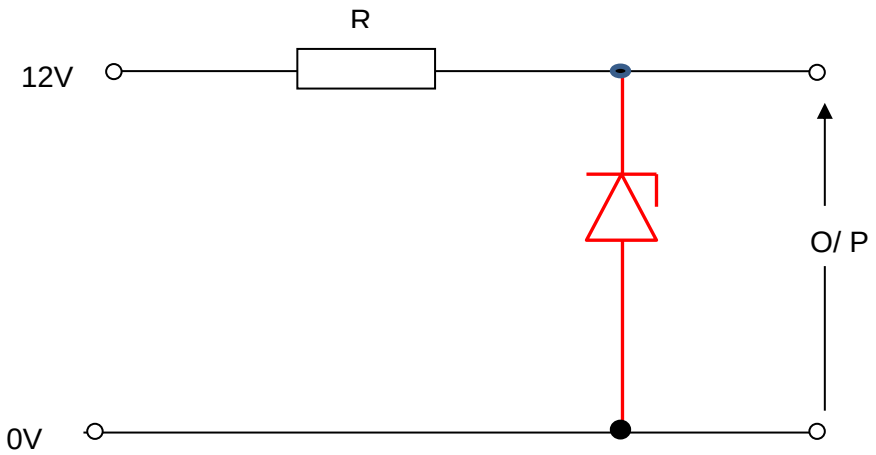
3	**(a)**	**(i)**	Negative Temperature Coefficient .	**1**	

3	**(a)**	**(ii)**	As the temperature increases, the resistance decreases or negative gradient .	**1**	

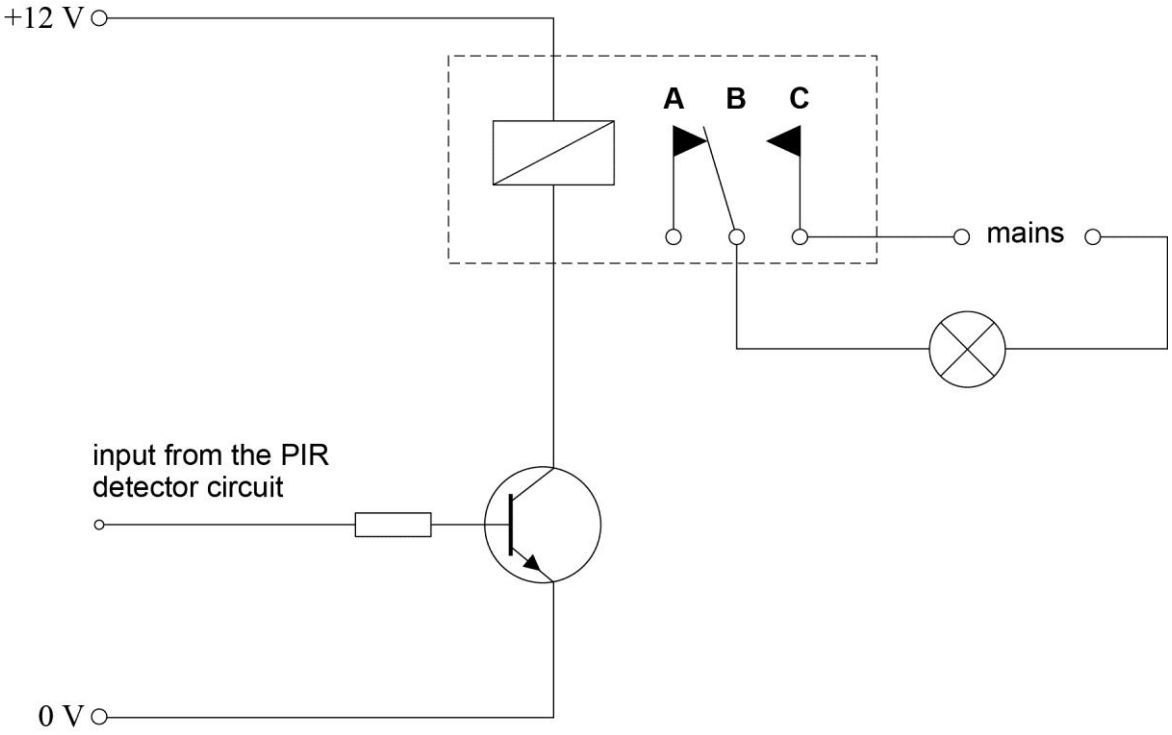
3	**(b)**		Thermistor (C) This thermistor gives the largest change in resistance over the stated temperature range	**2**	

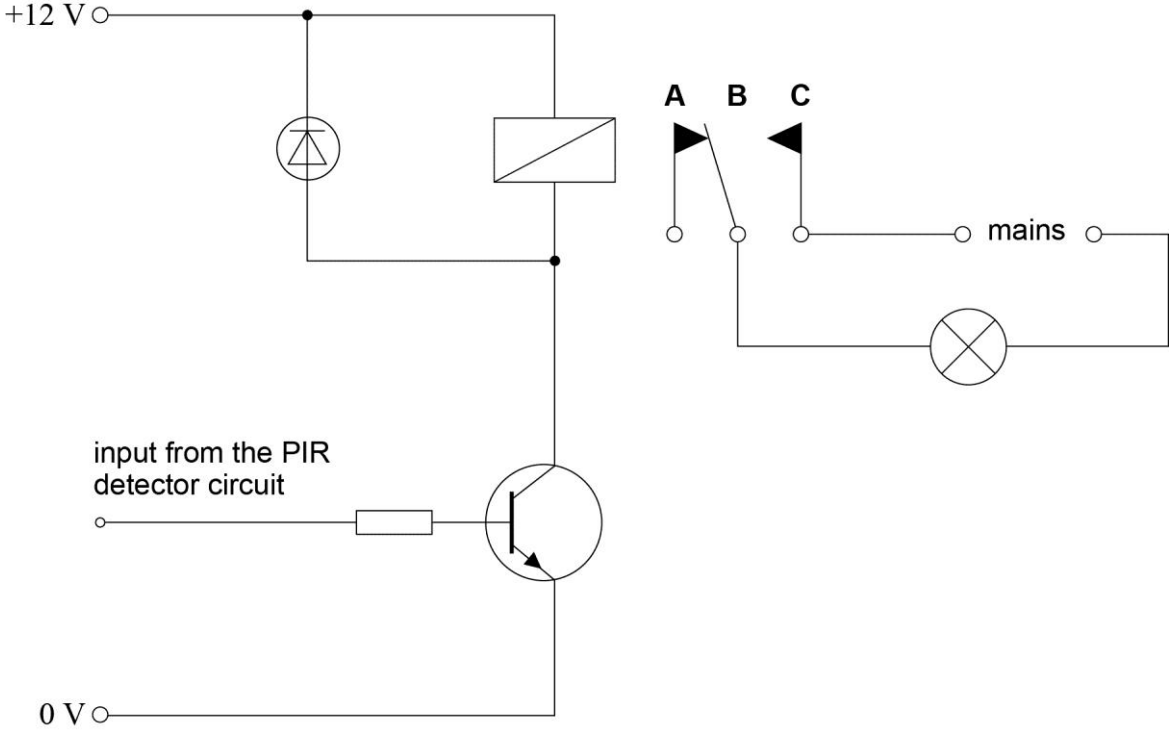
3	**(c)**		 Complete detector voltage divider Complete reference voltage divider / correct resistor values / resistor range 1KΩ → 2MΩ Correct connection to Op Amp inputs	**1** **3** **1**	

3	**(d)**		The real OP amp is likely to saturate above OV rail and below the 9V rail. Discussion as to how outputs from Op Amp affect the Red and Green LEDs given that they require 1.7V and 2.5V respectively to switch on.	**1** **2**	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
4	(a)	(i)	7.5V	1	
4	(a)	(ii)	10mA	1	
4	(b)		 Correct circuit symbol Correct place Correct way around	 1 1 1	

4	**(c)**	**(i)**	Use of V= 6.9v I= 505mA Answer R = 13.66Ω	**2** **1**	
4	**(c)**	**(ii)**	13 Ω (must include unit) Must be lower than calculated Ensures that Zener current is: not less than 5mA when delivering max load. Or is large enough to maintain Zener voltage.	**1** **1** **1**	
4	**(c)**	**(iii)**	I = V/R = $\frac{6.9}{13}$ = 0.53 A P = I x V = 0.53 x 5.1 = 2.7W (accept 2.6W if calculated R used)	**1** **2**	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
5	(a)	(i)	Resistor on input line Correct transistor symbol drawn in correct place 	1 1	

5	**(a)**	**(ii)**	A **reverse bias diode** drawn in **parallel** with the coil (Reverse diode across the collector emitter) 	**2**	

5	**(a)**	**(iii)**	Back emf (coil) when transistor is switched (off) could damage the transistor. Reverse bias diode used to tie high induced voltage to top rail of power supply.	**2**	

5	**(b)**		The relay coil needs I = V/R, I = 12V / 160Ω, I = 75mA But I_c = Gain x I_b hence 150 x 0.5mA =75mA so Gain must be at least 150	**1** **2**	

5	**(c)**		<table><tr><th>Contact A</th><th>Contact B</th><th>Contact C</th><th>Configuration</th><th></th></tr><tr><td>NC</td><td>COM</td><td>NO</td><td>SPST</td><td></td></tr><tr><td>COM</td><td>NC</td><td>NO</td><td>SPDT</td><td></td></tr><tr><td>NC</td><td>COM</td><td>NO</td><td>SPDT</td><td>✓</td></tr><tr><td>NO</td><td>COM</td><td>NC</td><td>SPDT</td><td></td></tr><tr><td>NO</td><td>COM</td><td>NC</td><td>SPST</td><td></td></tr></table>	**1**	

5	**(d)**		MOSFET has a very high input resistance so won't demand current from previous stage Or Higher current gain Or lower power dissipation	**1**	

<table>
<tr><th>Question</th><th>Part</th><th>Sub-part</th><th>Answer</th><th>Mark</th><th>Comments/ Guidance</th></tr>
<tr><td>6</td><td>(a)</td><td></td><td>
<table>
<tr><th>C</th><th>B</th><th>A</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
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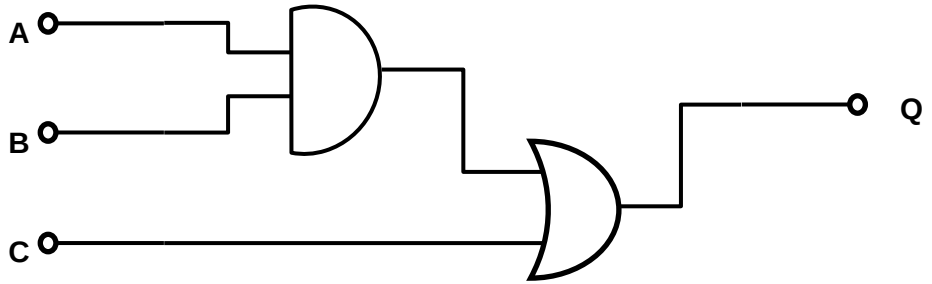
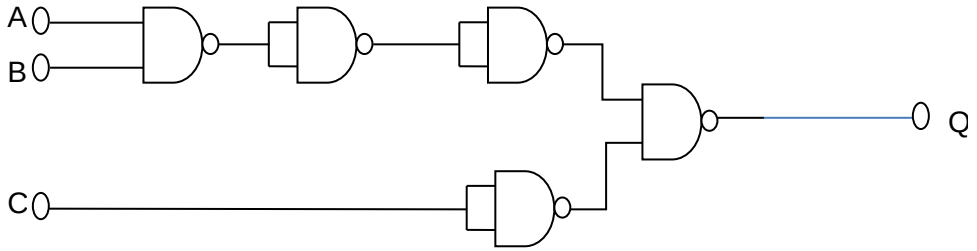
</table>
</td><td>1</td><td></td></tr>
<tr><td>6</td><td>(b)</td><td></td><td>The expression is constructed by using the lines of the truth table –
Q=1 where one line OR another is correct (OWTTE)</td><td>2</td><td></td></tr>
</table>

6	(c)		**Q = A.B.C + $\overline{A}$.B.C + A.$\overline{B}$.C + $\overline{A}$.$\overline{B}$.C + A.B.$\overline{C}$** **Q = B.C +$\overline{B}$ .C + A.B.$\overline{C}$** **Q = C + A.B.$\overline{C}$** **Q = C + A.B** 3 marks for two reductions and 1 identity **OR** **Diagram** Karnaugh map correctly completed 2 groups correctly identified Terms correctly identified from groupings	**1** **1** **1**	

B A / C	0 0	0 1	1 1	1 0
0			1	
1	1	1	1	1

6	**(d)**	**(i)**	 1 correct AND gate / position Plus correct OR gate / position	**1** **1**	

6	**(d)**	**(ii)**	 AND gate implemented with NAND gates OR gate implemented with NAND gates (Allow simplified version) for 2 marks	**1** **1**	