



AS
ELECTRONICS
ELEC1

INTRODUCTORY ELECTRONICS

Mark scheme

June 2016

Version: 1.0 Final

Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts. Alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

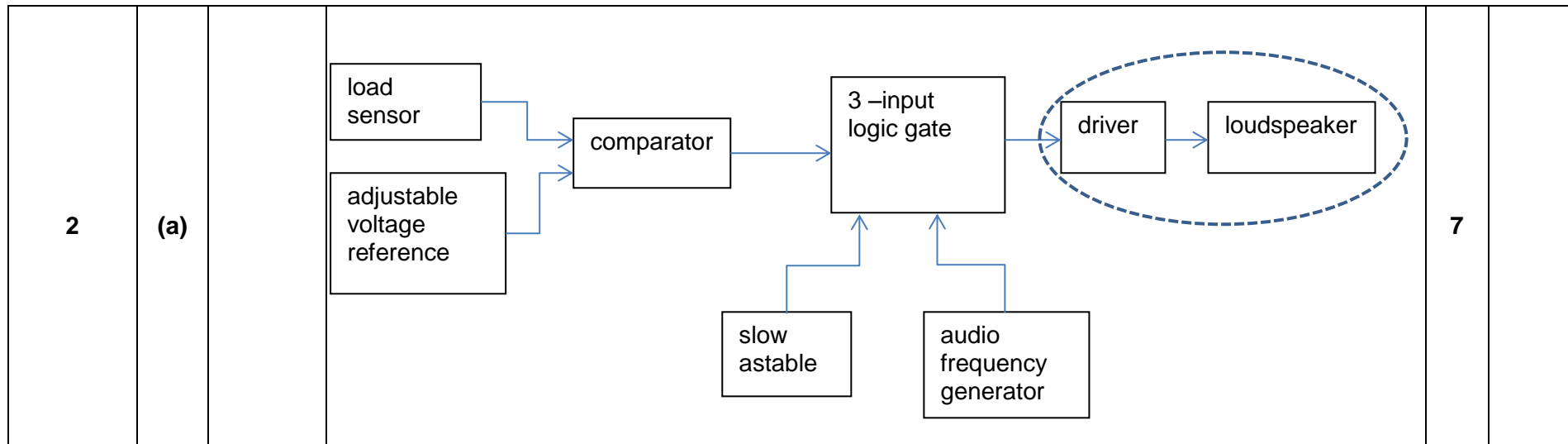
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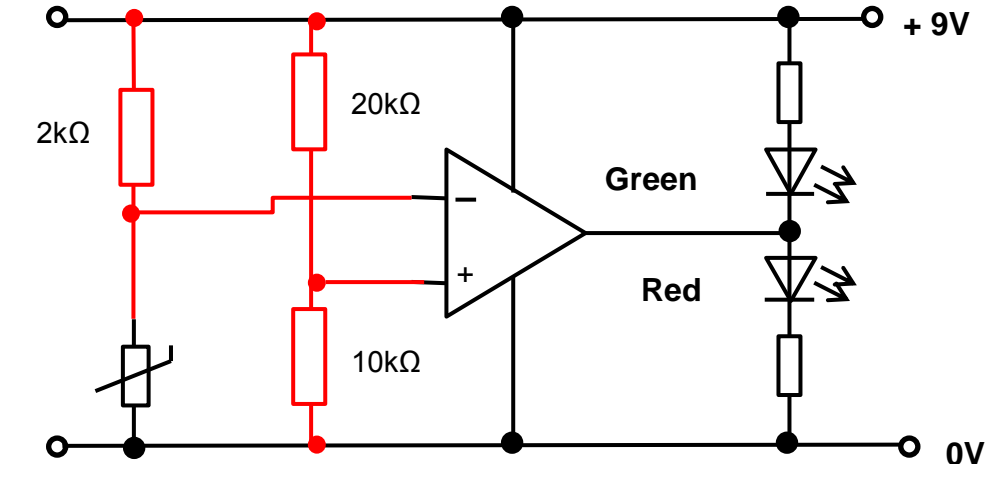
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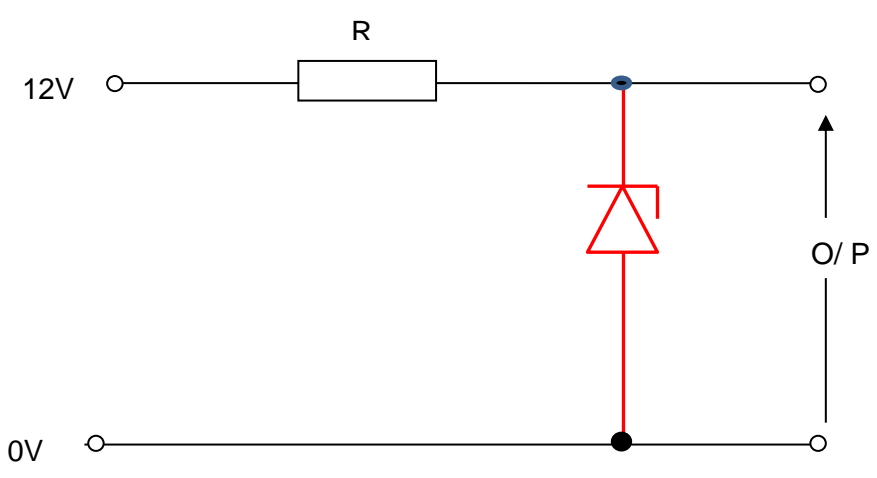
Question	Part	Sub-part	Answer	Mark	Comments/ Guidance																																			
1	(a)		<table border="1"> <thead> <tr> <th>B</th> <th>A</th> <th>C</th> <th>D</th> <th>E</th> <th>F</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> </tbody> </table>	B	A	C	D	E	F	Q	0	0	1	1	0	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	1	1	1	0	0	0	0	0	5	One mark per column
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1	1	0	0	0	0	0																																		
1	(b)	(i)	$E = \bar{A} \cdot B$	1																																				
1	(b)	(ii)	$F = A \cdot \bar{B}$	1																																				
1	(b)	(iii)	$Q = \bar{A}B + A\bar{B}$ / also accept $A \oplus B$	1 1	Correct terms / OR gate																																			
1	(c)		AND EXOR NOR NAND OR	1																																				



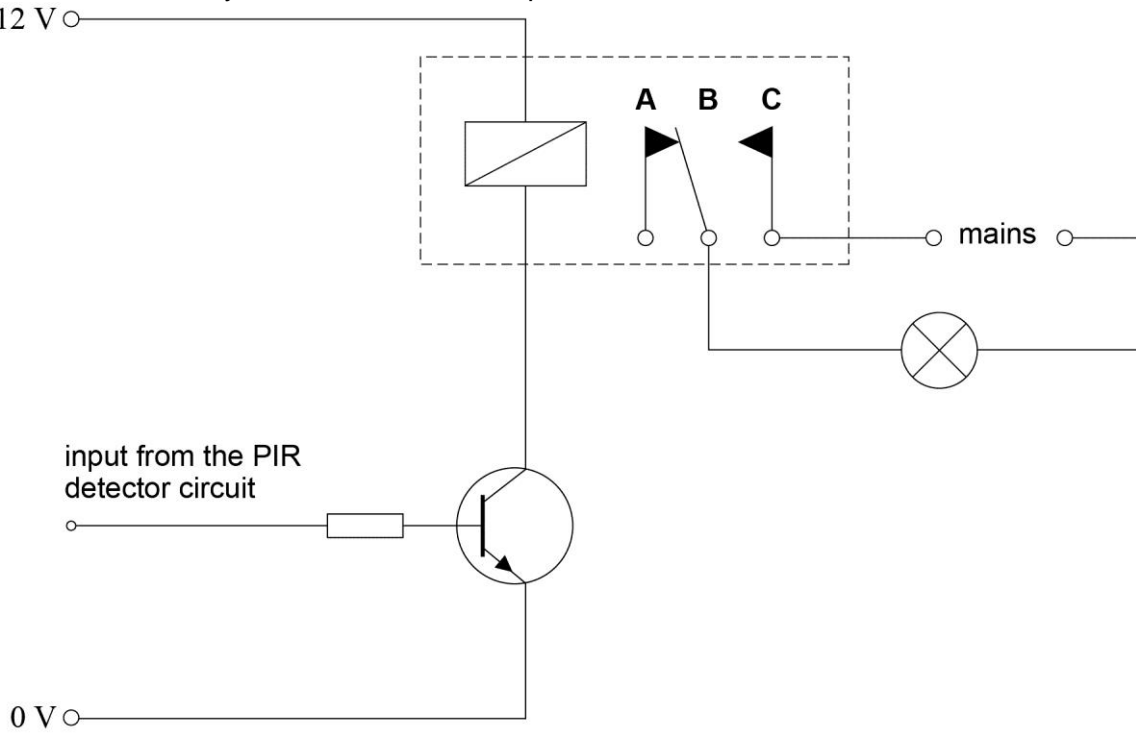
2	(a)			7
2	(b)	(i)	driver	1
2	(b)	(ii)	adjustable voltage reference	1
2	(b)	(iii)	comparator (also accept - audio frequency generator/slow astable)	1

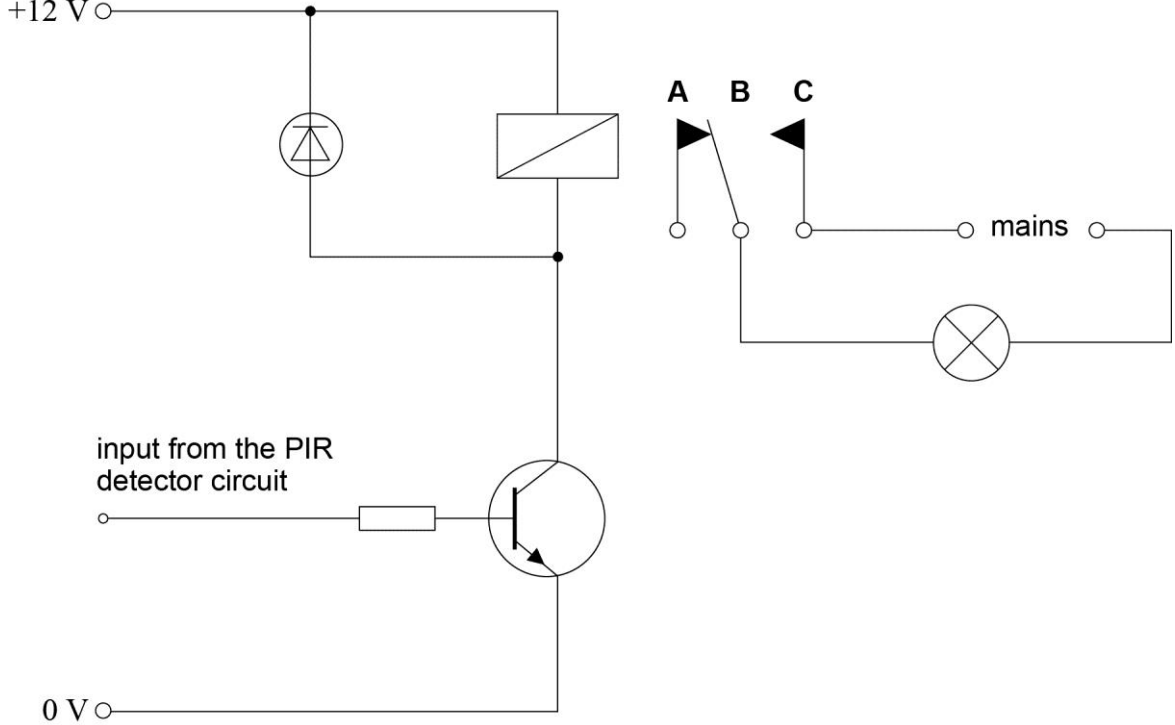
3	(a)	(i)	Negative Temperature Coefficient	1	
3	(a)	(ii)	As the temperature increases, the resistance decreases or negative gradient	1	
3	(b)		Thermistor (C) This thermistor gives the largest change in resistance over the stated temperature range	2	

<p>3</p>	<p>(c)</p>	 <p>Complete detector voltage divider Complete reference voltage divider / correct resistor values / resistor range $1\text{K}\Omega \rightarrow 2\text{M}\Omega$ Correct connection to Op Amp inputs</p>	<p>1 3 1</p>	
<p>3</p>	<p>(d)</p>	<p>The real OP amp is likely to saturate above 0V rail and below the 9V rail. Discussion as to how outputs from Op Amp affect the Red and Green LEDs given that they require 1.7V and 2.5V respectively to switch on.</p>	<p>1 2</p>	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
4	(a)	(i)	7.5V	1	
4	(a)	(ii)	10mA	1	
4	(b)		 <p>The diagram shows a circuit with a 12V DC source on the left. A resistor labeled 'R' is connected in series with the positive terminal of the source. Following the resistor, a diode is connected in parallel to the common ground (0V) terminal. The diode's cathode is connected to the common ground, and its anode is connected to the node between the resistor and the diode. The output terminals are on the right, with the top terminal connected to the node between the resistor and the diode, and the bottom terminal connected to the common ground. An arrow labeled 'O/P' indicates the output voltage across these terminals.</p>	<p>Correct circuit symbol Correct place Correct way around</p> <p>1 1 1</p>	

4	(c)	(i)	Use of $V = 6.9\text{v}$ $I = 505\text{mA}$ Answer $R = 13.66\Omega$	2 1	
4	(c)	(ii)	13 Ω (must include unit) Must be lower than calculated Ensures that Zener current is: not less than 5mA when delivering max load. Or is large enough to maintain Zener voltage.	1 1 1	
4	(c)	(iii)	$I = V/R = \frac{6.9}{13} = 0.53 \text{ A}$ $P = I \times V = 0.53 \times 5.1 = 2.7\text{W}$ (accept 2.6W if calculated R used)	1 2	

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance
5	(a)	(i)	<p>Resistor on input line Correct transistor symbol drawn in correct place</p> 	1 1	

5	(a)	(ii)	<p>A reverse bias diode drawn in parallel with the coil (Reverse diode across the collector emitter)</p> 	2	
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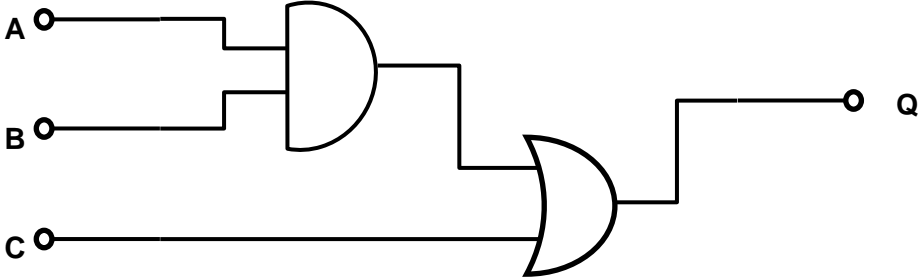
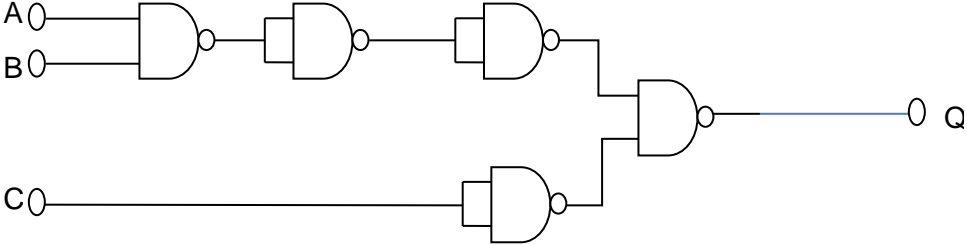
5	(a)	(iii)	<p>Back emf (coil) when transistor is switched (off) could damage the transistor. Reverse bias diode used to tie high induced voltage to top rail of power supply.</p>	2	
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5	(b)		<p>The relay coil needs $I = V/R$, $I = 12V / 160\Omega$, $I = 75mA$ But $I_c = \text{Gain} \times I_b$ hence $150 \times 0.5mA = 75mA$ so Gain must be at least 150</p>	1	
				2	

5	(c)		Contact A	Contact B	Contact C	Configuration	1		
			NC	COM	NO	SPST			
			COM	NC	NO	SPDT			
			NC	COM	NO	SPDT			✓
			NO	COM	NC	SPDT			
			NO	COM	NC	SPST			
5	(d)	MOSFET has a very high input resistance so won't demand current from previous stage Or Higher current gain Or lower power dissipation				1			

Question	Part	Sub-part	Answer	Mark	Comments/ Guidance																																				
6	(a)		<table border="1"> <thead> <tr> <th>C</th> <th>B</th> <th>A</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	C	B	A	Q	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1	1	1	
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6	(b)		The expression is constructed by using the lines of the truth table – Q=1 where one line OR another is correct (OWTTE)	2																																					

6	(c)	<p> $Q = A.B.C + \bar{A}.B.C + A.\bar{B}.C + \bar{A}.\bar{B}.C + A.B.\bar{C}$ $Q = B.C + \bar{B}.C + A.B.\bar{C}$ $Q = C + A.B.\bar{C}$ $Q = C + A.B$ </p> <p>3 marks for two reductions and 1 identity</p> <p style="text-align: center;">OR</p> <p style="text-align: center;">Diagram</p> <table border="1" style="margin: 10px auto;"> <tr> <td style="text-align: center;">BA C</td> <td style="text-align: center;">00</td> <td style="text-align: center;">01</td> <td style="text-align: center;">11</td> <td style="text-align: center;">10</td> </tr> <tr> <td style="text-align: center;">0</td> <td></td> <td></td> <td style="text-align: center;">1</td> <td></td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> </tr> </table> <p> Karnaugh map correctly completed 2 groups correctly identified Terms correctly identified from groupings </p>	BA C	00	01	11	10	0			1		1	1	1	1	1	<p>1 1 1</p>	
BA C	00	01	11	10															
0			1																
1	1	1	1	1															

<p>6</p>	<p>(d)</p>	<p>(i)</p>	 <p>1 correct AND gate / position Plus correct OR gate / position</p>	<p>1 1</p>	
<p>6</p>	<p>(d)</p>	<p>(ii)</p>	 <p>AND gate implemented with NAND gates OR gate implemented with NAND gates (Allow simplified version) for 2 marks</p>	<p>1 1</p>	