
A-LEVEL

Electronics

Further Electronics ELEC2

Mark scheme

2430

June 2015

Version/Stage: V1 Final Mark Scheme

Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts. Alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

Further copies of this mark scheme are available from aqa.org.uk

Question	Part	Sub part	Marking Guidance	Mark	Comments
1	(a)	(i)	A	1	(at inverting input)
1	(a)	(ii)	a point on the circuit where the voltage is 0v / ground but not connected to 0v / is almost 0v / simulates 0v assuming that the op-amp has not saturated	2 max	
1	(a)	(iii)	10k Ω (must have units unless 10,000 which assumes standard)	1	oe 10,000 Ω / 10K etc
1	(b)		correct formula rearranged Calculation / substitution 470k Ω	3	3 for just correct answer with units
1	(c)		inverted, same frequency, shape shows evidence of correct gain maximum amplitude 3v to 5v	4	

Question	Part	Sub part	Marking Guidance	Mark	Comments										
2	(a)		2 x two input NAND gates in parallel, cross coupled, other inputs to \bar{S} and \bar{R} , outputs to Q and \bar{Q}	4											
2	(b)		<table border="1" style="display: inline-table; vertical-align: middle;"> <thead> <tr> <th>Q</th> <th>\bar{Q}</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1✓</td> <td>1✓</td> </tr> </tbody> </table> See above one mark each for lines 2 and 3, 2 marks for line 4	Q	\bar{Q}	0	1	1	0	0	1	1✓	1✓	4	
Q	\bar{Q}														
0	1														
1	0														
0	1														
1✓	1✓														
2	(c)		Resistance of thermistor @ 50°C = 20kΩ, switching point when input = 2.5V, so R = 20kΩ	3											

Question	Part	Sub part	Marking Guidance	Mark	Comments
3	(a)	(i)	Cross-over (distortion)	1	
3	(a)	(ii)	Mention of transistors / MOSFETS Need a certain input voltage before they conduct / 'non-linear' behaviour. For low voltage signals, output is 0V.	3	
3	(a)	(iii)	Bias the output transistors (into conduction) OR apply negative feedback (around the whole amplifier)	1	Allow increased gain which does <u>reduce</u> the crossover distortion
3	(b)	(i)	Clipping or saturation (distortion)	1	
3	(b)	(ii)	The voltage gain is too large / the power supply voltage is too low / the input is too large making the output transistors saturate .	2	
3	(b)	(iii)	reduce the voltage gain / increase the power supply voltage / reduce input signal	1	
3	(c)		Formula $P = (\text{PEAK})^2 / 2R$ $= 20^2 / 16$ (20v found from 2 divisions at 10v/division) $= 25W$	3	Using a justified choice for V Alternative rms solution.

Question	Part	Sub part	Marking Guidance	Mark	Comments																																
4	(a)		when the clock signal goes from 0 to 1 / rises Q becomes equal to D	2	(Not when the clock <u>IS</u> high)																																
4	(b)		\overline{Q} connected to D input to clock output from Q or \overline{Q}	3																																	
4	(c)		<table border="1" style="margin-left: auto; margin-right: auto;"> <tbody> <tr> <td>4</td> <td>↑</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>5</td> <td>↑</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>6</td> <td>↑</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>7</td> <td>↑</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>one mark for each correct row</p>	4	↑	0	0	1	1	0	1	5	↑	1	0	1	1	1	0	6	↑	1	1	0	0	1	0	7	↑	0	1	0	0	0	1	4	
4	↑	0	0	1	1	0	1																														
5	↑	1	0	1	1	1	0																														
6	↑	1	1	0	0	1	0																														
7	↑	0	1	0	0	0	1																														
4	(d)	(i)	4:1	1																																	
4	(d)	(ii)	1 clock cycle	1	Allow 3 clock cycles / 90°																																

Question	Part	Sub part	Marking Guidance	Mark	Comments
5	(a)		Formula rearranged, substitution, $0.72\mu\text{F}$	3	
5	(b)		a falling signal / going low going to less than 1/3 of the supply voltage, shorter period than monostable	2 max	Not <u>IS</u> low.
5	(c)	(i)	input to trigger (and nowhere else), and must be clearly labelled threshold to junction of C and variable resistor, discharge to junction of C and variable resistor.	3	IF last 2 marks not gained, can award 1 if threshold joined to discharge
5	(c)	(ii)	to limit the current flowing through discharge (when variable resistor is set to a low resistance).	1	Allow to protect 555
5	(c)	(iii)	$T = 0.1\text{s}$ substitution into monostable formula giving 605k	2	ECF for incorrect T Allow 606k

Question	Part	Sub part	Marking Guidance	Mark	Comments
6	(a)		calculation of $(0.718V - 0.619V)/100\text{ }^{\circ}\text{C}$ (= 99mV/ $^{\circ}\text{C}$)	1	
6	(b)		a series resistor to the inverting input, a series resistor to the non-inverting input, a resistor from the output to inverting input, a resistor from the non-inverting input to 0V	4	
6	(c)		voltmeter will display 5V for 50 $^{\circ}\text{C}$ change = 0.1V/ $^{\circ}\text{C}$. Diode produces 50mV for 50 $^{\circ}\text{C}$ change = 1mV/ $^{\circ}\text{C}$ So voltage gain needed is 0.1V/1mV or 5V/50mV (= 100)	3	Use of V_{out} / V_{in} given an appropriate temperature range.
6	(d)		Use of difference amplifier formula rearranged substitution 15k x 100 = 1.5 M Ω (1,500k)	3	For 3 marks must have units