## 

## A-LEVEL **Electronics**

ELEC1 – Introductory Electronics Mark scheme

2430 June 2015

Version V1: Final Mark Scheme

Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts. Alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

Further copies of this mark scheme are available from aqa.org.uk

Copyright © 2015 AQA and its licensors. All rights reserved.

AQA retains the copyright on all its publications. However, registered schools/colleges for AQA are permitted to copy material from this booklet for their own internal use, with the following important exception: AQA cannot give permission to schools/colleges to photocopy any material that is acknowledged to a third party even for internal use within the centre.



															1 mark for row L						
				Α	В	а	b	С	d	е	f	g	Display		1 mark for row S (both)						
				0	0	0	0	0	1	1	1	0	L								
2	(a)			0	1	1	0	1	1	0	1	1	S	3							
				1	0	1	0	1	1	0	1	1	S								
										1 1	1	0	1	1	0	1	1	1	Н		
					•		•	•	•	•	•										
2	(b)		EXOR g	gate										1							
			-																		
			Commo	n cat	hode	displa	y requ	uires lo	ogic 1	applie	d to s	egmen	t as all cathodes are hel	d	Two points made						
2	(c)		low											2							
			Commo	n and	nde re	auire	s logic	0 to b	e ann	lied to	liaht	each se	ament								
L		I					, logio	0.00	- upp		igne										
2	(d)	(i)	Differen	t com	binat	ions p	roduc	e diffe	rent b	rightn	ess			1	1 Disadvantage						
														÷							
2	(d)	(ii)	R=V/I; (	5V –	2.2V)	/ 20m	nA; 2.8	3V/20n	nA = 1	40Ω				2	1 mark for 2.8V drop						
<u> </u>	(4)	(")												-	1 mark for answer						
	( 1)	(111)																			
2	(d)	(iii)	E24 = 1	50Ω										1	1 mark for answer						

3	(a)		x s 12V0 R V PROJECT V V V V V V V V V V V V V	2	
3	(b)	(i)	80mA + 5mA = 85mA	1	Answer – 1
	()	(7			
3	(b)	(ii)	12V - 5.1 V = 6.9V	1	Calculation and answer – 1
		-			
3	(b)	(iii)	$R = 6.9V/85mA = 81\Omega$	2	Calculation and answer – 2
	·				
3	(c)	(i)	$P = V^2 / R$ $P = (6.9 \times 6.9) / 75$ $P = 0.64W$ Hence P is approx. 0.6W	2	Calculation and answer – 2
3	(c)	(ii)	I = V/R $I = 6.9 / 75$ $I = 92mA$	2	Calculation and answer –

		D = C + B		1
4	(a)	$E = \bar{A}$	3	1
	. ,	$G = \overline{A + B}$		1

											2 marks for each of
				INPUTS		INTERN		JTPUTS			correct columns D & G
			С	В	Α	D	E	G			1 mark for column E
			0	0	0	0	1	1			
			0	0	1	0	0	0			
			0	1	0	1	1	0	1		
4	(b)		0	1	1	1	0	0	_	5	
			1	0	0	1	1	1			
			1	0	1	1	0	0	_		
			1	1	0	1	1	0			
			1	1	1	1	0	0			

		$Q = (\overline{A}  .  \overline{B} ) +$	(Ā.C)+(Ā.B)		1 mark $(X + \overline{X}) = 1$ reduction
		$Q = \overline{A} (B + \overline{B})$	+ ( Ā . C)		1 mark for (1+ X) =1
		$Q = \overline{A} (1) + (\overline{A})$	. C)		
		$Q = \overline{A}$			
4	(c)	Final gate is a Karnaugh map <b>OR</b>	<b>NOT</b> gate (Accept $\overline{A}$ ) alternative	3	1 mark for final gate
		A.B	$\overline{A} \cdot \mathbf{B} = \overline{A} \cdot \overline{B} = \mathbf{A} \cdot \overline{B}$		
		C 0	······································		1 mark for table with values
		<i>C</i>   <b>O</b>			1 mark for cluster
					1 mark for final gate

5	(a)	(i)	Log graph enables a wide range of values to be displayed on the same axis. Allow – (enables values to be displayed as straight line)	1	
		_	-		
5	(a)	(ii)	7 lux	1	
			$30k\Omega$		

5	(b)	$30k\Omega$	1	
		1 mark for connections correct way round		

5	(c)	(i)	$60 \text{ k}\Omega / (60 \text{k}\Omega + 30 \text{k}\Omega)) \times 12 \text{V} = 8 \text{V}$	2	Working – 1 Answer – 1
---	-----	-----	---	---	---------------------------

5	(c)	(ii)	$R_1$ = 11k $\Omega$ to give same value at Y as switching voltage at X (2:1 ratio) (No ecf on value)	2	Reason / calculation – 1 Answer – 1
			The op-amp is not ideal and will saturate above 0V		Saturation – 1
5	(d)		Need to drop voltage	3	Voltage drop – 1

Acceptable method

Method – 1



				INPUTS			OUTPUTS			
			Tunnel Sensor T	Car Sensor C	Lorry Sensor L	Message Display M	Red Stop light R	Green Go light G		
		(	0	0	0	0	0	1		
6	(a)	(	0	0	1	0	0	1	4	
		(	0	1	0	0	0	1		
		(	0	1	1	1	1	0		
		-	1	0	0	0	1	0		
			1	0	1	0	1	0		
			1	1	0	0	1	0		
			1	1	1	1	1	0		

		R = T +(C.L)		1 mark for terms
				1 mark for OR
6	(b)		2	
		Or for full expression $S - T + \overline{T} C I$		
				Max 1 mark



