## AQA

# A-LEVEL ELECTRONICS 

Programmable Control Systems ELEC4
Mark scheme

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Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts: alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

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## COMPONENT NUMBER:

ELEC4
COMPONENT NAME: Programmable Control Systems

| Question | Part | Sub part | Marking Guidance | Mark | Comment |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | (a) |  | Example noisy input signal giving multiple crossing of threshold each period $\checkmark$ leading to more pulses being recorded by the counter | 2 |  |
| 1 | (b) |  | Schmitt trigger has two switching levels <br> Example so signal must go above upper when going positive/below lower going negative OR relevant valid representation on diagram $\checkmark$ so preventing the multiple pulses occurring as the signal crosses the OV point $\checkmark$ | 3 |  |
| 1 | (c) | (i) | input to op-amp inverting input <br> feedback resistor to non-inverting input $\checkmark$ <br> remainder of the circuit all functionally correct AND input and output labelled | 3 |  |
| 1 | (c) |  | an appropriate calculation feedback resistor larger than other resistor all resistor values $1 \mathrm{k}-1 \mathrm{M} \Omega$ <br> resistors in the ratio 2:1 $\checkmark$ | 4 |  |
| 2 | (a) | (i) | $16 \mu s \checkmark$ | 1 |  |
| 2 | (a) | (ii) | MOVW 0x0F MOVWR PRE | 2 |  |


| 2 | (b) | (i) | $\begin{aligned} & 4 \mathrm{~ms} / 16 \mu \mathrm{~s}=250 \checkmark \\ & 0 \times F A \checkmark \end{aligned}$ |  | 2 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | (b) | (ii) | MOVRW SR $\checkmark$ ANDW $0 \times 02$ |  | 2 |  |
| 2 | (c) | (i) | $250 \pm 1$ loops to give 1s $\checkmark$ |  | 1 |  |
| 2 | (c) | (ii) | MOVW 0xFA MOVWR 0xB0 |  | 1 |  |
| 2 | (c) | (iii) | ```loop1: CALL TIME1 // initiate/call the 4ms subroutine loop2: MOVRW SR ANDW 0x02 JPZ loop2 // check whether the 4ms delay has finished. DEC 0xB0 MOVRW 0xB0 JPZ end // decrement 0xB0 and check for zero JMP loop1 // return to loop1 and repeat } end:``` | loop1: <br> CALL TIME1 <br> // initiate/call the 4 ms subroutine <br> DEC 0xB0 <br> MOVRW 0xB0 <br> JPZ end <br> // decrement 0xB0 and check for zero <br> JMP Ioop 1 <br> // return to loop1 and repeat end: | 3 | First answer includes checking for the 4 ms subroutine to end. <br> Both are only examples examiners will have to check answers carefully and award marks for the three basic steps - as shown by the comments. |
| 3 | (a) |  | closed $\checkmark$ there is (negative) feedback $\checkmark$ |  | 2 |  |



| 4 | (d) | (ii) | Example. mean voltage (8.7V), justified voltage used $\checkmark$ sensible calculation <br> 237W $\checkmark$ <br> (More accurate answer is 214 W ) | 3 | Example if mean power calculated rather than voltage,then 282W. |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5 | (a) |  | voltage divider calculation $2.5=(12.6 \times 10) /(10+\mathrm{R}) \checkmark$ $40.4 \mathrm{k} \Omega \checkmark$ | 2 |  |
| 5 | (b) |  | Example <br> When capacitor voltage less than 4.7 V , voltage divider of 13 k and 15 k give a voltage of less than 2.5 V at $\mathrm{D}_{1} \checkmark$ microcontroller can detect this as logic $0 \checkmark$ | 2 |  |
| 5 | (c) |  | appropriate flow chart with marks for the following key points correct symbols <br> read $D_{0}$ until $D_{0}=1$ (loop) $\checkmark$ <br> turn motor on <br> read $D_{1} \checkmark$ <br> read $D_{1}$ until $D_{1}=0$ (loop) $\checkmark$ <br> return loop with motor turned off $\checkmark$ | 6 |  |
| 6 | (a) |  | Example <br> ADC-convert analogue signal from the PC to digital signal for transmission $\checkmark$ DAC convert received digital signal to analogue signal for the hi-fi $\checkmark$ | 2 |  |
| 6 | (b) |  | lower resolution $\checkmark$ fewer conversion levels $\checkmark$ less dynamic range $\checkmark$ etc | 2 max |  |


| 6 | (c) |  | calculation $1 / 44000=\checkmark$ $22.7 \mu \mathrm{~s} \checkmark$ | 2 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 6 | (d) | (i) | invert the output from op-amp A $\checkmark$ provide unity gain | 2 |  |
| 6 | (d) | (ii) | $0 \times 80$ gives $D_{7} 5 \mathrm{~V} \checkmark$ <br> Example of calculation of summing amplifier leading to $\checkmark$ $10 k \Omega \checkmark$ | 2 max |  |
| 6 | (e) |  | Input value steadily increases, so output voltage steadily increases until count reaches 0xFF $\checkmark$ whereupon it starts again from 0 | 2 |  |
| 7 | (a) |  | calculation e.g. 3 LEDs each with 2 bits giving 6 bits $2^{6}=64 \checkmark$ <br> Accept 63 - when all of the LEDs are off - not a colour | 2 |  |
| 7 | (b) | (i) | only on for $33 \%$ of time so LED perceived as only being $1 / 3$ as bright or similar $\checkmark$ | 2 |  |
| 7 | (b) | (ii) | human eye persistence of vision $>50 \mathrm{~ms} \checkmark$ flash rate $\approx 3 \mathrm{~ms}$ | 2 |  |
| 7 | (c) | (i) | input bits are $00011011 \checkmark$ $0 \times 1 \mathrm{~B} \checkmark$ | 2 |  |
| 7 | (c) | (ii) | red on continuously, green on for $2 / 3$ duty cycle and blue on for $1 / 3$ duty cycle red plus one other correct third colour correct $\checkmark$ | 2 |  |

