
A-LEVEL ELECTRONICS

Further Electronics ELEC2
Mark scheme

2430
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Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts: alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

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COMPONENT NUMBER: ELEC2
COMPONENT NAME: Further Electronics

Question	Part	Sub part	Marking Guidance	Mark	Comments
1	(a)		correct substitution into voltage gain formula ✓ gain = 100 ✓	2	Award 2 marks for correct answer
1	(b)		a correctly wired amplifier, inverting or non inverting ✓ non-inverting amplifier ✓ resistor ratios to give Gv of 100 ✓ all resistors between 1k and 4M7 ✓	4	
1	(c)	(i)	Example Voltage gain x bandwidth is a constant ✓ Or Large gain = small bandwidth ✓	1	
1	(c)	(ii)	voltage gain × frequency = 10^6 => gain at 40kHz is 25 ✓ 25 x 40mV = 1V ✓	2	
1	(c)	(iii)	Example Set up two amplifiers each with a voltage gain of 10 ✓ and cascade them ✓ Or Add an amplifier to the output ✓ with a gain of 4 ✓	2	
2	(a)		exponential charging curve through 0V ✓ (not quite) touching V_s ✓	2	

2	(b)	time = 0.69RC = 0.69 × 6200 × 0.0068 ✓ 29.1s ✓ Accept 29	2	
2	(c)	statement of suitable time (example) 1 hour (3600s) ✓ => R = 3600 / (0.69 × 0.0068) R = 767kΩ ✓ Accept the correct R – 6.2 Accept 1MΩ (as 767 resistors don't exist!)	2	
2	(d)	leakage current ✓ comment on charging current close to leakage current ✓ so that Vs/2 is never reached ✓	3	
2	(e)	gate 1 output goes low ✓ diode conducts discharging capacitor through 1kΩ resistor ✓	2	
3	(a)	discharge to junction of R _A and R _B ✓ trigger linked to threshold ✓ threshold to junction of R _B and C ✓	3	
3	(b)	graph between 4 and 8V ✓ charging curve when output goes high ✓ discharging curve when output goes low ✓	3	
3	(c)	substitution into correct 555 frequency formula ✓ correct rearrangement ✓ Calculated value of 35.5kΩ ✓	3	

3	(d)		substitution into correct 555 frequency formula and correct rearrangement ✓ calculated value = approx. 680K ✓	2	
4	(a)	(i)	Biases the MOSFETs ✓	1	
4	(a)	(ii)	Provides power gain ✓	1	
4	(b)	(i)	substitution into a gain formula ✓ correct value = 40kΩ ✓	2	
4	(b)	(ii)	Example Overall voltage gain of the amplifier includes the voltage gain of the source followers ✓ Voltage gain of source followers < 1 ✓	2	
4	(c)	(i)	The op-amp does not saturate at the supply voltages ✓	1	
4	(c)	(ii)	power output formula ✓ substitution $P = (7^2/2 \times 4)$ ✓ $P = 6.125W$ ✓	3	
4	(c)	(iii)	Increase power supply voltages ✓	1	
5	(a)		all Rs to 0V ✓ all flip-flops D connected to Qbar ✓ Q to following flip-flop CK ✓ input to first CK ✓	4	

5	(b)	summing amplifier formula and attempt at substitution ✓ correct substitution ✓ output voltage = -6.875V ✓	3	
5	(c)	correct down counter shape ramp ✓ correct polarity –ve, which returns to 0V every 16 clock pulses ✓ correct amplitude (9.375V) ✓ evidence of steps in ramp ✓	4	
6	(a)	on the rising edge of the clock pulse ✓ the value of D is transferred to Q ✓ some correct mention of S and/or R ✓ some correct mention of \overline{Q} ✓	3 max	
6	(b)	first data input labelled as serial data input and label of clock input correct ✓ all clock inputs connected together ✓ Q connected to following D ✓ Resets not left floating ✓	4	
6	(c)	Example 4-input NOR gate or equivalent ✓ output to serial data input ✓ inputs from all Qs or all \overline{Q} s ✓	3	
6	(d)	Q _A goes high on rising edge of first clock pulse for one clock pulse ✓ repeats only on 6 th clock pulse ✓	2	