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General Certificate of Education (A-level)
June 2013

Electronics ELEC1

(Specification 2430)

Unit 1: Introductory Electronics

Final

Mark Scheme

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all examiners participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for standardisation each examiner analyses a number of students' scripts: alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, examiners encounter unusual answers which have not been raised they are required to refer these to the Principal Examiner.

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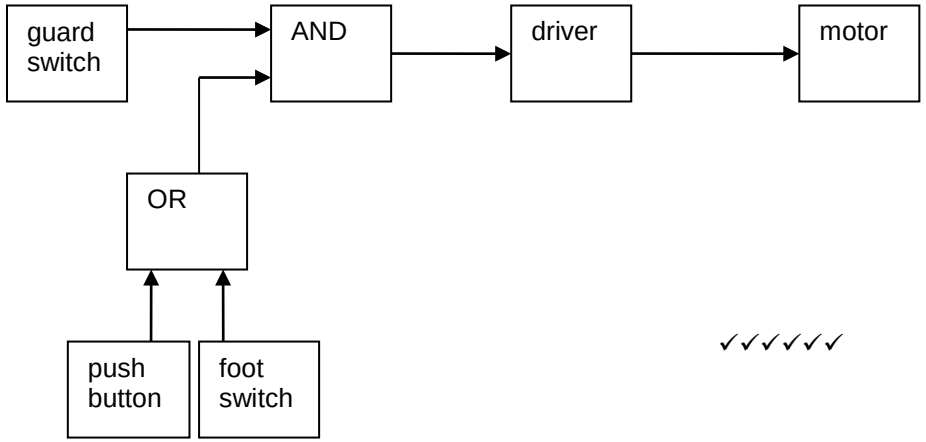
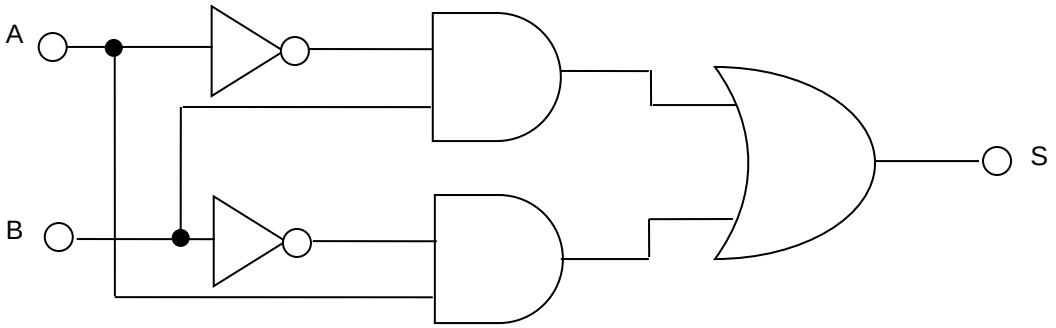
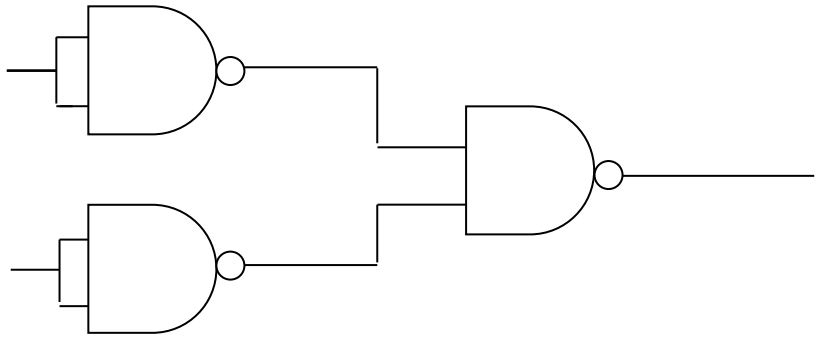
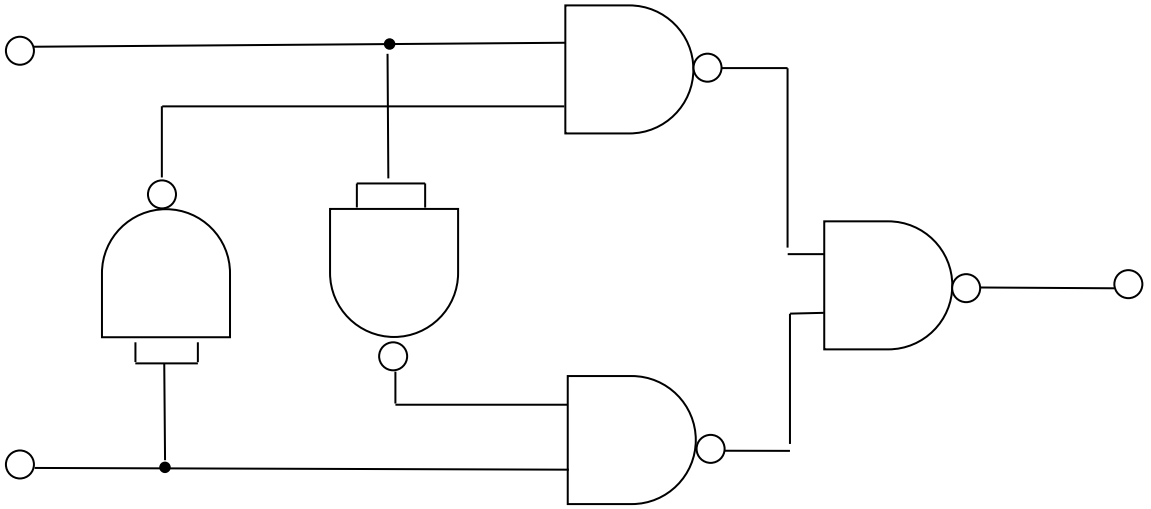
Question	Part	Sub	Marking guidance		Mark
1	(a)		Example only:  ✓✓✓✓✓✓		**6**
1	(b)	(i)	V = I x R, 5 x 0.1✓ = 0.5V✓		**2**
1	(b)	(ii)	Comparator, Schmitt trigger (gate or circuit) ✓		**1**
1	(b)	(iii)	op-amp✓		**1**
2	(a)		$\overline{A}$✓ $\overline{B.C}$✓✓		**3**
2	(b)		$\overline{D + E}$✓✓		**2**

2	(c)		<table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td></td><td></td><td></td><td>✓</td><td>✓</td><td>✓✓</td></tr></table>		**4**
2	(d)		(3-input) AND gate✓		**1**
3	(a)		LED only lights one way / damage if reversed ✓		**1**
3	(b)		Protect LED / from excess current / drop voltage ✓		**1**
3	(c)	(i)	9 – 2✓ – 0.7 = 6.3V ✓		**2**
3	(c)	(ii)	V/I = 6.3/0.02✓ = 315Ω✓ (ecf)		**2**
3	(c)	(iii)	330Ω (ecf) ✓ and reason ✓		**2**
3	(d)		increase value of R_1 ✓		**1**
3	(e)		protect LED against reverse voltage ✓ diodes do not allow reverse bias to respective LEDS✓ Battery voltage > reverse voltage for LED ✓ (Max 2)		**2**
4	(a)	(i)	Top: non-inverting input✓ Bottom: inverting input✓		**2**
4	(a)	(ii)	when V+ > V–, output goes high ✓ when V+< V–, output goes low ✓		**2**

4	(b)	(i)	5V across 30k + 10k + 10k = 50k (or similar calc) ✓ 70k needed✓		**2**
4	(b)	(ii)	calc leading to✓≥ 9V✓		**2**
4	(c)		V_{-sat} output from op-amp is higher✓ than Vf for red LEDs✓ Vf for blue LEDs higher ✓ (Max 2)		**2**
5	(a)		10mA + 88mA = 98mA✓; V across resistor = 4.4-2.7 = 1.7V✓; R=1.7/0.098 ✓= 17.3Ω✓		**4**
5	(b)		98mA✓		**1**
5	(c)		P = I.V = 0.098 x 2.7✓ = 0.265W✓; use 0.5W✓		**3**
5	(d)		Voltage across R will increase✓, so current through R will increase. ✓ current through zener will increase ✓		**3**
6	(a)		$S=\overline{A}.B + A.\overline{B}$ (allow A ⊕ B)✓✓ C=A.B✓		**3**

6	(b)		 one mark per correctly connected correct gate ✓✓✓✓✓		**5**

6	(c)		 Use of Boolean Algebra, Karnaugh Map, or annotated logic diagram and truth table✓✓✓		**3**

6	(d)		 A bar and B bar generated✓, correctly combined signals in two NAND gates✓, OR gate implemented, 5 gates with redundant gates removed✓		**3**

6	(e)		So that no gates are wasted/only one type of IC is needed/NAND gates are cheaper/less board space ✓		**1**