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General Certificate of Education (A-level)
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Electronics ELEC4

(Specification 2430)

Unit 4: Programmable Control Systems

Final

Mark Scheme

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Question	Part	Subpart	Marking guidance		Mark
1	(a)		Period of rotation 8.3ms ✓, sensible ecf..... =>7200rpm ✓		**2**
1	(b)		Noisy signal ✓, not at appropriate logic levels **OR** analogue signal **OR** it needs to be digital signal ✓		**2**
1	(c)	(i)	Rs in parallel 6.7kΩ ✓, voltage divider ✓, 3V ✓		**3**
1	(c)	(ii)	ecf for common error ..... calculation ✓, 2V ✓		**2**
1	(d)		Output between 0 and 5V (allow 5.3V) (allow up to 1 and down to 4V)✓, Inverted ✓, **All** vertical sides at appropriate levels (ecf from (c) above) ✓		**3**
2	(a)		Label a virtual earth point with the letter X		**1**
2	(b)		In total darkness $I_d = 0$ ✓, (so no current passes through the feedback resistor ✓) $V_{out} = I_d \times 10^6 = 0$✓		**2**
2	(c)		I_d = current through 1M resistor ✓, $V_{out} = I_d.1M$ ✓, $V_{out} = 0.1L$ ✓		**3**
2	(d)		Correct symbols ✓, read in values of the two diodes ✓, compare the two values ✓, adjust the position of the focussing motor ✓, read in values and compare difference with **previous** value ✓, adjust to **maximum** difference ✓, etc		**5 Max**

3	(a)		**Just 'Battery' = 0** 1 appropriate source (Pb acid, Li, NiMh, large capacitor) ✓, relevant advantage ✓ a second appropriate source, ✓ different relevant advantage ✓		**4**
3	(b)	(i)	many simple processors ✓		**1**
3	(b)	(ii)	memory distributed between the synapses (nodes) ✓		**1**
3	(b)	(iii)	neural networks trained not programmed ✓		**1**
3	(b)	(iv)	sensible advantage, i.e. it can learn about its environment and adjust what it does ✓		**1**
3	(c)		4 MOSFETs, recognisable symbols ✓, p&n MOSFETs correct in one arm ✓, correct in two arms ✓, motor between the two arms ✓		**4**
4	(a)		calculation ✓, sensible ecf..... 65536 ✓		**2**
4	(b)		MOVW 0x00 ✓, MOVWR TRISA ✓, MOVWR TRISB ✓, MOVW 0xFF ✓, MOVWR TRISC ✓		**5**
4	(c)	(i)	**Labels & Connections** Data into Ds ✓, outputs from Qs ✓, clocks connected to form **latch select** ✓		**3**
4	(c)	(ii)	Data set up on D inputs ✓, clocks pulsed (high) ✓		**2**

5	(a)		Analogue signal E.g. RAM stores (binary) digital values ✓, and so only two values ✓		**2**
5	(b)	(i)	**Imply Compare** flash much faster than ramp ✓		**1**
5	(b)	(ii)	**Imply Compare** flash more complex than ramp ✓		**1**
5	(b)	(iii)	**Imply Compare** Flash expensive, ramp cheaper ✓		**1**
5	(c)		Bit B_3✓, Bit 3 is set as an input by the code ✓		**2**
5	(d)	(i)	Taking the input to logic 0 starts the process ✓ (Accept 'low' if in context)		**1**
5	(d)	(ii)	ANDing with FD makes $B_1 = 0$ ✓, then ORing with 02 makes it 1 again ✓		**2**
5	(e)		continuously check (monitored) the value of the input ✓		**1**
6	(a)	(i)	Any sensible response ✓ e.g. accuracy of rotation (not resolution)		**1**
6	(a)	(ii)	Any sensible response ✓ e.g. less complex to implement, cheaper, more efficient, more torque		**1**
6	(b)	(i)	closed system ✓, because there is feedback to the controller ✓		**2**
6	(b)	(ii)	2^4 = 16 discrete positions ✓, Sensible ecf …… 360/16 = 22.5° ✓		**2**
6	(c)	(i)	sensors/bands are not all aligned ✓, so some bits change at different times to others ✓, leading to errors ✓		**3**

6	(c)	(ii)	Only one bit changes at a time ✓, so sensors do not have to be so accurately aligned ✓		**2**
7	(a)	(i)	**Compare No comparison = 0** **ONE MARK** LED higher power consumption than LCD ✓, **OR** LED consumes power when segment is lit ✓, LCD only consumes power when switching state ✓		**2**
7	(a)	(ii)	**Compare No comparison = 0** **ONE MARK** LED visible in the dark but LCD is not unless back lit ✓, **OR** LED easily visible in poor light but not in good light ✓, LCD, the other way round ✓		**2**
7	(a)	(iii)	**Compare No comparison = 0** LED, very limited ✓, LCD, any character (can be put onto the screen at manufacture) ✓		**2**
7	(b)		two AND gate outputs to OR gate ✓ NOT gate inverting control signal ✓ Sensible ecf from NOT gate in wrong place correct wiring to AND gate inputs ✓		**3**
7	(c)		Correct reduced solution ✓ ✓ **OR** conversion of OR gate to NAND ✓ Conversion of AND gates to NAND ✓		**2**