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General Certificate of Education (A-level)
June 2012

Electronics ELEC2

(Specification 2430)

Unit 2: Further Electronics

Final

Mark Scheme

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all examiners participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for standardisation each examiner analyses a number of students' scripts: alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, examiners encounter unusual answers which have not been raised they are required to refer these to the Principal Examiner.

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Question	Part	Subpart	Marking guidance		Mark
1	(a)		<table><tr><th>Q</th><th>$\overline{\mathbf{Q}}$</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td></tr></table> ✓ for each line		**4**
1	(b)		D input ✓, CK input ✓, CKs joined ✓, D to previous Q ✓		**4**
1	(c)		Changes occur on the rising edge of the clock pulse ✓, pulses moving along the shift register ✓, repeated after four pulses ✓		**3**
2	(a)	(i)	Correct formula ✓, substitution ✓, calculation, 50 ✓,		**3**
2	(a)	(ii)	Correct circuit (non-inverting) ✓, Variable element in a correct place ✓, Appropriate values (1kΩ - 10MΩ) (gain of 10 to ≈100) (must work as an amplifier) ✓		**3**
2	(b)	(i)	Correct circuit (summing amp) ✓, Appropriate resistor values (1kΩ - 10MΩ) ✓, Appropriate gain (0.1 - 3) ✓		**3**
2	(b)	(ii)	Signals out of phase, inverted ✓, so when added they cancel ✓		**2**

3	(a)		Must be at least 2 NAND gates ✓, or no marks. correct output ✓, cross coupled ✓, inputs correct ✓		**4**
3	(b)		Invert the input, NOT the input etc ✓		**1**
3	(c)		Formula ✓, ecf ..... substitution ✓, 2200(s) ✓		**3**
3	(d)		Formula ✓, ecf ..... Substitution ✓, 1518 - 1540(s) ✓		**3**
3	(e)		Definite switching levels so definite on/off ✓		**1**
4	(a)	(i)	0.6< ✓ <1 100% feedback, source voltage less than gate voltage, etc ✓ for one valid justification – (a)(i) – (a)(iii)		**1**
4	(a)	(ii)	10^6< ✓ <10^9 (very large) Voltage driven device, very large current gain, etc ✓ for one valid justification – (a)(i) – (a)(iii)		**1**
4	(a)	(iii)	10^6< ✓ <10^9 Ω (very large) no physical connection between gate and channel, field effect, etc ✓ for one valid justification – (a)(i) – (a)(iii)		**2**
4	(b)		Reduce cross over distortion, bias MOSFETs into conduction, etc ✓		**1**
4	(c)	(i)	formula ✓ ecf ..... gain of op-amp is 11 ✓,		**2**
4	(c)	(ii)	(x2 because it is a bridge amplifier) 22 ✓,		**1**

4	(d)		peak voltage =30V ✓, ecf..... $V^2/2R$ ✓ ecf..... 112.5W ✓, (15V, 28W) (56W)		**3**
5	(a)		$+V_s$ to supply ✓ Reset to supply ✓ Discharge to R_A/R_B junction ✓ Trigger to R_B/C junction ✓ Threshold to R_B/C junction ✓ (Ignore control connections)		**5**
5	(b)		Formula ✓, substitution ✓, ecf ..... 480kHz ✓		**3**
5	(c)		frequency increases ✓, (overall) capacitance decreases ✓, relate to formula e.g. f α 1/C ✓,		**3**
6	(a)		D to $\overline{\mathbf{Q}}$ ✓, CK to $\overline{\mathbf{Q}}$ ✓, inputs to NOR gate from $\overline{\mathbf{Q}}$ ✓, clock input ✓, NOR output to Resets ✓, Sets to 0V ✓		**5 Max**
6	(b)		2^3 to 0V ✓, 3 Qs to any inputs ✓, Q_A to 2^0 ✓, any other correct ✓		**4**
6	(c)		Connect Reset of A to 0 ✓ Set of A to the output of the NOR gate ✓		**2**