Version 1.0

General Certificate of Education (A-level)
June 2011

Electronics ELEC2

(Specification 2430)

Unit 2: Further Electronics

Final

Mark Scheme

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Question	Part	Subpart	Marking guidance		Mark	Comment
1	(a)		formula (T=RC)✓, substitution/calculation (6.8s) ✓		**2**	
1	(b)	(i)	formula/substitution (0.69RC) ✓, calculation✓, 4.7s✓		**3**	
1	(b)	(ii)	exponential charging shape ✓, passing approx. through (6V/4.7s or 12V/35s or) 7.6V/6.8s ✓,		**2**	
1	(c)	(i)	adjust time delay (time constant) ✓ for the relay to switch on ✓		**2**	
1	(c)	(ii)	Diode conducts✓, C discharges through diode/R_1 ✓		**2**	
2	(a)		rising edge ✓ of signal at clock ✓ causes signal at D ✓ to be transferred to Q ✓		**4**	
2	(b)		FF2 is the only flip-flop where the D input at logic 1 ✓, (when button 2 is pressed) it produces a clock pulse ✓, so FF2 Q output becomes 1 ✓		**3**	
2	(c)		FF4 D input is now 1 ✓, so Q will become 1 (when button 4 is pressed) ✓		**2**	
2	(d)		(first 2, second 4) ✓ (third 1, fourth 3) ✓		**2**	

3	(a)		R_f from output to inverting input **AND** non inverting input to 0V✓, input resistor (in series with microphone) to inverting input ✓, resistor values 1kΩ<R<4MΩ ✓, ratio of resistors 82 ✓		**4**	
3	(b)		R & C in series ✓, in correct place and correct way round ✓, Threshold connected correct ✓, Discharge connected correct ✓		**4**	
3	(c)		Input connected to Trigger ✓		**1**	
3	(d)		Substitution into correct formula (1.1RC) ✓, C=30μF ✓		**2**	
4	(a)		Two input resistors to the inverting input ✓, feedback resistor to the inverting input from the output ✓, non-inverting input to 0V ✓		**3**	
4	(b)		All resistors the same value ✓, 1kΩ<R<4MΩ ✓		**2**	
4	(c)		Two input resistors, one to each op-amp input ✓, feedback resistor to the inverting input from the output ✓, resistor from non-inverting input to 0V ✓		**3**	
4	(d)		All resistors the same value ✓, 1kΩ<R<4MΩ ✓		**2**	
4	(e)		(L + R) + (L - R) = 2L ✓, (L + R) - (L - R) = 2R ✓		**2**	or equivalent by diagram or description

5	(a)	(i)	1MΩ ✓		**1**	
5	(a)	(ii)	correct formula / substitution ✓, answer 4.9 ✓		**2**	
5	(b)	(i)	Push-pull, or source follower ✓		**1**	
5	(b)	(ii)	Voltage gain of MOSFETs is 0.9 – 1 ✓		**1**	
5	(c)	(i)	signal in phase with input ✓, symmetrical positive and negative ✓, amplitude 9.8V ✓		**3**	
5	(c)	(ii)	flat region between positive and negative ✓, symmetrical positive and negative ✓, consistent voltage less than OP-AMP graph ✓, e.g. 2V		**3**	
6	(a)		outputs of one to inputs of other ✓, free NAND gate inputs to inputs AND outputs to Q and $\overline{Q}$ ✓		**2**	
6	(b)		0 ✓,0 ✓,1 ✓, 0 ✓		**4**	
6	(c)		D to own $\overline{Q}$ all three ✓, CK to previous $\overline{Q}$ last two ✓, Resets connected to AND output ✓, Q_B to AND input ✓, Q_C to AND input ✓		**5**	

UMS conversion calculator: www.aqa.org.uk/umsconversion