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General Certificate of Education

Electronics 1431/2431

ELEC2 Further Electronics

Report on the Examination

2010 examination - June series

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General Comments

This module examination tested the Further Electronics module of the AS Electronics specification as well as the basic knowledge acquired from the Introductory module, ELEC1. It is the second examination of the new specification for ELEC2 following its revision.

The examination reflected the style of the previous papers, with questions being set in the context of real applications where ever possible, so recognising the importance of electronics in the real world.

When constructing the examination, 50% of the marks were based on standard bookwork which should have been readily available to all candidates who had studied the course and undertaken some revision. All sections of the specification were examined and it is expected that this will continue in future years.

This year the papers were marked via an online viewing system and so the presentation and handwriting of candidates was very important. While the presentation and handwriting of some candidates was excellent, a significant number of candidates produced scripts which were problematic for examiners. Candidates communicate with examiners via their handwriting, and all too often their responses were verging on being illegible. Candidates need to be reminded that examiners must be able to read responses if they are to gain any credit. Candidates should also consider crossing out errors with a single line and not producing a scribbled mess over which they attempt to write a modified answer.

All of the marks were gained overall by candidates with no marks being inaccessible. Marks ranged from 0 to 67 with the mean mark being 33. As in previous examinations, candidates gained credit for all responses that contained correct electronics.

Question 1

This question was intended to provide a straight forward introduction to the paper.

For section (a) candidates were required to show how they would connect the four D-type flip-flops to form a shift register. While many candidates were able to do this successfully, a significant number of candidates connected the flip-flops as a counter and therefore did not gain credit for many of the marks on this section. A significant number of candidates also lost marks by not reading the instructions to the question and not showing the data and clock inputs and the four outputs.

Section (b) required candidates to know that data is transferred from one flip-flop to the next on the rising edge of the clock pulse. Unfortunately many candidates had not read the question and so concentrated on explaining how a D-type flip-flop worked rather than the shift register.

Section (c) was more demanding and required candidates to have knowledge of the function of both an XOR gate and the shift register. Many candidates succeeded in producing completely correct responses, while a significant number of others gained many marks after having made a single error in the operation of the XOR gate.

Question 2

This question was also intended to be straightforward and was based on the 555 astable circuit. Sections (a) and (b) presented most candidates with few problems and they scored full marks. Problems that candidates did have were usually as a result of not being able to process powers of 10, not being able to rearrange the formula or more worryingly could not look up correct formula on the data sheet.

Section (c) presented candidates with more of a challenge, in requiring them to connect the sprayer unit between the positive supply and the 555 IC output. A significant number of candidates did not think through the problem and so connected the sprayer between 0V and the 555 IC output. Full credit was given to those candidates who used a NOT gate to enable them to have the sprayer unit connected to 0V.

For section (d), most candidates were unaware that the frequency of the 555 IC astable is not affected by variations in supply voltage. It was pleasing to see some candidates deduce this by saying that since the supply voltage is not in the timing equations then the time period is not affected until the supply voltage falls below the operating voltage for the IC.

Question 3

This question should have provided few difficulties to candidates.

Section (a) part (i) required candidates to connect the D-type flip-flops as a 3-bit counter, which most candidates were able to do successfully. A small minority chose to label the output in reverse, with the Z output being from the flip-flop on the left, presumably as a result of getting confused with the binary number outputs. Part (ii) again provided few problems for most candidates, though there were candidates who chose to gate the X and Z counter outputs together rather than the Y and Z outputs. Presumably this was as a result of the counter being required to have 5 as its maximum value.

Section (b) was well answered by the majority of candidates, though a few had some difficulty in converting 3, 4 and 5 into binary numbers while others struggled to visualise the dice output for 4 and 6.

Question 4

This question tested a new area of the specification and should have been anticipated by candidates. It had been hoped that section (a) would have been straightforward for all candidates – calculating the required voltage gain of the circuit. Unfortunately many candidates confused the input and output voltages and so produced an answer of 0.002 instead of 500.

For section (b), most candidates gained many of the marks for completing the circuit diagram of the difference amplifier. A large number of candidates demonstrated a complete lack of knowledge about the circuit.

The calculation for section (c) caused some candidates difficulties in wondering what values they should take for $(V_+ - V_-)$ instead of realising that this just represents the input voltage. However, many candidates did obtain the correct value for the resistors and so gained full marks.

Answers for section (d) part (i) appeared to be a guess by many candidates with answers ranging from 0Ω to ∞Ω. A significant number of candidates did know the value for the input resistance and so gained full credit. Part (ii) should have been two straightforward marks for candidates, but worryingly, many candidates had no idea of the voltage follower circuit. Those candidates that did often connected the output back to the non-inverting input rather than the inverting one.

Question 5

This was probably the most demanding question of the examination but a significant number of candidates managed to gain many of the marks that were available.

Section (a) part (i) essentially tested if candidates knew the formula for the time taken for a capacitor to fully charge. Unfortunately many candidates did not and chose to use T=RC or even T=1.1RC. A number of candidates also had problems manipulating the powers of ten for the capacitor value.

A significant number of candidates believed, incorrectly, that the op-amp was configured as either a difference amplifier or an inverting amplifier. This section was also characterised by poor arithmetic with 3 x 3.2 = 9.9 and 1 + 2.2 = 3.3 being common errors. Part (iii) was answered much better with many candidates obtaining the correct response, although too many failed to gain credit as a result of confusion with powers of ten. For part (iv), there were many correct answers although many candidates incorrectly believed that the voltage increased or oscillated between ± 12V.

Section (b) was poorly answered with many candidates making no attempt. Of those candidates attempting this section too many responses focussed on the positive gain rather than the input impedance/resistance. Few candidates gained both marks for either comparing it with the inverting amp or for saying that it reduced the rate of decay of the capacitor voltage.

Question 6

This question required candidates to carry out three calculations and then compare their findings with the required specification. Unfortunately many candidates made vague unjustified comments about suitability and so gained little credit.

Section (a) gained many good responses with the only difficulties being for those candidates who used the non-inverting amp formula. However they were then able to make a valid judgement on the suitability of the gain and so gained credit.

Section (b) was more demanding with many candidates either not attempting the question or just making a comment without a calculation. Candidates struggled to remember the formula for the gain bandwidth product for the op-amp and those who did then had difficulty rearranging it. Some candidates also tried to use their knowledge of amplifier bandwidth and so tried to find 70% of the supply voltage as the bandwidth. These problems aside, there were some very good responses by candidates

Section (c) also gained many non-attempts, though there was little to indicate that candidates were short of time. The most common error for those candidates making a serious attempt at this section was using the incorrect formula or not using rms voltage. However, even with these errors many candidates gained two of the three available marks. It was pleasing to see some candidates taking into account the voltage drop across the MOSFETs and the maximum output voltage of the op-amp, when assessing the amplifier's output power.

Mark Ranges and Award of Grades

Grade boundaries and cumulative percentage grades are available on the **Results statistics** page of the AQA Website.