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ASSESSMENT and QUALIFICATIONS ALLIANCE

General Certificate of Education

Electronics 5431/6431

ELE4 Electronic Control Systems

Mark Scheme

2008 examination – June series

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1 (a) The voltage across the resistor is 12 - 4.2 = 7.8V ✓
=> R = 7.8 / 0.045 = 173Ω ✓
=> increase to preferred value is 180Ω ✓

(b) (i) Virtual earth point at inverting input to op-amp ✓

(ii) **Photodiode** between inverting input and negative supply ✓
cathode connected to inverting input of op-amp ✓
anode connected to the negative supply ✓

(c) The current through the feedback resistor will be 5μA ✓
=> the output voltage will be 5μA x 1MΩ = 5V ✓

Total – 9

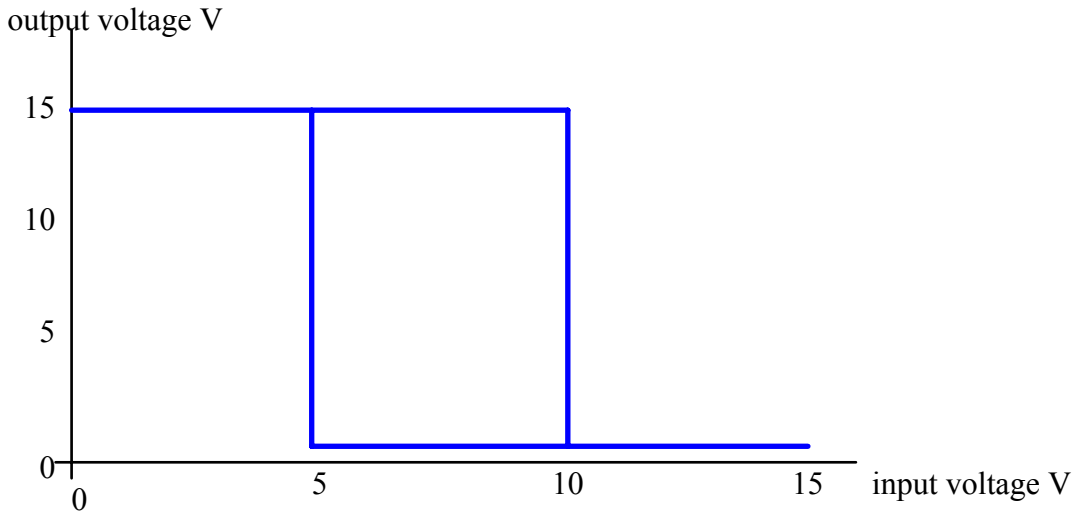
2 (a) (i) Very large open loop voltage gain ✓

(ii) V_{in} must be between 0V and 7.5V ✓

(b) (i) Feedback resistor in parallel with top 47kΩ resistor giving 23.5kΩ ✓
=> voltage at non-inverting input terminal is 10V ✓
=> for output to be at +15V, the input voltage must be less than 10V ✓ (max 2)

(ii) Feedback resistor in parallel with bottom 47kΩ resistor giving 23.5kΩ
=> voltage at non-inverting input terminal is 5V
=> for output to be at 0V, the input voltage must be greater than 5V ✓

(c)



General shape ✓
Correct switching levels ✓

(d) (Capacitor charges and discharges between $^1/_3$ and $^2/_3$ of supply voltage)
(This is the same as the 555 timer)
=> T = 1.4 R C ✓
=> T = 1.4 x 10^4 x 10^{-7} = 1.4ms ✓

Total – 9

3 (a) (i) e.g. Information is stored in the connections between neurons in an ANN whereas it is stored at specific locations in the NAS ✓

(ii) e.g. The NAS is limited by the number of locations at which to store information
The ANN is essentially unlimited since there are so many possible interconnections between neurons ✓

(iii) e.g. The information in a NAS is more reliable than an ANN since connections between neurons are not stable, while that of the magnetic field is (relatively) ✓

(b) (i) e.g. ANN information processed in parallel by many neurons, in a computer it is processed in a few processors serially ✓ ✓

(ii) e.g. ANNs can learn and adapt to maximise traffic flow, whereas PCs cannot. ✓ ✓

(c) e.g. ANNs unsuitable for applications which require precision since they operate essentially through probability (fuzzy logic). ✓ ✓

Total – 9

4 (a) (i) 360 / 16 = 22.5° ✓

(ii) 360 / 16 = 22.5° ✓

(iii) (Add more rings), each with twice as many divisions (bits) as the previous ✓

(b) Absolute position and direction ✓ ✓

(c) e.g. Accuracy of rotation + explanation ✓ ✓
Speed of response + explanation ✓ ✓

Total – 9

5 (a) Closed loop + reason ✓

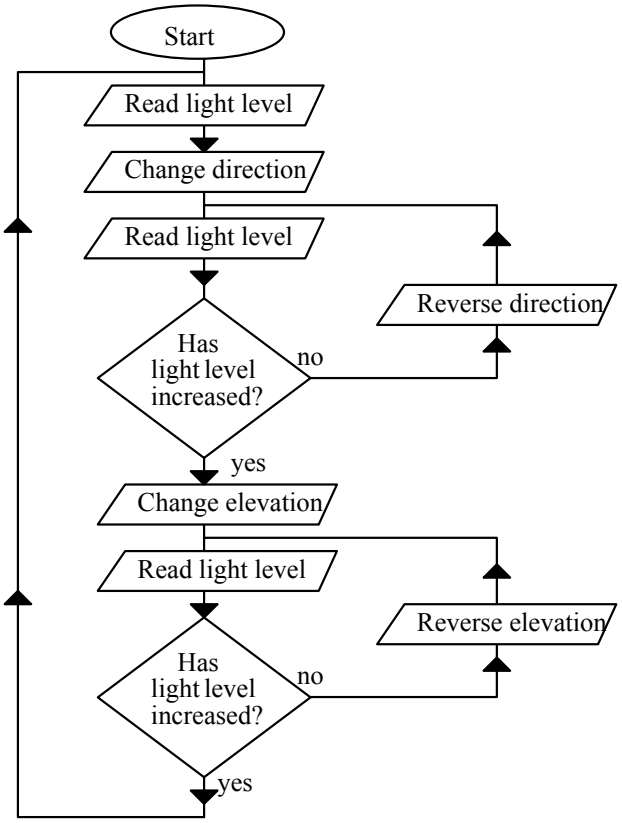
(b) (i) Eliminate reverse voltages generated as the motor coils switch off ✓

(ii)

Input A	Input B	Motor
0	0	Stop – 0
0	1	Rotate in one direction – 1
1	0	Rotate in the other direction – 0
1	1	Stop – 0

First and last row ✓
Middle two rows ✓ ✓

(c) e.g.



Horizontal direction changes ✓
Vertical direction changes ✓
Appropriate elements to flow chart ✓
Largely correct symbols ✓

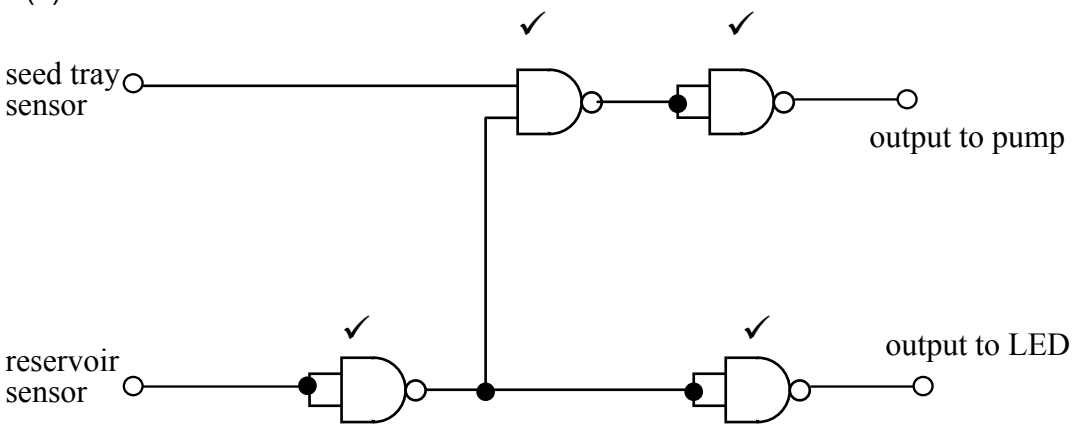
Total – 9

6 (a)

tray sensor	reservoir sensor	pump	LED
wet	wet	0	0
wet	dry	0	1
dry	wet	1	0
dry	dry	0	1

Minus 1 per row. ✓ ✓ ✓

(b)



(c) Very large input resistance – (so it does not load the output of the logic gates) ✓
Very large power gain – (so that a logic gate can readily control the pump) ✓

Total – 9

7 (a) e.g. Computer inputs are digital and only accept two voltage levels ✓ which is not compatible with the wide range of voltages from an analogue sensor ✓

(b) (i) Tristate - three output states - 0, 1 ✓
and high impedance ✓

(ii) The tristate (buffer) outputs are active low ✓
When D_6 is 1, output enable of the most significant nibble tristate buffer is logic 1 and so disabled and the output enable of the least significant nibble tristate buffer is logic 0 and so enabled ✓

(c) 15300 / 255 = 60 ✓
so resolution is 60 lux ✓

(d) SC is taken low to start the conversion. ✓
PC waits until EoC goes high ✓
D_6 high - least significant nibble read ✓
D_6 low - most significant nibble read and added to least significant. ✓

(e) (i) &H379 ✓

(ii) Masks the least significant three bits ✓
to avoid errors from undefined bits ✓

(f) (i) Sets bit D_6 to logic 1 without affecting the other bit values ✓

(ii) It moves the bits in Y% to the right, changes bits on D_4 to D_7 to D_0 to D_3 ✓

(iii) It sets D_6 to logic 0 ✓

Total – 18

Paper Total – 72