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ASSESSMENT and QUALIFICATIONS ALLIANCE

General Certificate of Education

Electronics 5431/6431

ELE2 Further Electronics

Mark Scheme

2008 examination – June series

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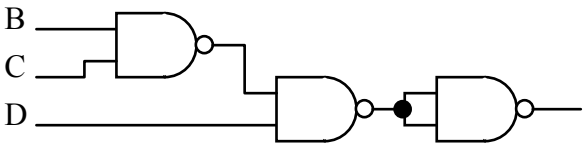
1 (a) E ✓

(b) E.g. There are six occasions when the green light of traffic lights 1 is on and so each of these occasions must be **ORed** together. ✓
For each individual occasion, the logic state of the four counter outputs must be **ANDed** together to give logic 1. This means some of the counter outputs must be inverted. ✓

(c) Karnaugh map or Boolean algebra to give $\mathbf{G = D \cdot \overline{B \cdot C}}$
One mark for each simplification. ✓ ✓ ✓

(d)



✓ ✓ ✓

Total – 9

2 (a) (i) $V = I \times R = 10^7 \times 2 \times 10^{-10}$ ✓
$= 2 \times 10^{-3}V$ ✓

(ii) $G_v = V_{out} / V_{in} = 200 \times 10^{-3} / 2 \times 10^{-3}$ ✓
$= 100$ ✓

(b) Very high impedance (resistance) input ✓
This will not shunt the 10MΩ resistor of the ionisation chamber so lowering the output voltage ✓

(c) (i) Inverting amp connection to junction of 10MΩ resistor and R ✓

(ii) $(Gv = 1 + Rf / R)$
$\Rightarrow 100 = 1 + 10^7 / R$ ✓
$\Rightarrow R = 10^7 / 99 = 101k\Omega$ ✓

Total – 9

3 (a) (i) On the line joining the MOSFET to the transmitter

(ii) (Source) follower (common drain amplifier) ✓

(b) (i) Voltage divider **OR** 12V in the ratio of 1 : 2 ✓
Calculation ✓
=> Voltage at non-inverting input is 8V

(ii) Negative feedback attempts to reduce the difference between the two inputs to zero.
=> In the absence of an input signal both inputs will be at 8V so the output must be at 8V ✓

(iii) Two volts appear across the gate to source of the MOSFET so there will be 6V across the rf amplifier ✓

(c) (i) $G_v = -R_f / R_1 = -470 / 10 = (-)47$ ✓

(ii) If input is 40mV, then op-amp output is 1.88V ✓
Assume G_v of source follower is 1 the voltage change across rf amplifier is also 1.88V ✓

Total – 9

4 (a) Inverting amplifier with a voltage gain of 200 / 10 = 20 ✓
So with a 500mV input the output will be 10V ✓

(b) $P_{rms} = V_p^2 / 2 \times R = 10^2 / 2 \times 8 = 100 / 16$ ✓ = 6.25W ✓

(c) (i) Cross over distortion, when neither of the output transistors conducts at small (input) output voltages ✓

(ii) Diode **biasing** networks to **turn on** the output transistors ✓
Push-pull stage included in the (negative) feedback loop ✓

(d) Large surface area ✓
Dark, matt colour ✓
Good conductor of heat ✓ (max 2)

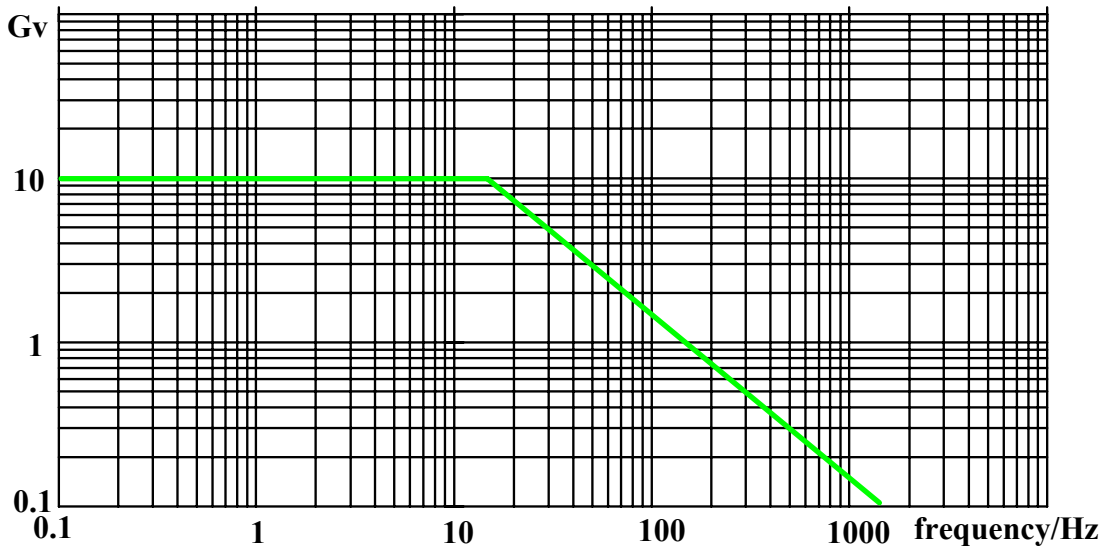
Total – 9

5 (a) (i) Allows low frequencies to pass, ✓
but blocks high frequencies ✓

(ii) The frequency at which the output voltage (gain) is 70% of the maximum output voltage (gain) ✓

(b) $X_c = 1 / 2 \pi f C$ ✓
$X_c = 1 / 2 \times 3.142 \times 20 \times 10^{-7}$ ✓
$X_c = 79.6k\Omega$ ✓

(c)



horizontal line to about 10-20Hz ✓
at a gain of 10 ✓
diagonal line - decreasing (at about 10 per decade) ✓

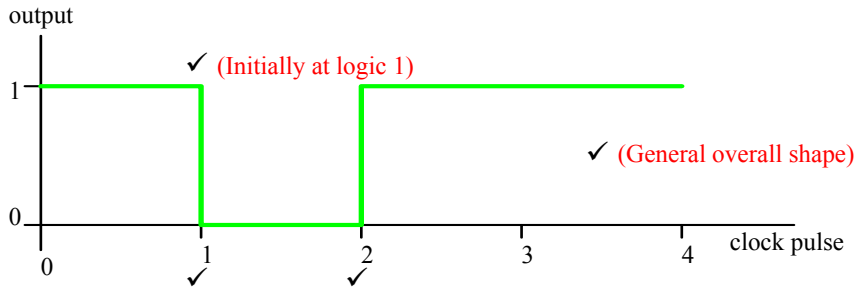
Total – 9

6 (a) For each flip-flop Q becomes D ✓
On the rising edge of the clock pulse ✓
Since D is connected to the previous Q, data is moved along the shift register (on each clock pulse) ✓

(b) (i) Making S logic 0 will not set Q to 0
=> the shift register must be reset before the parallel data is loaded ✓

(ii) Logic 1 ✓

(c)



Total – 9

7 (a) (i) 240 / 60 = 4{Hz} ✓

(ii) (f=1/2RC =>) R = 1 / 2 x 10^{-6} x 4 ✓
= 125kΩ ✓

(b) 30bpm = 0.5bps ✓
=> R = 1 / 2 x 10^{-6} x 0.5 = 1MΩ ✓
(allow 825kΩ if calculated accurately)

(c) (i) T = R x C = 47 x 10^{-9} x 10^{5} ✓
= 47 x 10^{-4}s = 4.7ms ✓

(ii) This starts to charge capacitor C through resistor R and so makes the input of gate Y high. ✓
The output of gate Y goes low, which is fed back to gate X so keeping its output high. ✓
C charges through R until the input voltage to gate Y is below half of the supply voltage. ✓
The output of gate Y goes high, making output of gate X low, circuit resets. ✓
When input of gate X goes low the output of gate X goes high ✓
(X = left gate, Y = middle gate) (max 4)

(d) (i) D to $\overline{Q}$ for each flip-flop ✓
CK of second flip-flop to $\overline{Q}$ of the first flip-flop ✓
Output of monostable to CK of first flip-flop ✓

(ii) LED lights if both Q_A and Q_B are logic 0 ✓

(e) ✓ ✓ ✓ ✓

No of Beats	R_A	R_B
2	0	1
3	$\mathbf{Q_A \bullet Q_B}$	$\mathbf{Q_A \bullet Q_B}$
4	0	0

(Max 3)

Total – 18

Paper Total – 72