ASSESSMENT and
OUALIFICATIONS
ALLIANCE

## General Certificate of Education

## Electronics 5431/6431

## ELE4 Electronic Control Systems

## Mark Scheme <br> 2006 examination - June series

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation meeting attended by all examiners and is the scheme which was used by them in this examination. The standardisation meeting ensures that the mark scheme covers the candidates' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for the standardisation meeting each examiner analyses a number of candidates' scripts: alternative answers not already covered by the mark scheme are discussed at the meeting and legislated for. If, after this meeting, examiners encounter unusual answers which have not been discussed at the meeting they are required to refer these to the Principal Examiner.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of candidates' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

## Unit ELE4 - Electronic Control Systems

1
(a) (i) Binary digit; one binary piece of information
(ii) Data bus - a set of wires connecting together all parts of a computer system and allowing data to flow in both directions along them
(2 marks)
(b) (i) To ensure that the ADC only puts data onto the data bus when the microcontroller is ready to receive it.
(1 mark)
(ii) When microcontroller takes OE low.
(c) (i) Output from humidity sensor is analogue and microcontroller needs digital.
(1 mark)
(ii) Microcontroller takes SC low - so starting conversion process When conversion finished EoC goes high Microcontroller takes OE low and reads data
(3 marks)
(d) readings to 1 in 256 (eight bits) $=>$ resolution $=100 / 256=0.39 \% \checkmark$
(1 mark)
(question total 9 marks)

2 (a) open loop $\checkmark$
since there is no feedback from the direction of the beam of the lamps to the control system $\checkmark$
(2 marks)
(b) (i) Stepper motor - a motor which moves in discrete steps
(1 mark)
(ii) Pulses of current are applied in sequence to the pairs of field coils
(2 marks)
(c) (i) 4-bit optical shaft encoder

(2 marks)
(ii) $360 / 16=22.5^{\circ} \checkmark$
(iii) absolute position OR direction of rotation
(1 mark)
(question total 9 marks)
(a) (i) Integer variable
(ii) mask the lower nibble
(iii) $10100000_{2} \equiv \mathrm{~A} 0_{16} \equiv 160_{10} \checkmark$
(b) Correct Flow Chart symbols expected.

START $\longleftarrow$
Read port \&H379
Mask all bits but $\mathrm{D}_{7}$ Is $\mathrm{D}_{7}=1$ ? no

yes
Output 02 to port \&H378
Read port \& H379 $\longleftarrow$
Mask all bits but $\mathrm{D}_{6}$
Is $\mathrm{D}_{6}=1$ ? no

yes
Output 00 to \&H378
STOP
(6 max)
(question total 9 marks)

4 (a) (i) Neural network many simple processors, PC a few very complex ones
(ii) ANN distributed memory - data stored in connections, PC data stored in dedicated memory
(iii) ANN - taught not programmed, PC follows instructions $\checkmark$
(b) e.g. ANN adjusts its responses
to match available data so that subsequent predictions are more accurate $\checkmark$
(c) (i) comparator $\checkmark$
(1 mark)
(ii) 6 V
(1 mark)
(iii) when 4 or more inputs are at $+V_{s}$
making the voltage on the non-inverting input is greater that that on the inverting input
(2 marks)
(question total 9 marks)

5 (a) Advantages - e.g. seven segment display easier to drive, brighter Disadvantages - e.g. seven segment displays produce limited characters
(b) $\quad \mathrm{R} 2$ positive with respect to $\mathrm{C} 2 \checkmark$
by the forward voltage of the LED
(2 marks)
(c) (i) Top latch stores the row address, bottom latch stores the column address
(ii) When strobe at logic 1, the top latch is written to
(iii) XXX11110, XXX11101, XXX11011, XXX10111, XXX01111
(l mark)
(d) X1111100, X0001010, X0001001, X0001010, X1111100

6 (a) D is transferred to Q on the rising edge of the clock pulse
(b) D must be connected to $\overline{\mathbf{Q}}$
(c) (i) The ratio of the time that the signal is high to the time that the signal is low
(ii) Clock pulse rising edges occur at equal time intervals so the output transitions will be equally timed
(d) connect D to $\overline{\mathbf{Q}}$ for each FF connect together the resets $\checkmark$ connect CK to preceding $\overline{\mathbf{Q}}$ AND together $\mathbf{Q}$ of first and last FF output of AND gate to reset
(max 5)
(question total 9 marks)

7 (a) (i) correct MOSFET symbol correctly connected
(ii) very large input resistance very large current gain $\checkmark$
(b) prevents large induced voltage produced by the relay coil when it is switched off from damaging the semiconductors
(c) $\quad 0 \mathrm{~V}$ and $6 \mathrm{~V} \checkmark \checkmark$
(d) (i) $40^{\circ} \mathrm{C}$
thermistor has resistance of $10 \mathrm{k} \Omega$ at this temperature which will give 6 V at the inverting input terminal.
(ii) Make one of the $10 \mathrm{k} \Omega$ resistors into a variable resistor
(e) When temperature just marginally exceeds $40^{\circ} \mathrm{C}$, then relay will switch off
When temperature marginally falls to just below $40^{\circ} \mathrm{C}$, relay will switch on
(f) (i) Resistor from op-amp output to non-inverting input.
(ii) voltage divider formula Feedback resistor R, when in parallel with 10k must give a value of $9.2 \mathrm{k} \Omega$
Resistors in parallel to give a value for R of $115 \mathrm{k} \Omega$
(iii) Temp. will not be as stable but will fall further below and rise further above the switching temp than it did with a Schmitt trigger.

