

A S S E S S M E N T and Q U A L I F I C A T I O N S A L L I A N C E

## Mark scheme June 2003

## GCE

## Electronics

Unit ELE4

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## ELE4 – Electronic Control Systems

1	(a)	(i)	data in ROM cannot be changed, data in RAM can be $\checkmark$ ROM retains data after power is removed, Ram looses data $\checkmark$ etc.
		(ii)	basic input and output instructions ✓ basic operating system commands ✓ any sensible response
	(b)	(i)	A bus is a collection of wires along which data is sent and received and to which each section of the microcomputer system is connected $\checkmark$
		(ii)	(1 mark) Buses are used to reduce the number of connection routes needed $\checkmark$
		(iii)	To enable data to pass to and from the microprocessor (or RAM etc) $\checkmark$
	(c)	(i)	(1 mark) Memory mapped ports are decoded as memory addresses and accessed as memory elements $\checkmark$
		(ii)	I/O mapping has its own separate control line (or commands) to indicate an address is an I/O port. ✓       (1 mark)         I/O mapping does not take up memory allocation (addresses) ✓       (2 marks)         (Total 9)       (1 mark)
2	(a)	(i) (ii)	a, b, c, d, g $\checkmark$ (1 mark) D <sub>0</sub> , D <sub>1</sub> , D <sub>2</sub> , D <sub>3</sub> and D <sub>6</sub> $\checkmark$ i.e. 01001111 (or 79 <sub>10</sub> ) $\checkmark$
	(b)	(i)	giving 4F ✓ (3 marks) 60mA ✓
		(ii)	5 LEDs => 5 x 1.9 = 9.5V ✓ (1 mark) voltage across R approx. 15 - 9.5 = 5.5V ✓ => R = 5.5 / 0.06 = 91.7Ω ✓
		(iii)	Power = V x I = 5.5 x $0.06 \checkmark$ =>Power = $0.33W$ (accept 0.5 or 1W) $\checkmark$

(2 marks) (Total 9)

(ii) $12.75 \vee / 255 \checkmark$ (1 r $\Rightarrow$ change in output for a change of 1 in the input is $0.05 \vee (50 \text{ mV}) \checkmark$ (2 m (iii) $100 \text{ k}\Omega$ from DAC $0 \vee \circ$ (b) (i) start: is a label $\checkmark$ (2 m (ii) sends the integer variable N% to the output port $378_{16} \checkmark$ (1 r (ii) sends the integer variable N% to the output port $378_{16} \checkmark$ (1 r (c) Enter a number greater than 255 or less than $0 \checkmark \checkmark$ (2 m (Tot 4 (a) (i)	nark) narks) narks) nark) nark) narks) tal 9)
(iii) (iii) (iii) (i) (i) (i) (i)	aarks) narks) nark) nark) arks) t <b>al 9)</b>
(iii) $100k\Omega$ from DAC $0 V \circ$ (b) (i) start: is a label $\checkmark$ (ii) sends the integer variable N% to the output port $378_{16} \checkmark$ (c) Enter a number greater than 255 or less than $0 \checkmark \checkmark$ (2 m (1 m (1 m (2 m (1 m (2 m (1 m))))))))))))))))))))))))))))))))))))	uarks) nark) nark) uarks) t <b>al 9)</b>
(2 m (b) (i) start: is a label $\checkmark$ (ii) sends the integer variable N% to the output port $378_{16} \checkmark$ (c) Enter a number greater than 255 or less than $0 \checkmark \checkmark$ (2 m (1 r (2 m (1 r (2 m (1 r (2 m (1 r (2 m (1 r (2 m (1 r))))))))))))))))))))))))))))))))))))	narks) nark) nark) narks) t <b>al 9)</b>
(i) Sum to is a note that is a not t	mark) nark) Iarks) <b>tal 9)</b>
(ii) $\checkmark$ sends the integer variable 17.6 to the output point 57.6 [6] (1 r (c) Enter a number greater than 255 or less than $0 \checkmark \checkmark$ (2 m (Tot (Tot	nark) Iarks) <b>tal 9)</b>
(c) Enter a name of greater than 200 of 1000 than 0 (2 m (Tot	arks) <b>tal 9)</b>
4 (a) (i) S	
$ \begin{array}{c} D & Q \\ \\ >CK & \overline{Q} \\ \hline R & \checkmark \end{array} $	
(ii) whatever value is put on D is transferred to $Q \checkmark$ only on the rising edge of the clock pulse $\checkmark$	nark)
(2 m (b) (i) three possible output states $\checkmark$	arks)
<ul> <li>0, 1, high impedance ✓ (2 m</li> <li>(ii) to isolate the outputs from the two 4 bit latches ✓</li> </ul>	arks)
(1 m (c) (i) Neural networks have lots of very basic processors whereas a PC has a few complex processors ✓ data is stored through a neural network, whereas a PC stores it centrally	nark) y ✓
<ul> <li>(ii) justified reason e.g. No, because ANNs only predictive and are not able to do accurate measurements ✓</li> <li>(1 r (Tot)</li> </ul>	arks) nark) <b>tal 9)</b>
5 (a) (i) Whole system built in a single IC ✓ PICs have separate instruction bus ✓ (appropriate and sensible response)	
(ii) Sensible answer e.g. cheap and very versatile $\checkmark$ (1 r	nark)

	(b)	Closed loop when system monitors the output and uses state of output to control the input (feedback) $\checkmark$ eg. Filling with water requires the amount of water to be monitored and stopped at the required amount - could not do by time because of variation in water pressure $\checkmark$ Heating could not be done by time because of variation in input water temp $\checkmark$				
	(c)	(i)	$ \begin{array}{c} \max \\ \text{Negative feedback is where information from the output is} \\ \text{used to adjust the input so that the output remains steady } \checkmark \end{array} $	(2 marks)		
		(ii)	If the speed is too fast the input drive to the motor will be reduced and vice versa if the speed is too slow $\checkmark$	(1 mark)		
	(1)			(1 mark)		
	(d)	(1)	thermistor 🗸	(1 mark)		
		(ii)	thermistor is part of a voltage divider circuit which produces a voltage dependent upon the temperature of the thermistor. $\checkmark$ The op-amp compares this voltage with that from the PIC/AVR an produces a low output when the voltage from the voltage divider exceeds that from the PIC/AVR $\checkmark$	d		
				(2 marks) (Total 9)		
6	(a)	To clean up the pulses,( restoring the logic levels and sharp rise and fall times) $\checkmark$				
	(b)	(i)	When the output is at 0V, the voltage divider connected to point A consists of a $47k\Omega$ resistor at the top and two $47k\Omega$ resistors in parallel at the bottom $\checkmark$ Combined resistance at bottom is $23.5k\Omega \checkmark$ Voltage divided into ratio of $2:1 \Rightarrow$ voltage at point A = 4V $\checkmark$	(1 mark)		
		(ii)	When output is 12V, there are two $47k\Omega$ resistors at the top of the voltage divider and one $47k\Omega$ resistor at the bottom $\checkmark$ Combined resistance at top is $23.5k\Omega \checkmark$ Voltage divided into ratio of 1:2 => voltage at point A = 8V $\checkmark$	(3 marks)		
		(iii)	Op-amp has a very large open loop voltage gain so acts as a compa When the input rises above 8V, the inverting input to the op-amp is than the non-inverting input, so the output goes to $0V \checkmark$ Similarly when the input voltage goes below 4V when the output is $12V \checkmark$	(3 marks) arator ✓ s greater s at		
			max	(2 marks) (Total 9)		
7	(a)	MOSFET or transistor with coils in drain/collector circuit. $\checkmark$ Input to gate or base (with series resistor) $\checkmark$ Protection diode for MOSFET/transistor correctly placed $\checkmark$				
	(b)	(i)	A 4 pole stepper motor rotates 7.5° as each successive coil is energised, so with four coils energised in sequence it rotates $30^{\circ} \checkmark$	(3 marks)		
		(ii)	Reverse the sequence $\checkmark$	(1 mark)		
		()	so that $D_3$ is energised first, then $D_2$ , then $D_1$ then finally $D_0 \checkmark$	(2 marks)		
		(iii)	Alter the value of the <b>pause</b> $\checkmark$	(1 mark)		

(c) (i) **OUT(&H378)**, is command to write what follows to the parallel port and 4 corresponds to making the bit  $D_2$  logic 1  $\checkmark$ 

(d)

- (ii) OUT(&H378), 1 GOSUB waitabit OUT(&H378), 2 GOSUB waitabit OUT(&H378), 4 GOSUB waitabit OUT(&H378), 8 STOP  $\checkmark \checkmark \checkmark \checkmark$ (4 marks) (i) Polled is when the computer monitors a port by regularly reading its value  $\checkmark$ 
  - (ii) Interrupt; the computer performs other operations until an external device generates a signal, upon which the computer will stop what it is doing and service the interrupting device. It does not therefore need to continuously monitor the device unlike with polling. ✓
- (iii) Make the motor rotate one step at a time ✓
   (1 mark)
   (iii) Make the motor rotate one step at a time ✓
   Read in the value of port (&H379) and examine bit 5 ✓
   Repeat this until bit 5 is high, tube A is then aligned with the pipe ✓
   (3 marks)

(e) It would be very difficult to make a conventional motor accurately rotate  $30^{\circ} \checkmark$  (1 mark)

(Total 18)

(Paper Total 72 marks)