THIS IS A NEW SPECIFICATION

OCR
RECOGNISING ACHIEVEMENT

ADVANCED SUBSIDIARY GCE

ELECTRONICS

Signal Processors

F612

OCE/13464

Candidates answer on the Question Paper

OCR Supplied Materials:
None

Other Materials Required:
- A scientific calculator may be used

Tuesday 25 May 2010
Afternoon

Duration: 1 hour 30 minutes

F612

Candidate Forename		Candidate Surname	

Centre Number						Candidate Number				

INSTRUCTIONS TO CANDIDATES

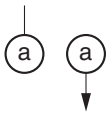
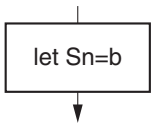
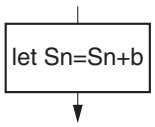
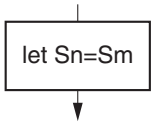
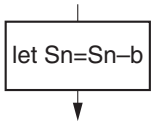
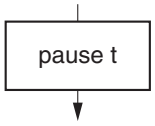
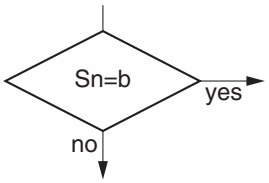
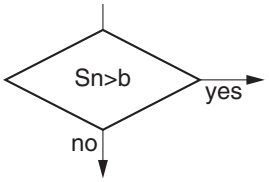
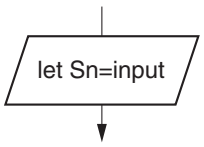
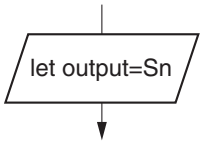
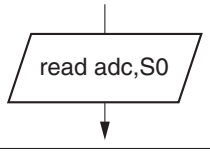
- Write your name clearly in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your Candidate Number, Centre Number and question number(s).

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You will be awarded marks for the quality of written communication where this is indicated in the question.
- You are advised to show all the steps in any calculations.
- This document consists of **16** pages. Any blank pages are indicated.

A scientific calculator may be used for this paper

DC (SHW 00378 12/08) 13464/7

symbol	meaning
	start the program
	link to part of the program with the same label a
	stop the program
	place the byte b in register Sn
	add the byte b to the byte in register Sn
	copy the byte in register Sm into register Sn
	subtract the byte b from the byte in register Sn
	introduce a time delay of t milliseconds
	branch if the byte in register Sn is equal to the byte b
	branch if the byte in register Sn is greater than the byte b
	copy the byte at the input port to register Sn
	copy the byte in register Sn to the output port
	activate the analogue-to-digital converter and store the result in register S0

Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15V and –15V
- logic circuits are run off supply rails at +5V and 0V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$
	$A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$
	$\overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$
	$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$

Answer **all** the questions.

1 Fig. 1.1 shows a microcontroller circuit

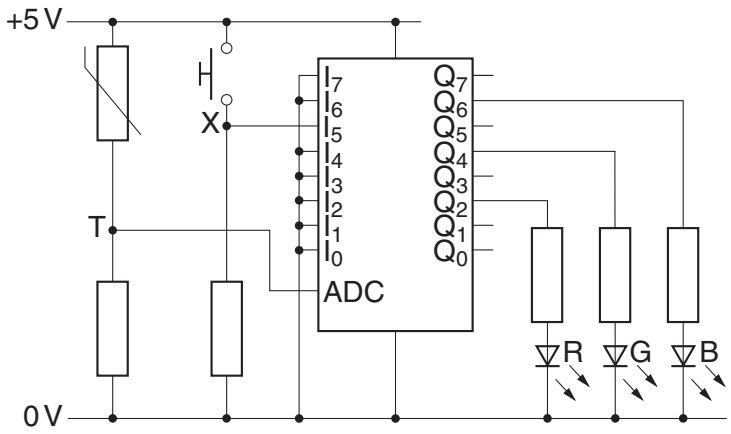


Fig. 1.1

(a) The circuit uses the analogue-to-digital converter (ADC) of the microcontroller. Describe the function of the ADC.

.....

.....

..... **[2]**

(b) The microcontroller could be replaced with op-amps and logic gates.

(i) State **one** advantage of using op-amps and logic gates instead of the microcontroller. Give **one** reason for your answer.

.....

.....

..... **[2]**

(ii) State **two** advantages of using the microcontroller.

.....

.....

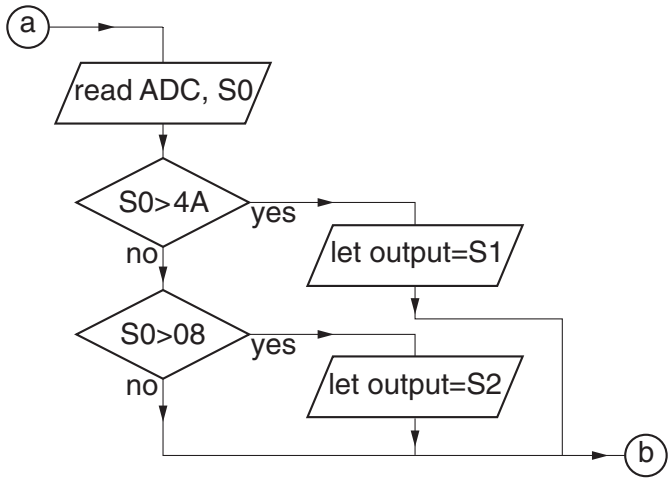
..... **[2]**

(c) Complete the table with R, G or B.

word at output port	LEDs which glow
0000 1111	
D8	

[2]

(d) Here is a flowchart for part of the program in the microcontroller.



Describe the effect that this part of the program has on the output port.

Assume that S1 holds 0F and that S2 holds D8.

.....

.....

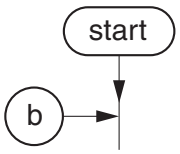
.....

..... **[3]**

(e) The rest of the program has to do the following.

- store 0F in S1, D8 in S2
- place 60 at the output port
- wait until the switch has been pressed, then pass control to **a**

Complete the flowchart in the space below.



[6]

[Total: 17]

2 Fig. 2.1 shows an op-amp circuit.

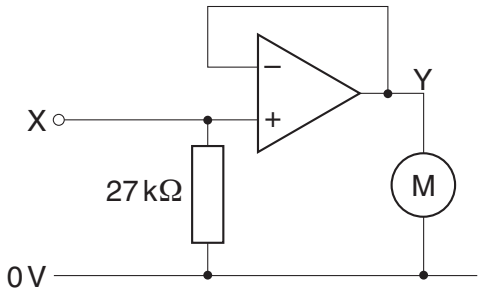


Fig. 2.1

(a) The open-loop gain of the op-amp is 200 000. Explain what this means.

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..... **[3]**

(b) Explain why the voltage gain of the whole circuit is +1.

.....

.....

..... **[2]**

(c) A signal of +5 V is placed at X.

(i) Show that the current in the 27 kΩ resistor is about 0.2 mA.

[2]

(ii) Calculate the power drawn from the source of the signal at X.
State any assumption you have to make.

assumption ..... power = ... W **[2]**

(iii) The motor has an effective resistance of 40 Ω.
By calculating the current in the motor, calculate the power delivered to it by the op-amp.

power = ... W **[3]**

[Total: 12]

3 The circuit of Fig. 3.1 is part of a system which acts as a clock.

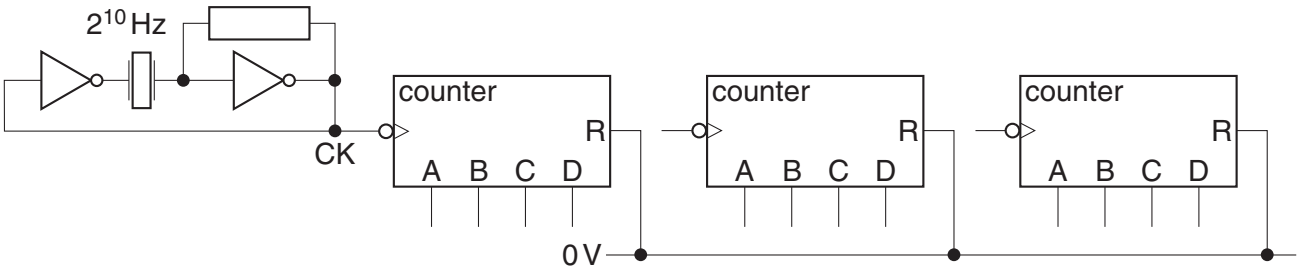

Fig. 3.1

(a) The oscillator contains a crystal which oscillates at a frequency of 2^{10} Hz.
Suggest why a clock uses a crystal oscillator instead of an RC network.

.....

..... **[1]**

(b) The four-bit counters are used to generate a 2 Hz signal from the 2^{10} Hz signal at CK. Draw on Fig. 3.1 to show how this can be done. Label the 2 Hz output. **[2]**

(c) Draw on Fig. 3.2 to show how one of the four-bit counters of Fig. 3.1 can be assembled from D flip-flops and a logic gate. Label all inputs and outputs.

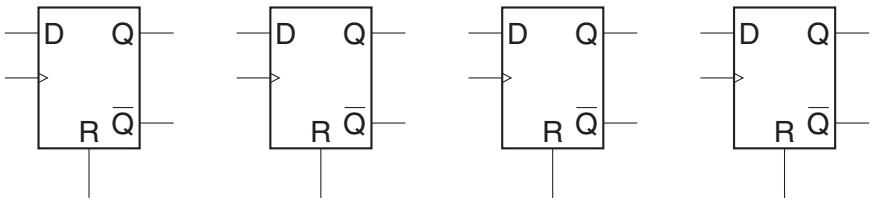

Fig. 3.2

[5]

(d) The clock circuit contains an oscillator and a binary counter. It is required to display the output of the clock circuit in decimal.

State the **two** extra sub-systems required and describe their function.

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..... **[4]**

[Total: 12]

4 Fig. 4.1 is an incomplete block diagram for an audio amplifier.

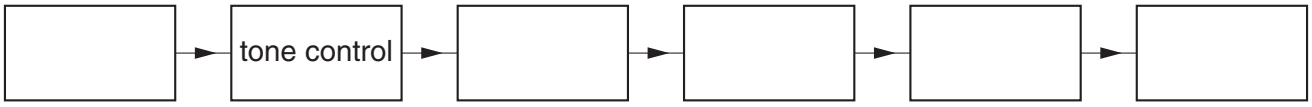


Fig. 4.1

(a) Complete the diagram. Choose from these blocks.

loudspeaker **microphone** **power amplifier** **voltage amplifier** **volume control**

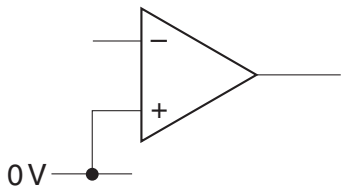
[3]

(b) The tone control is a bass cut filter with the following properties:

- input impedance of 47 kΩ
- high frequency gain of –20
- break frequency of 100 Hz

In the space below, draw a circuit diagram for the filter.

Show all component values and justify them.



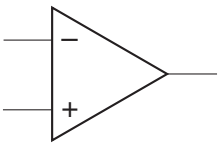
[6]

(c) The voltage amplifier has the following properties.

- voltage gain of +20
- input impedance of 4.7 kΩ

In the space below, draw a circuit diagram for the voltage amplifier.

Show all component values and justify them.



[4]

(d) The volume control can be made from a potentiometer.

Show below how this can be done. Label the input and output.

[3]

[Total: 16]

5 The logic system of Fig. 5.1 behaves like a latch.

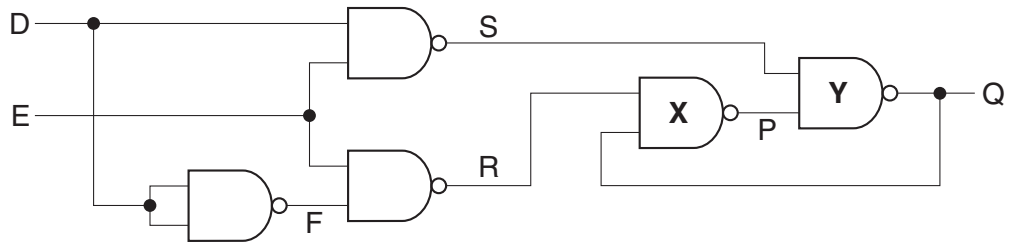


Fig. 5.1

(a) The latch has data (D) and enable (E) inputs and an output Q.

(i) Explain how to reset the output of the latch to logic 0.

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.....

..... **[2]**

(ii) Complete the timing diagram of Fig. 5.2.

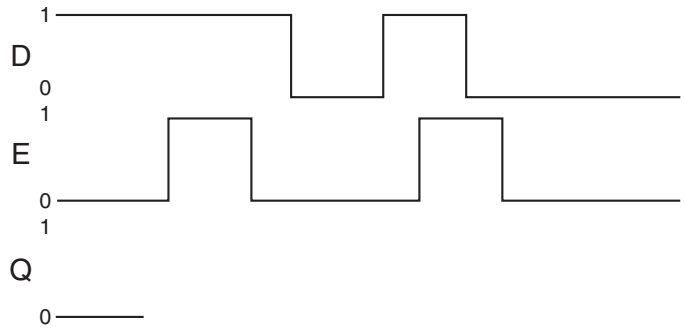

Fig. 5.2

[2]

(b) Complete the truth table for the circuit of Fig. 5.1.

D	E	F	S	R
0	0			
0	1			
1	0			
1	1			

[3]

(c) The logic gates labelled **X** and **Y** in Fig. 5.1 make a bistable.

By describing the behaviour of the logic gates, explain why Q can be either a logic 1 or a logic 0 when both S and R are logic 1.

.....

.....

.....

.....

..... **[3]**

(d) Fig. 5.3 shows how a pair of latches and a NOT gate can be used to make a system which behaves like a rising-edge triggered D flip-flop.

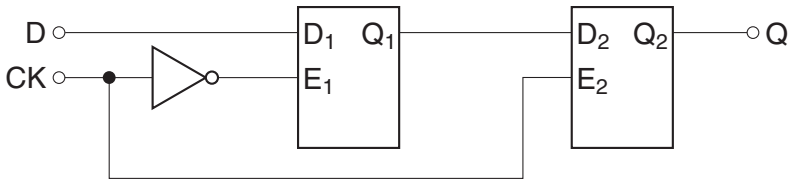

Fig. 5.3

Explain how the system of Fig. 5.3 operates.

Include a description of the behaviour of a D flip-flop.

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..... **[6]**

[Total: 16]

6 The circuit of Fig. 6.1 contains a relaxation oscillator.

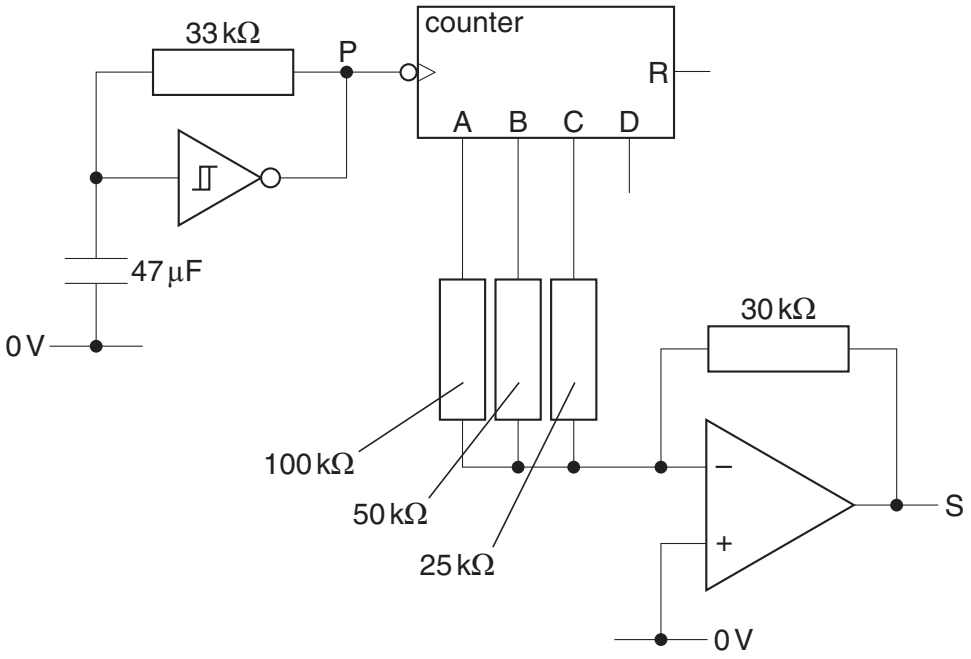

Fig. 6.1

(a) Show that the frequency of the pulses at **P** is about 1 Hz.

[3]

(b) The counter is required to reset DCBA to 0000 each time that five pulses have entered P. Draw on Fig. 6.1 to show how this can be done with a logic gate. **[3]**

(c) At one point in the sequence CBA = 011.

Calculate the voltage at S at this point of the sequence.

voltage = ... V **[2]**

(d) The signal at S is to be processed by an inverting amplifier with a gain of –0.4.

Complete the circuit diagram of Fig. 6.2 to show how this can be done.

Show all component values and justify them.

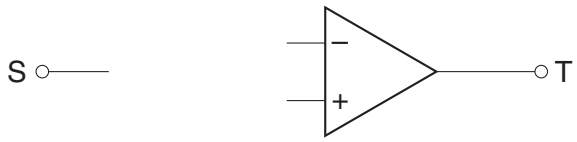

Fig. 6.2

[4]

(e) When the complete circuit operates, the output at T rises from 0V in steps to a maximum value before returning to zero.

Calculate the voltage of the highest step at T.

voltage = ... V **[2]**

[Total: 14]

Quality of Written Communication **[3]**

END OF QUESTION PAPER

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