THIS IS A NEW SPECIFICATION

OCR
RECOGNISING ACHIEVEMENT

ADVANCED GCE
ELECTRONICS
Control Systems

F614

Candidates answer on the Question Paper

OCR Supplied Materials:
None

Other Materials Required:
- Scientific calculator

Tuesday 8 June 2010
Morning

Duration: 1 hour 40 minutes

Candidate Forename		Candidate Surname	

Centre Number						Candidate Number				

INSTRUCTIONS TO CANDIDATES

- Write your name clearly in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your Candidate Number, Centre Number and question number(s).

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **110**.
- You will be awarded marks for the quality of written communication where this is indicated in the question.
- You are advised to show all the steps in any calculations.
- This document consists of **20** pages. Any blank pages are indicated.

A calculator may be used for this paper

Microcontroller instructions

The microcontroller contains eight general purpose registers Sn, where to n = 0, 1, 2 ... 7.
The microcontroller has an eight bit input port, I, an eight bit output port, Q, and an analogue input, ADC.

In the table of assembler instructions given below, Sd is the destination register and Ss the source register.

assembler	**function**
MOVI Sd,n	Copy the byte n into register Sd
MOV Sd,Ss	Copy the byte from Ss to Sd
ADD Sd,Ss	Add the byte in Ss to the byte in Sd and store the result in Sd
SUB Sd,Ss	Subtract the byte in Ss from the byte in Sd and store the result in Sd
AND Sd,Ss	Logical AND the byte in Ss with the byte in Sd and store the result in Sd
EOR Sd,Ss	Logical EOR the byte in Ss with the byte in Sd and store the result in Sd
INC Sd	Add 1 to Sd
DEC Sd	Subtract 1 from Sd
IN Sd,I	Copy the byte at the input port into Sd
OUT Q,Ss	Copy the byte in Ss to the output port
JP e	Jump to label e
JZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC, SHL or SHR was zero
JNZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC SHL or SHR was not zero
RCALL s	Push the program counter onto the stack to store the return address and then jump to label s
RET	Pop the program counter from the stack to return to the place the subroutine was called from
SHL Sd	Shift the byte in Sd one bit left putting a 0 into the lsb
SHR Sd	Shift the byte in Sd one bit right putting a 0 into the msb

There are three subroutines provided:

- readtable – copies the byte in the lookup table pointed at by S7 into S0. The lookup table is labelled table: When S7=0 the first byte from the table is returned in S0
- wait1ms – waits 1ms before returning
- readadc – returns a byte in S0 proportional to the voltage at ADC

Datasheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15V and –15V
- logic circuits are run off supply rails at +5V and 0V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{\text{out}} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_\text{d}}$
inverting amplifier gain	$G = \frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$ $A + \overline{A} = 1$ $A.(B + C) = A.B + A.C$ $\overline{A.B} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}.\overline{B}$ $A + A.B = A$ $A.B. + \overline{A}.C = A.B + \overline{A}.C + B.C$
amplifier gain	$G = -g_\text{m}R_\text{d}$
ramp generator	$\Delta V_{out} = -V_{in}\frac{\Delta t}{RC}$

Answer **all** questions

1 Registers can be used for processing digital information.

(a) Draw the circuit for a six bit register using D-type flip-flops. Label the inputs, the outputs and the clock.

[4]

(b) Write the decimal number 19 in six bit binary.

[2]

(c) The diagram in Fig. 1.1 shows two numbers being added.
Complete the diagram to show the binary number at the output.

Fig. 1.1 **[3]**

(d) The system in Fig. 1.1 can be used for subtracting by making one of the numbers negative. Use two's complement to write decimal –14 in six bit binary. Show all of your working.

[3]

(e) Show how addition can be used to do the decimal calculation 19 – 14 using binary and two's complement. Explain each step in your calculation.

[4]

[Total: 16]

2 The block diagram of a microcontroller is shown in Fig. 2.1. Some of the labels are missing.

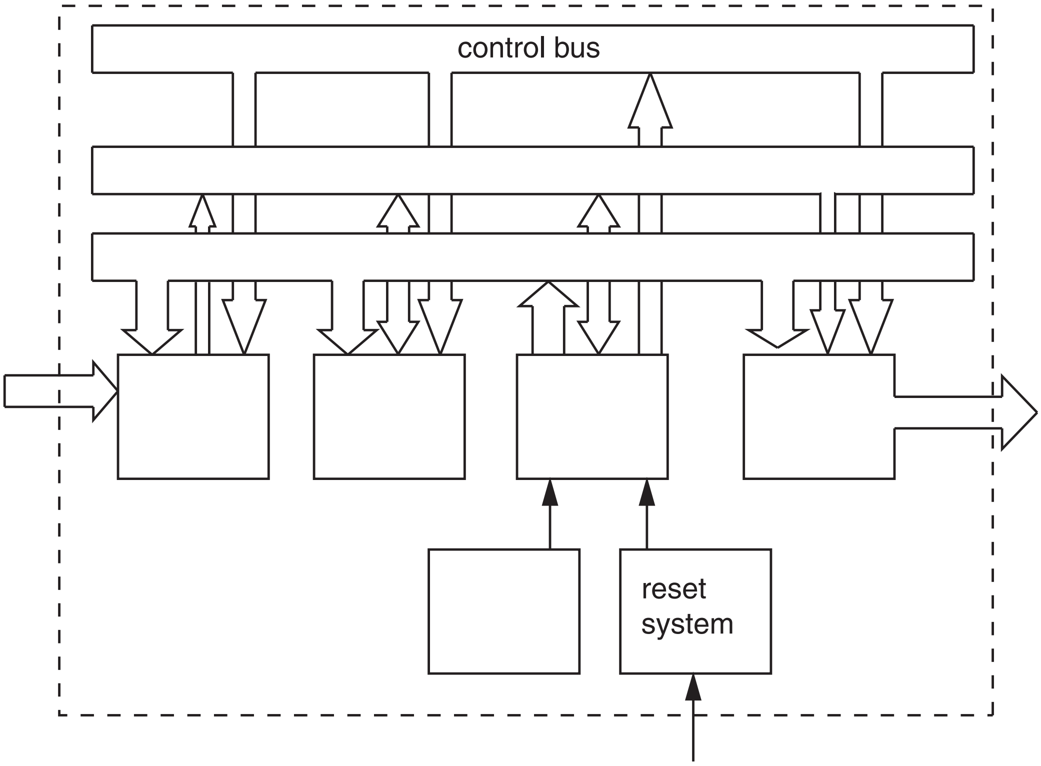

Fig. 2.1

(a) Complete the block diagram in Fig. 2.1 by writing the correct labels in each block and on the busses. Choose from the list below:

address bus **clock** **CPU** **data bus** **input port** **memory** **output port**

[7]

(b) Describe the data bus. Explain what it is used for.

....

....

.... **[3]**

(c) Describe a general purpose register. Explain what it is used for.

....

....

.... **[3]**

(d) Describe what happens in the microcontroller during one machine cycle.

....

....

....

....

....

.... **[5]**

[Total: 18]

3 A power supply circuit is used to charge the battery in an MP3 player.

(a) The circuit in Fig. 3.1 forms part of the power supply.

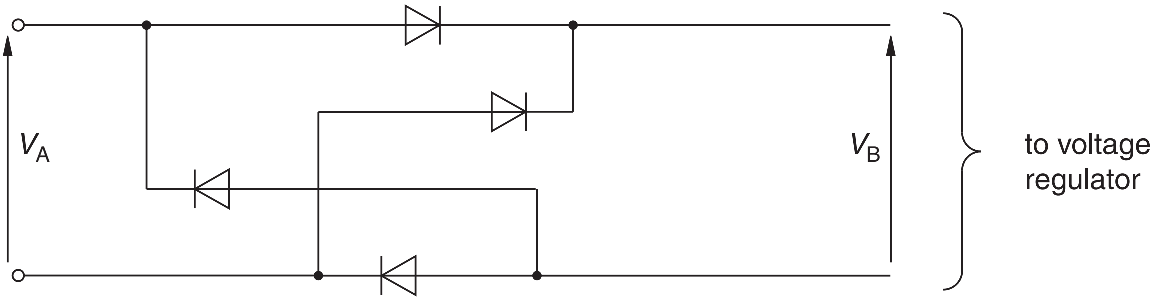

Fig. 3.1

(i) State the name of the part of the circuit shown in Fig. 3.1.

.... **[1]**

(ii) The graph of Fig. 3.2 shows the a.c. input to the power supply.

Draw on Fig. 3.2 to show how V_B changes with time.

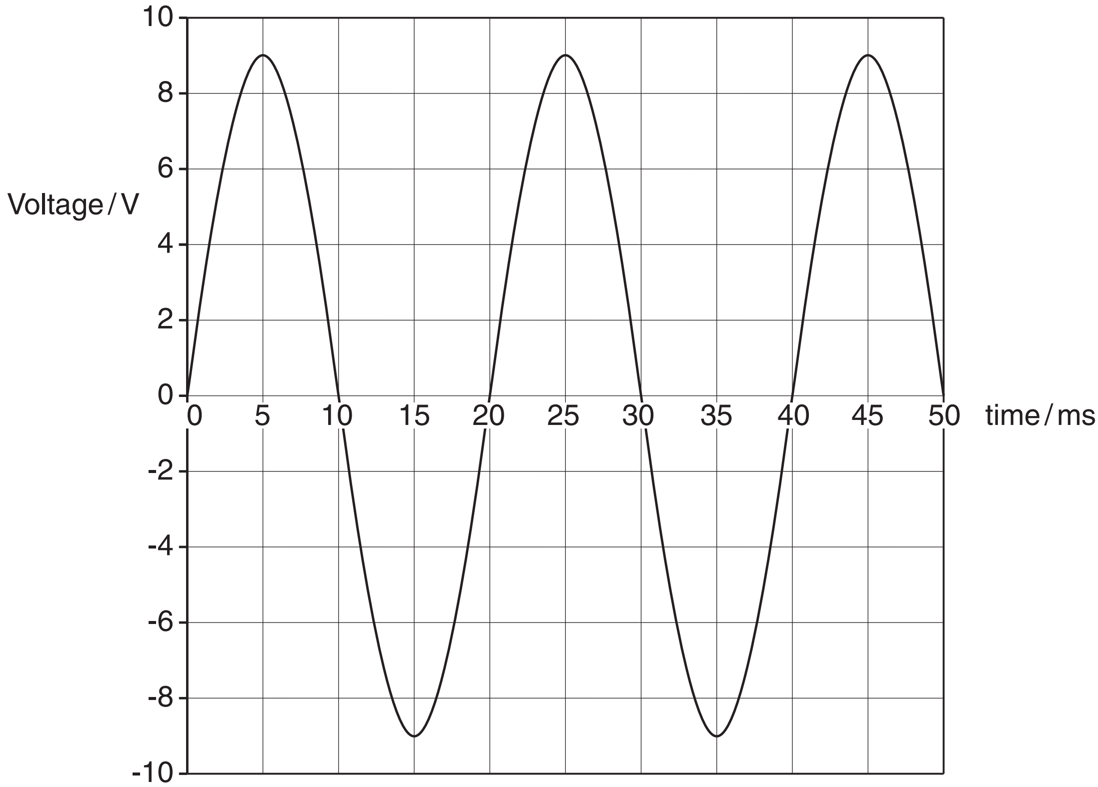

Fig. 3.2 **[4]**

(iii) Add a smoothing capacitor to the circuit in Fig. 3.1 **[1]**

(iv) Draw on Fig. 3.3 to show how V_B varies with time now that the smoothing capacitor is in the circuit. Assume that the current is being drawn by the voltage regulator.

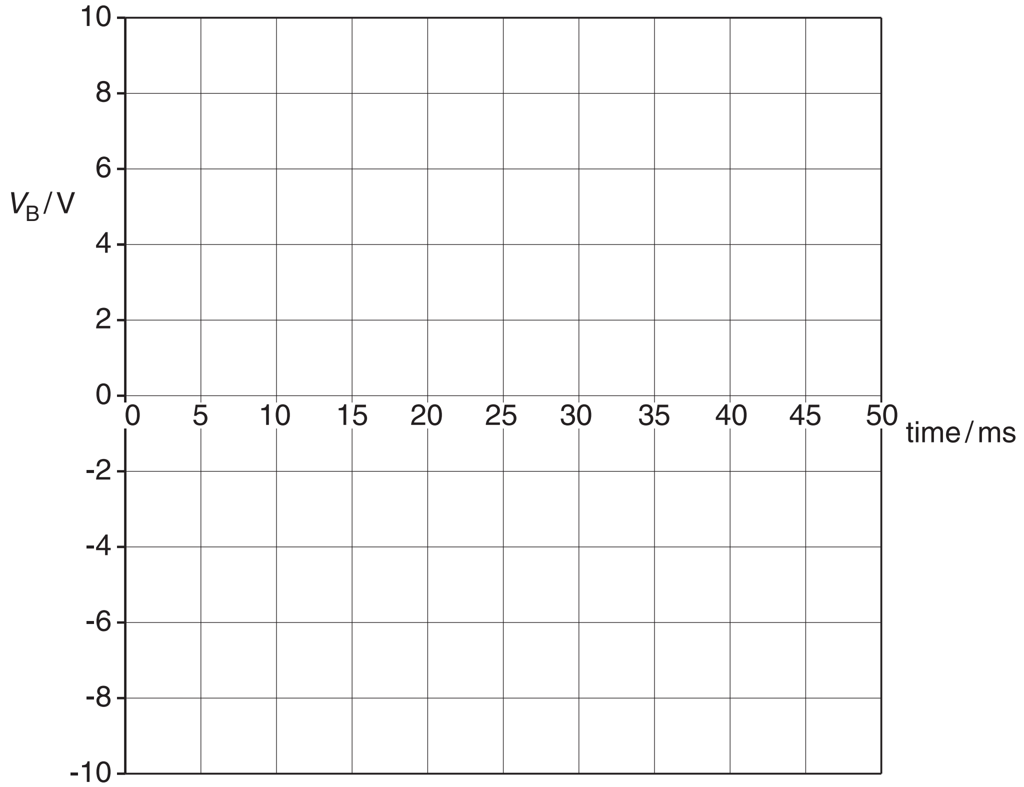

Fig. 3.3

[3]

(b) An incomplete circuit for the regulator is shown in Fig. 3.4.

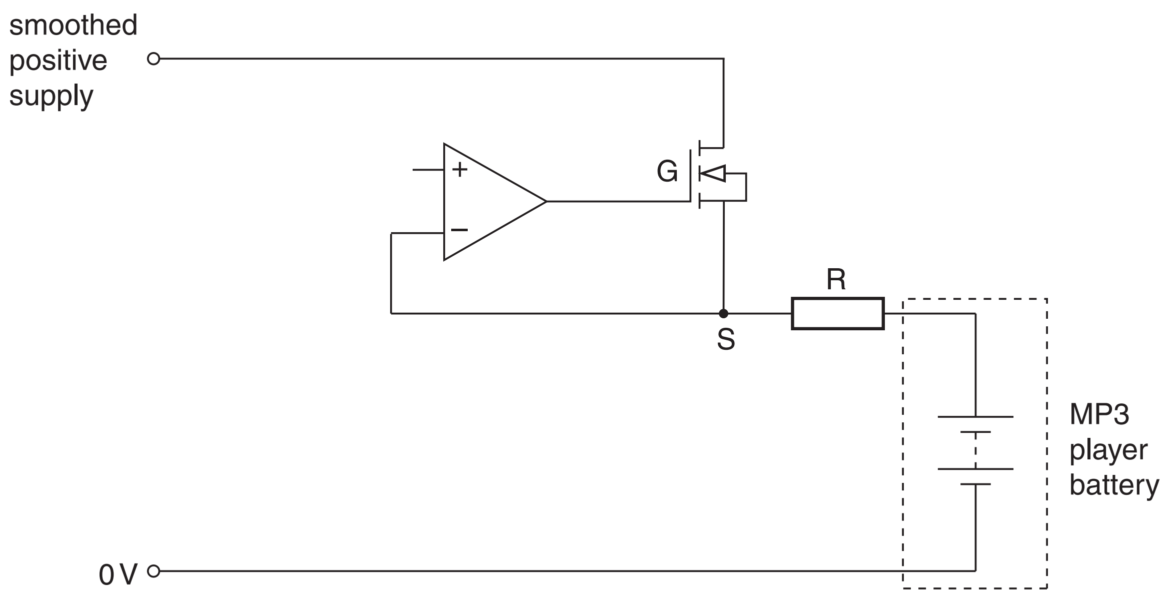

Fig. 3.4

(i) Complete the circuit in Fig. 3.4 by adding a resistor and zener diode to produce 5V at the non-inverting input of the op-amp. **[4]**

(ii) The MP3 player uses a current of 60 mA when charging. Calculate how much power is dissipated in the MOSFET when the smoothed supply is 12 V.

Power = ... W **[3]**

(iii) As the battery in the MP3 player charges up the voltage across the battery increases. Explain how the regulator of Fig. 3.4 responds to this change.

....

....

....

....

....

.... **[4]**

[Total: 20]

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4 Fig. 4.1 shows a circuit containing a MOSFET.

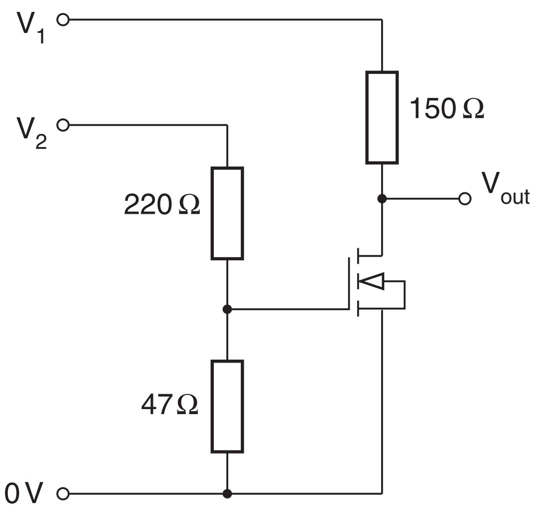


Fig. 4.1

(a) Draw a voltmeter on Fig. 4.1 to show how you would measure the voltage between the gate and source of the MOSFET. **[2]**

(b) Do a calculation to show that the voltage at the gate of the MOSFET is about 2 V when V_2 is 12 V.

[3]

(c) The graph in Fig. 4.2 show the how drain-source current depends on drain-source voltage at different gate-source voltages, V_{GS}.

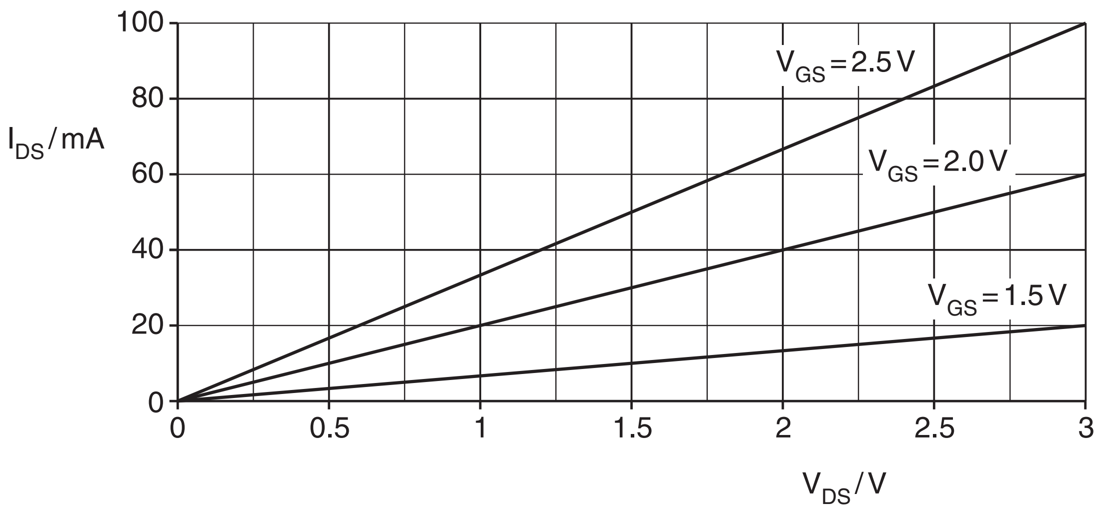


Fig. 4.2

(i) Calculate the resistance between the drain and source of the MOSFET when V_{GS} is 2 v.

Resistance = …………… Ω **[3]**

(ii) Calculate V_{out} when V_1 = 4 V and V_2 = 12 V.

V_{out} = …………… V **[3]**

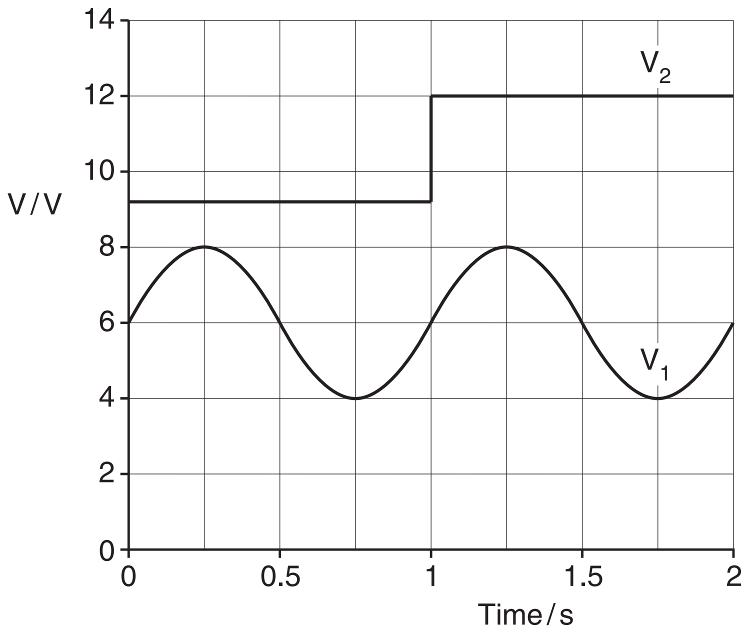
(iii) Explain what would happen to V_{out} if the voltage at the gate was decreased whilst V_1 was kept at 4 V.

....

....

.... **[2]**

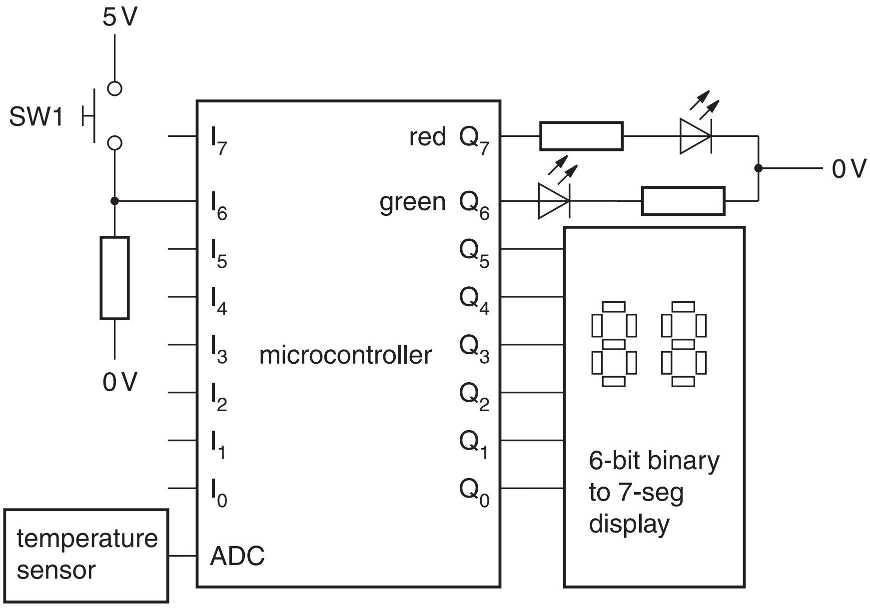
(iv) Draw the waveform for V_{out} on the graph below.



[3]

[Total: 16]

5 A microcontroller is used to make a thermometer for measuring body temperature.




```
start:   MOVI    S0, 00
         OUT     Q, S0
         RCALL   switch
         RCALL   readadc
rising:  MOV     S1, S0
         RCALL   wait2s
         RCALL   readadc
         SUB     S1, S0
         JNZ     rising
         MOVI    S4, 40
         EOR     S0, S4
         OUT     Q, S0
         RCALL   wait250ms
         EOR     S0, S4
         OUT     Q, S0
         RCALL   switch
         JP      start
```

Fig. 5.1

The system operates as follows:

- Press and release SW1.
- The red LED flashes to show the temperature of the sensor is changing.
- The green LED glows when the temperature stops changing.
- The temperature is displayed on the 7-seg display until SW1 is pressed.

(a) The subroutine at switch: which waits for the switch to be pressed is listed below. Fill in the missing parts.

```
switch:   IN        S4,I
          MOVI      S5, ............
          ..........  ...... , .........
          JZ        switch
          RET
```

[2]

(b) The subroutine at wait2s: produces a delay of 2 seconds whilst flashing one of the LEDs. Explain how the subroutine works.

Label	Instruction		Explanation
wait2s:	MOVI	S5, 08	....
	MOVI	S6, 0	....
loop:	MOVI	S7, 80	
	EOR	S6, S7	....
	OUT	Q, S6	....
	RCALL	wait250ms	wait for 0.25s before continuing
	DEC	S5	....
	JNZ	loop	....
	RET		.... **[7]**

(c) Write a subroutine to produce a time delay of 250 ms at wait250 ms:. Use the subroutine at wait1 ms:.

Labels	Instructions
wait250ms:	....
....	....
....	....
....	....
....	....
....	....

[5]

(d) State the hexadecimal number that will need to be output to Q to turn on the green LED and display the number 37:

(i) In binary .... **[1]**

(ii) In hexadecimal .... **[1]**

[Total: 16]

6 The diagram for a system to control the position of an aerial on a roof is shown in Fig. 6.1.

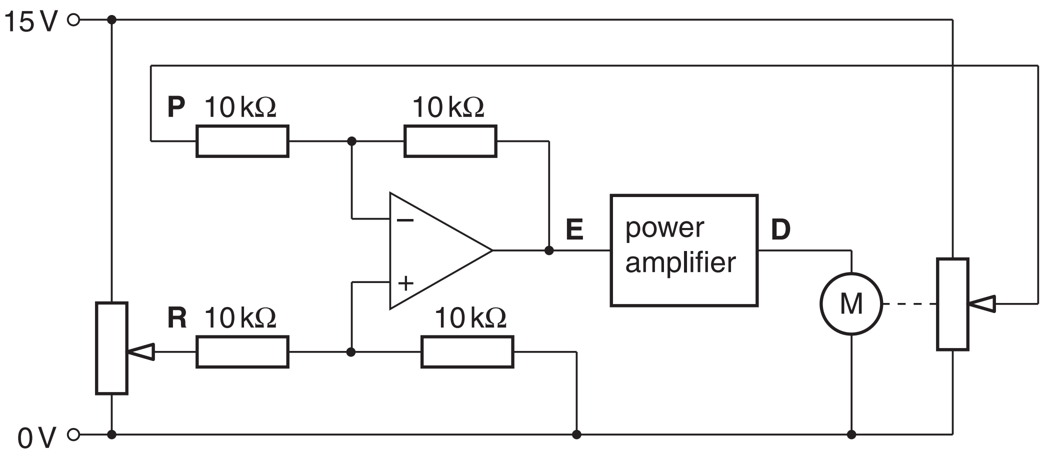


Fig. 6.1

(a) State the voltage at **E** when the voltage at R is 2.5V and the voltage at P is 7.5V.

Voltage at E = ...V **[1]**

(b) The power amplifier has voltage gain of 2. Draw a diagram for the power amplifier based on a high current op-amp. Show all component values.

[4]

(c) The graphs in Fig. 6.2 show the voltages in the circuit. Complete the graphs for E, D and P. P starts at 7.5V.

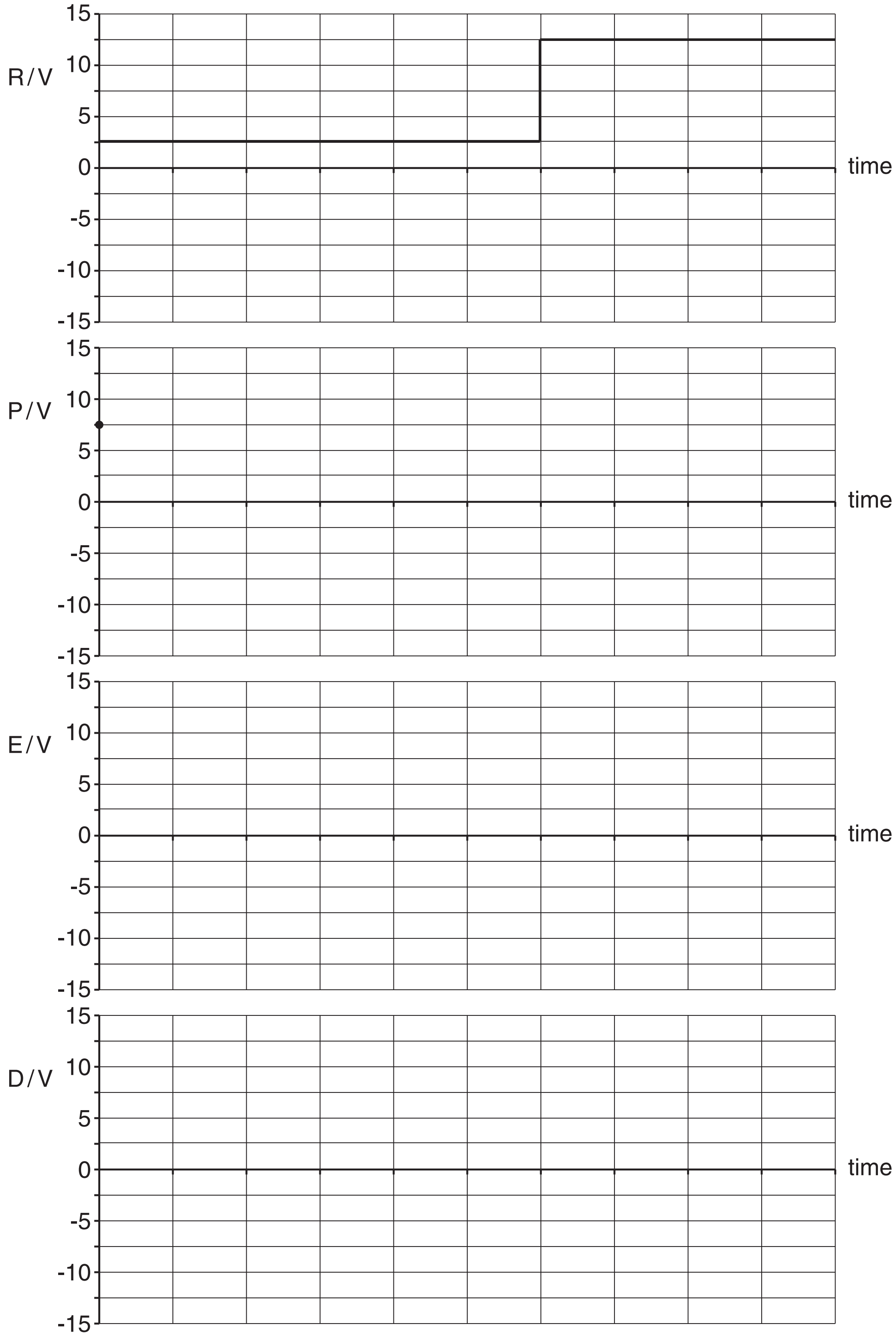


Fig. 6.2

[7]

[Total: 12]

7 Fig. 7.1 shows a volatile memory cell made from a D-type flip-flop and a tristate.

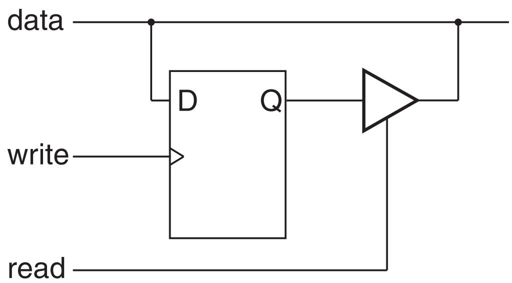


Fig. 7.1

(a) Explain the meaning of the word "volatile" for a memory.

.... **[1]**

(b) State the function of the tristate in a memory cell.

.... **[1]**

(c) Fig. 7.2 shows a memory module with two data lines D_0 and D_1 and one address line A_0.

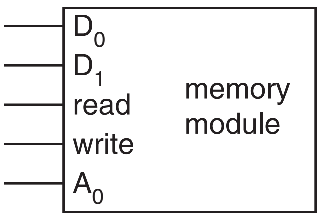


Fig. 7.2

Draw on Fig. 7.3 to show how the memory module in Fig. 7.2 can be constructed from several memory cells in Fig. 7.1 and the two demultiplexers shown.

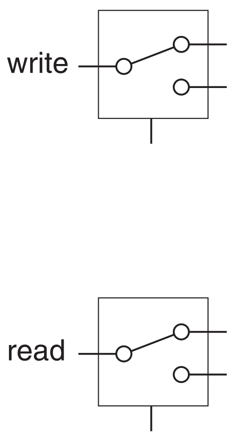
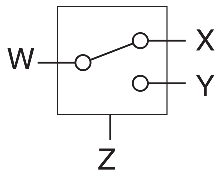


Fig. 7.3 **[4]**

(d) Show how one of the demultiplexers can be constructed from logic gates. Use a truth table to justify your design.



[3]

[Total: 9]

Quality of written communication [3]

END OF QUESTION PAPER

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