GCE MARKING SCHEME

ELECTRONICS
AS/Advanced

SUMMER 2015

INTRODUCTION

The marking schemes which follow were those used by WJEC for the Summer 2015 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>1.</td><td>(a)</td><td></td><td>One mark for each correct column X, Y and Q no ecf
<table>
<tr><td>B</td><td>A</td><td>X</td><td>Y</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>3</td></tr>
<tr><td></td><td>(b)</td><td></td><td>Correct NAND gate replacement for OR gate drawn.</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>4</td></tr>
<tr><td>2.</td><td>(a)</td><td>(i)</td><td>
<table>
<tr><td>C</td><td>B</td><td>A</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
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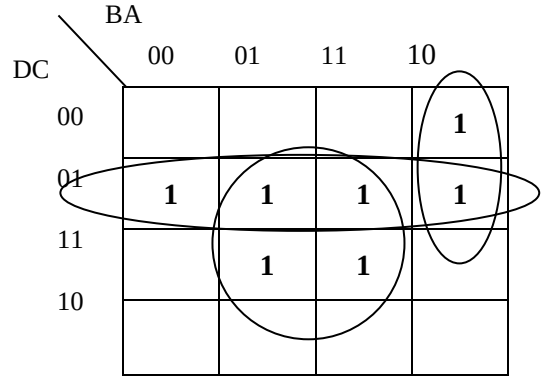
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Completely correct 2 marks. Reverse order 1 mark only

$Q = \overline{C}.B.\overline{A} + C.\overline{B}.\overline{A} + C.B.\overline{A}$ allow correct simplification (one error award 1 mark) ecf (a)(i)</td><td>2

2</td></tr>
<tr><td></td><td>(b)</td><td></td><td>By altering the connections between the D inputs <u>and</u> the power rails.</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>5</td></tr>
</table>

Question			Marking detail	Marks available
3.	(a)		Output Logic 1 between first falling-edge of A and first-rising edge of B	1
			Output logic 1 when A is logic 0 for final time. (-1 mark for each additional transition up to a maximum of 2 marks)	1
	(b)		EXNOR, XNOR	1
				3
4.	(a)		To keep the input X at logic 1 when switch A is open. (accept 'it acts as a pull-up resistor')/ To prevent short-circuit of power rails.	1
	(b)		Y = [logic] 0	1
	(c)		Inputs from switches to NOR gate Output of NOR and Pulses to AND gate Output of AND gate to Q (Possible alternative OR then NOR)	1 1 1
				5

Question			Marking detail	Marks available
5.	(a)	(i)	$\overline{C}.0 = 0$	1
		(ii)	$D + \overline{D} = 1$	1
	(b)			
			Correct map	1
			Two groups of 4 and one of 2 identified (**ecf** map)	1
			Any correct term from groups identified on the map	1
			Simplest overall expression	1
			$Q = \overline{D}.C + C.A + \overline{D}.B.\overline{A}$	
	(c)		$Q = (B.A) + \overline{A}$ 1 mark (DeMorgan) $B + \overline{A}$ 1 mark (simplification) Alternative solution: $\overline{(\overline{B} + \overline{A}).A} = \overline{\overline{B}.A} = B + \overline{A}$	2
				8
6.	(a)	(i)	Binary 11101101	1
		(ii)	BCD 0010 0011 0111	1
	(b)		Band D selected and connected to logic gate inputs	1
			Single AND gate chosen with output to R	1
				4

Question			Marking detail	Marks available
7	(a)		$\overline{Q}$ = [logic] **1**	1
	(b)		Q responds correctly to: ▪ Clock/data (3 correct = 2 marks, 2 correct = 1 mark) ▪ Reset ▪ Set (-1 mark for each additional transition up to a maximum of 2 marks)	2 1 1
				5
8.	(a)		▪ $\overline{Q}$ to D × 3 ▪ clock inputs correct × 3 ▪ Q to resistor/LED × 3	1 1 1
	(b)		Switch and resistor across power rails with correct orientation. Correct connection of switch unit to 3 resets	1 1
	(c)	(i)	120	1
		(ii)	15 **ecf** from (c)(i) (i.e. $\frac{1}{8}$ of the answer)	1
				7

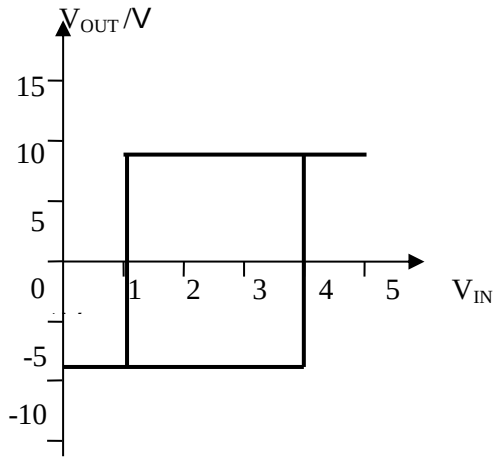
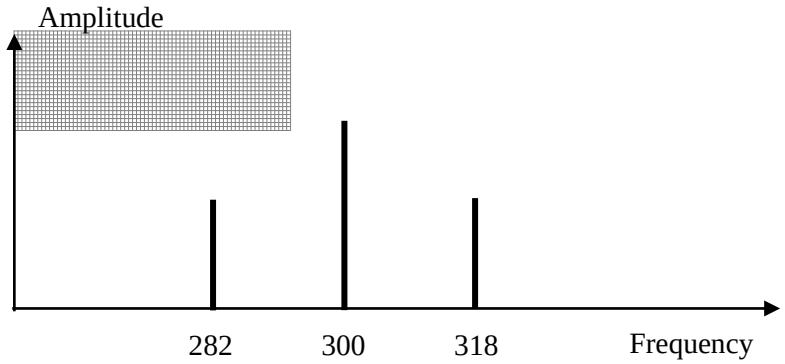
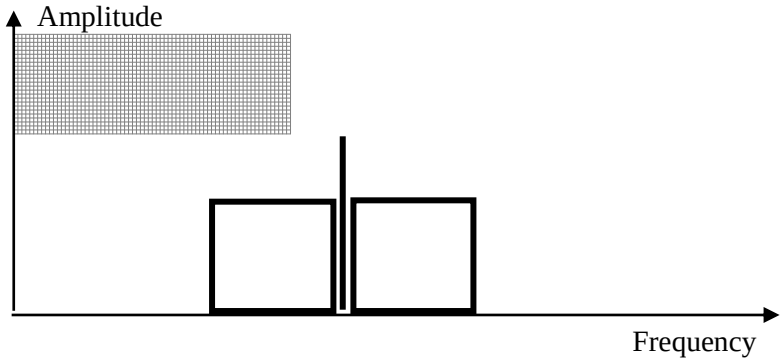
Question			Marking detail	Marks available
9.	(a)		▪ Inverse sloping line through (0,0) ▪ Correct gradient (passes through 100, -7.5) ▪ Saturation at 18 V × 2 (240, -18)	1 1 1
	(b)	(i)	BW = 48 k[Hz] or 0.048 M[Hz] or 48 000 [Hz]	1
		(ii)	Horizontal line at gain 75 Sloping line through (48,53) **ecf** from (b)(i)	1 1
	(c)	(i)	▪ Operational amplifier with negative feedback resistor drawn correctly ▪ Resistor between V_{IN} and inverting input ▪ Non-inverting input to 0 V	1 1 1
		(ii)	R_F and R_1 in ratio 75:1 (both 1 kΩ or greater as requested) Correctly assigned and identified on the circuit diagram.	1 1
				11
10.	(a)		Voltage gain = 7	1
	(b)		2.0×10^{12} [Ω] or 2 T[Ω]	1
	(c)	(i)	$40 \times 9 = 360$ [mV]	1
		(ii)	Sine wave of correct frequency and phase Voltage peaks at ± 360 mV **ecf** from (c) (i)	1 1
	(d)		$\frac{13.5}{9} = 1.5$ [V] or 1 500 m[V]	1
	(e)		$\frac{27}{6} = 4.5$ (1 mark) μs (1 mark) (unit consistent with number)	2
				8

ET2

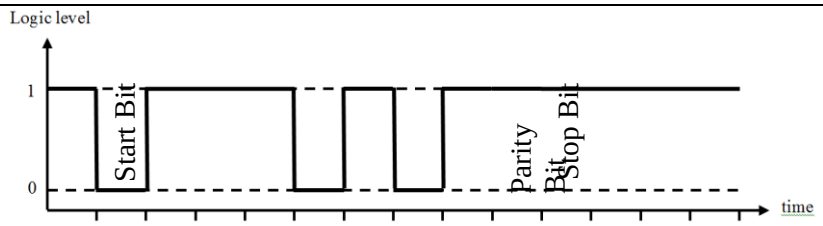
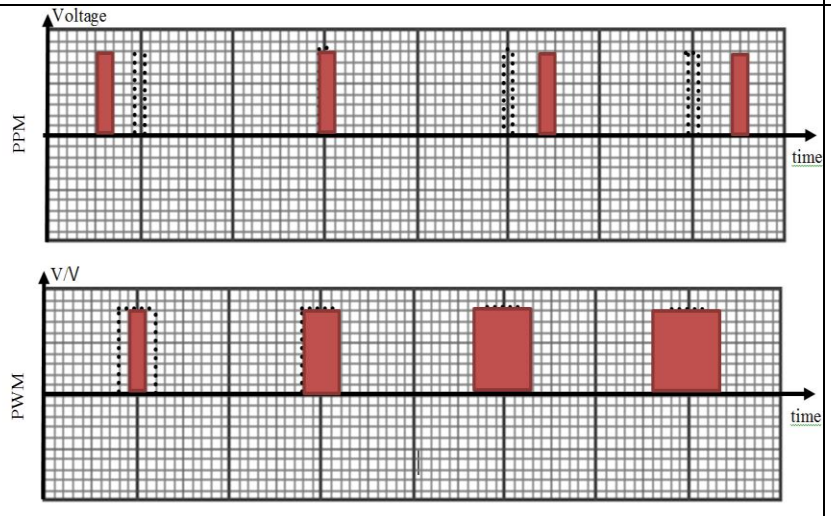
Question			Answers/Explanatory Notes * Indicates that ECF will be allowed from a previous part	Marks Available
1	a	(i)	0.5 kΩ (1)	2
		(ii)	1.5 kΩ (1)	
	b	(i)	I_1 = 8 mA (1) *	4
		(ii)	I_2 = 4 mA (1) *	
		(iii)	V_1 = 4 V (1)	
		(iv)	V_2 = 8 V (1) *	**[6]**
2.	a	(i)	V_{OC} = 6.75 V (1)	3
		(ii)	I_{SC} = 0.069 A (1)	
		(iii)	R_O = 97.5 Ω (1) *	
	b		Voltage drop across 120 Ω resistor = 3 V (1) Current through 120 Ω resistor = 0.025 A (1) Minimum value of load resistance = 200 Ω (1) *	3 **[6]**
3.	a	(i)	5.5 V (1)	2
		(ii)	3 V (1) [allow 1 mark if answers reversed]	
	b	(i)	Resistor connected between i/p and o/p of Schmitt (1) Capacitor connected between 0 V and Schmitt i/p (1)	2
		(ii)	Suitable method (1) Correct values (1) Any combination of R and C with a period of 5 ms e.g. R = 1 kΩ; C = 5 μF	2 **[6]**
4.	a	(i)	Graph 3 (1)	3
		(ii)	Graph 4 (1)	
		(iii)	Graph 2 (1)	
	b	(i)	Correct position and symbol for capacitor (1) 3 correct connections (1)	2
		(ii)	16.6 V (1)	1 **[6]**

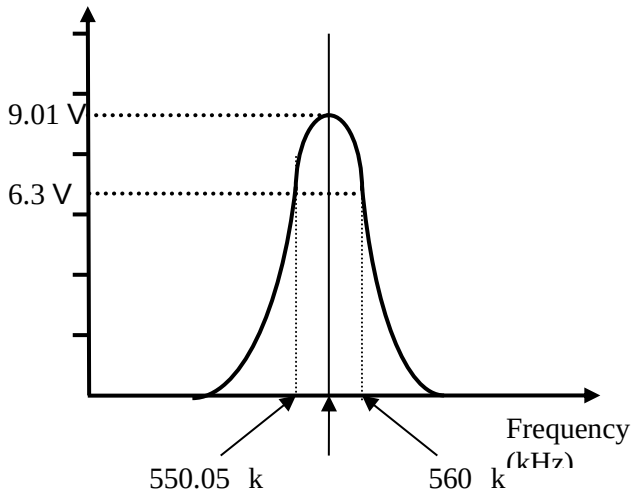
Question			Answers/Explanatory Notes * Indicates that ECF will be allowed from a previous part	Marks Available
5.	a		Correct components in voltage divider (1) Correct orientation (with pull up resistor) (1)	2
	b		Substitution with correct multipliers (1) 5.17 secs (1)	2
	c	(i)	Voltage across R = 4 V (1)	3
		(ii)	$R = \frac{4}{24mA} = 167\,\Omega$ (1) * 180 Ω (1) *	
				[7]
6.	a		Diode in inverse parallel across solenoid (1)	1
	b		Substitution (1) 4.8 V (1) *	2
	c		Substitution (1) 18.72 W (1)	2
				[5]
7.	a	(i)	Appropriate scales (1) Quality of curve (1) At least 5 accurate points (1)	3
		(ii)	4 kΩ (accept 3.8 – 4.2 kΩ) (1) *	1
	b	(i)	Two 10 kΩ resistors in voltage divider connected to V- (1)	3
		(ii)	2.08 V (accept 2– 2.1 V / * allow ecf from a(ii)) (1)	
		(iii)	LED off : V- larger than V+ (1)	
				[7]

Question			Answers/Explanatory Notes * Indicates that ECF will be allowed from a previous part	Marks Available
8.	a	(i)	$I_B = \frac{120}{80} = 1.5\,mA$ (1)	3
		(ii)	Voltage across base resistor = 3.4 - 0.7 = 2.7 V (1) $R = \frac{2.7V}{1.5mA} = 1.8\ k\Omega$ (1) *	
	b		Shape (1) Plotting point (0.7, 9) (1) Plotting point (3.4, 0) (1)	3
	c	(i)	$V_{OUT} = 3 \pm 0.5\,V$ (1) *	2
		(ii)	$3\,V \times 80\,mA = 240\,mW$ (1)	
	d		Resistor and LDR in voltage divider (1) LDR at bottom (1)	2
				[10]
9.	a		15 – 5.6 = 9.4 V (1) $\frac{9.4}{20} = 0.47\,A = 470\,mA$ (1)	2
	b		470 – 6 = 464 mA (1) *	1
	c		Voltage across 20 Ω resistor = 600 mA × 20 Ω = 12 V(1) $V_{LOAD} = 3\,V$ (1)	2
	d		Horizontal line at 5.6 V until I = 464 mA (1) * Gradual downward slope thereafter (1)	2
				[7]
			TOTAL	**60**

Question			Marking details	Marks Available
1	*(a)*		Non-Inverting	1
	(b)			
			Saturation Levels at ± 9 V	1
			Switching thresholds at 1 V and 4 V	1
			Non-inverting characteristic	1
				[4]
2	*(a)*			
			Line spectrum	1
			Correct carrier frequency	1
			Correct side band frequencies	1
	(b)	(i)		
			Continuous band spectrum	1
		(ii)	36 kHz	1

Question			Marking details	Marks Available
2.	*(c)*	(i)	$f_c = \frac{1}{14.28 \times 10^{-6}} = 70\ 000$ Hz $= 70$ kHz ($\pm$ 0.2 kHz)	1
		(ii)	$f_i = \frac{1}{200 \times 10^{-6}} = 5\ 000$ Hz $= 5$ kHz	1
		(iii)	Modulation Depth $= \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}} \times 100\%$	
			$= \frac{3-0.4}{3+0.4} \times 100\% = 76.5\%$ (Accept 71-77%)	1
				[8]
3.	*(a)*	(i)	T	1
		(ii)	Q	1
		(iii)	R & S	1
		(iv)	P or R or S	1
	(b)	(i)	Poor Selectivity – The inability to reject nearby stations.	1
		(ii)	Poor Sensitivity – The inability to detect weak stations.	1
	(c)	(i)	1.680 MHz / 2.145 MHz / 3.825 MHz / 0.465 MHz or 465 kHz	
			All 4 Correct = 2 marks 3 Correct = 1 mark	2 or 1
		(ii)	0.465 MHz or 465 kHz	1
				[9]

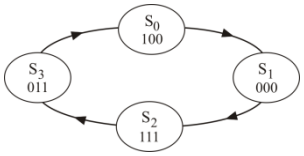
Question			Marking details	Marks Available
4.	*(a)*	(i)	 1 mark for each correct label	3
		(ii)	Character transmitted = "W", No marks for "U"	1
	(b)	(i)	<table><tr><td>P_4</td><td>P_3</td><td>P_2</td><td>P_1</td><td>P_0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table> All five correct = 2 marks All five inverted = 1 mark	2 or 1
		(ii)	(I) P_0 and P_4 fail the parity check	1
			(II) P_0 and P_4 fail the parity check – common to D_3, so this is where the error is.	
			<table><tr><td>D_7</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td>P_4</td><td>P_3</td><td>P_2</td><td>P_1</td><td>P_0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	1
				[8]
5.	*(a)*		 Correct Method in each case (2 x 1) Consistent Application in each case (2 x 1)	1 1 1 1
	(b)		No of levels required = $\frac{5}{500\text{x}10^{-6}} = 10\ 000$	1
			13 bits provide 2^{13} = 8 192 levels, 14 bits provide 2^{14} = 16 384 levels, so 14 bits would be suitable.	1 **[6]**

Question			Marking details	Marks Available
6.	*(a)*		$f_o = \dfrac{1}{2\pi\sqrt{LC}} = \dfrac{1}{2\pi\sqrt{0.02 \times 10^{-3} \times 4 \times 10^{-9}}}$ $= 562\ 698\ \text{Hz} \cong 560\ \text{kHz}$ multipliers answer	 1 1
	(b)		$R_D = \dfrac{L}{r_L C} = \dfrac{0.02 \times 10^{-3}}{2.5 \times 4 \times 10^{-9}} = 2\ 000\ \Omega = 2\ \text{k}\Omega$ correct substitution in correct formula answer	 1 1
	(c)		$V_{\text{OUT}} = \dfrac{10 \times 2\ 000}{220 + 2\ 000} = 9.01\ \text{V}$ Substitution in formula answer	 1 1
	(d)		$Q = \dfrac{2\pi f_o L}{r_L} = \dfrac{2\pi \times 562\ 698 \times 0.02 \times 10^{-3}}{2.5}$ $= 28.3\ (28.1\ f\text{or}\ 560\text{k})$ answer	 1
	(e)		bandwidth $= \dfrac{f_0}{Q} = \dfrac{562\ 698}{28.3} = 19\ 883\text{Hz} = 19.9\ \text{kHz}$ answer only	 1
	(f)		 • Shape (1) • Peak output voltage 9 V (1) • Correct resonant frequencies and use of 0.7 × peak to plot bandwidth (1)	 3
				[11]

Question			Marking details	Marks Available
7.	*(a)*		$\frac{12 - V_{IN}}{9} = \frac{12 - 1}{6.8}$ $12 - V_{IN} = \frac{9 \times 11}{6.8}$ $12 - V_{IN} = 14.56$ $V_{IN} = 12 - 14.56 = -2.56\ \text{V}$ correct formula / substitution correct answer	 1 1
	(b)		$\frac{-12 - V_{IN}}{9} = \frac{-12 - 1}{6.8}$ $-12 - V_{IN} = \frac{9 \times -13}{6.8}$ $-12 - V_{IN} = -17.21$ $V_{IN} = -12 + 17.21 = 5.21\ \text{V}$ correct formula / substitution correct answer	 1 1
				[**4**]

1. *(a)* One count not completely registered before next pulse arrives (or equivalent.) 1 mark

(b) (i)



Completely correct 1 mark

(ii) '001' (only correct answer) 1 mark

(iii) Any unused state, such as '010' 1 mark

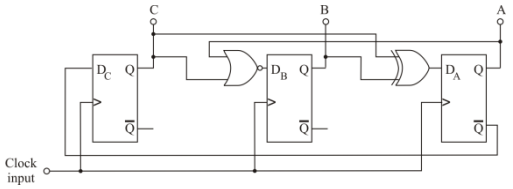
(iv) State 5 progresses through '110' to main sequence, or equivalent 1 mark

Timing information 1 mark

State 4 loops back to itself continuously, or equivalent 1 mark

Total for Q1 **7**

2. *(a)*



Clock connections correct 1 mark

D_C correct 1 mark

D_B correct 1 mark

D_A correct 1 mark

Use of $\overline{Q}$ 1 mark

(b)

	Current state				Next state			
State	**Light**	**Pump**	**Paddle**	**Solenoid**	**Light**	**Pump**	**Paddle**	**Solenoid**
0	0	0	0	0	1	0	0	0
1	1	0	0	0	1	1	0	0
2	1	1	0	0	1	1	1	0
3	1	1	1	0	1	0	1	1
4	1	0	1	0	1	0	0	1
5	1	0	0	1	0	0	0	0

Buzzer correct 1 mark

Pump correct 1 mark

Paddle correct 1 mark

Solenoid correct 1 mark

Total for Q2 **9**

3. *(a)* (i) Grey code 1 mark

(ii) Binary can give false readings when near segment boundaries/moving between segments causing either false alarms, or missing alarm conditions, or equivalent. 1 mark

(b) Q = Z . X, or equivalent

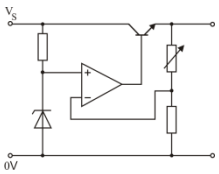
Correct operator 1 mark

Correct signals 1 mark

(c) Any application in which speed is monitored, or equivalent. 1 mark

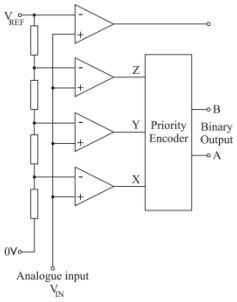
Total for Q3 **5**

4. *(a)* (i)



	Zener sub-system correct	1 mark
	Non-inv amp correct	1 mark
	Emitter follower correct	1 mark
(ii)	Line regulation keeps output voltage steady when supply voltage varies	1 mark
(iii)	As V_S increases, voltage across resistor increases, but output of zener, and so V_{REF}, remains constant, or equivalent	1 mark

(b) (i)



	Use of three comparators	1 mark
	Correct input and output connections to comparators	1 mark
(ii)	All resistor values equal	1 mark
	All resistor values >1 kΩ	1 mark
(iii)	V_{REF} = 1.00 V	1 mark
(iv)	B = 1_2 A = 0_2	1 mark
	Total for Q4	**11**

5. *(a)* 04 goto **warn** 1 mark

(b) 100 warn movlw b'**10000000**' 1 mark

101 **movwf** PORTB 1 mark

(c) Instruction at address 103 switches off the lamp, or equivalent 1 mark

(d) Working register contains '4' 1 mark

(e) (i) 99 warn **movwf** **Wstore**

107 **movf** **Wstore,0**

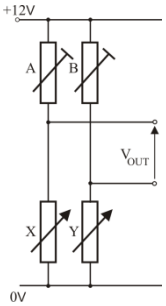
correct use of Wstore 1 mark

correct destination 1 mark

(ii) Flag indicates that interrupt has been serviced or equivalent 1 mark

Total for Q5 **8**

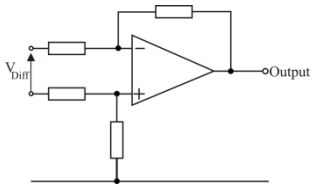
6. *(a)*



Two voltage dividers each having strain gauge and variable resistor — 1 mark
Correct orientation / use of correct symbols — 1 mark

(b) Both strain gauges warm up equally. Both increase in resistance equally.
Produces same change in output of each voltage divider.
Changes cancel each other out, (or equivalent.) — 1 mark

(c) (i)



Inverting input at mid-point of voltage divider as shown — 1 mark
Non-inverting input at mid-point of voltage divider as shown — 1 mark

(ii) Correct ratio of feedback to input resistor, AND values > 1 kΩ — 1 mark
Values symmetrical on inverting and non-inverting inputs — 1 mark

(iii) Output = 200 × 3.5 = 700 mV — 1 mark

Total for Q6 **8**

7. *(a)* (i) **A, F, H**
All three conditions, and no others — 1 mark

(ii) **C**
All three conditions (and no other) — 1 mark

(b) (i) X = 12 V AND Y = 12 V — 1 mark

(ii) X = 0 V AND Y = 12 V — 1 mark

(iii) I X = -12 V AND Y = 0 V — 1 mark
II Reverse biases the thyristor, causing it to switch off, or equivalent — 1 mark

Total for Q7 **6**

8. *(a)* (i) Signal 4 — 1 mark

(ii) Signal 5 — 1 mark

(iii) Signal 2 — 1 mark

(b) (i) Diac — 1 mark

(ii) C — 1 mark

(c) Phase shift = $\tan^{-1}\left(\frac{R}{Xc}\right)$ — 1 mark

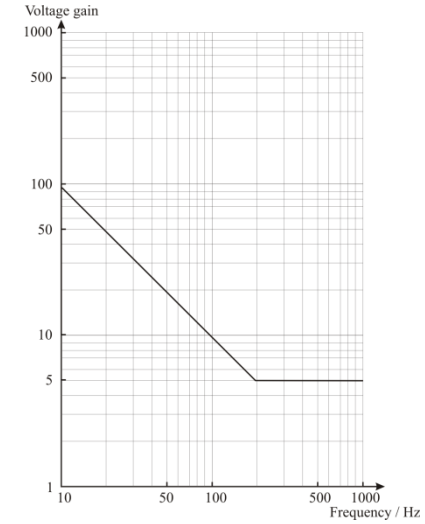
Evidence of correct interpretation of multipliers and/or X_C
$= 88.4^0$ — 1 mark

Total for Q8 **7**

9. *(a)* (i) Break frequency = 195 Hz (or 195.04 Hz) 1 mark

(ii) Voltage gain = 5 1 mark

(iii)



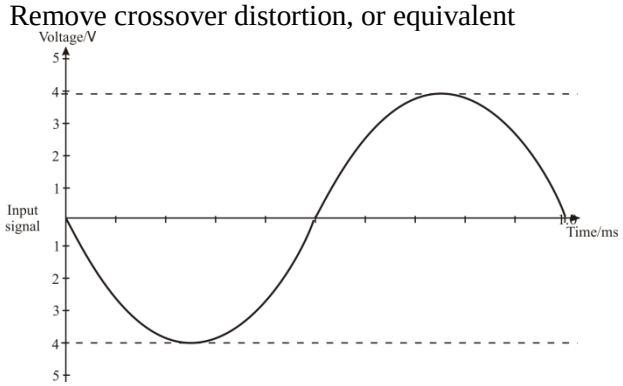
Correct shape for bass boost filter 1 mark

Break frequency as in *(a)*(i) 1 mark

Voltage gain as in *(a)*(ii) 1 mark

(b) (i) Remove crossover distortion, or equivalent 1 mark

(ii)



No crossover distortion 1 mark

Correct amplitude 1 mark

(iii) Max output power = $\frac{V_s^2}{8R_L}$

= 1.13 W (Accept 1 W) 1 mark

Total for Q9 **9**

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