Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

S15-1141-01

ELECTRONICS – ET1

A.M. TUESDAY, 12 May 2015

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**4**	
2.	**5**	
3.	**3**	
4.	**5**	
5.	**8**	
6.	**4**	
7.	**5**	
8.	**7**	
9.	**11**	
10.	**8**	
Total	**60**	

1141
010001

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier $G = -\frac{R_F}{R_{IN}}$

$$G = 1 + \frac{R_F}{R_1}$$

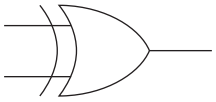
$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities $A + \overline{A}.B = A + B$

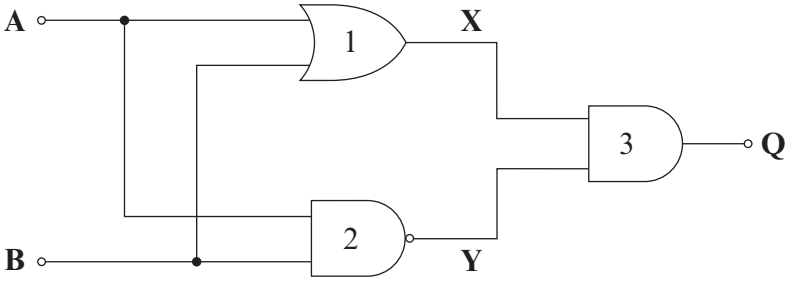
$$A.B + A = A.(B+1) = A$$

Examiner only

1. The symbol for the 2-input EXOR gate is shown below.



(a) An EXOR gate can be built from other logic gates. Complete the truth table to show that the following circuit produces the same output as an EXOR gate. [3]



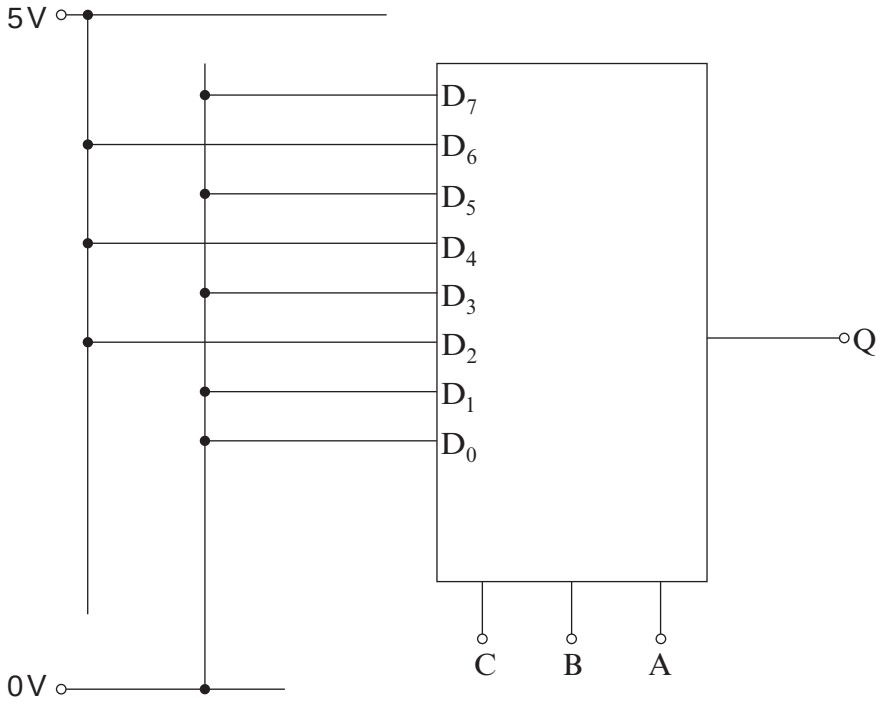
B	A	X	Y	Q
0	0			
0	1			
1	0			
1	1			

(b) The above circuit could be rebuilt using NAND gates only. Draw the NAND equivalent circuit for **gate 1** below. [1]

Turn over.

Examiner only

2. *(a)* A multiplexer can be used to perform logic functions.



(i) Complete the truth table for the multiplexer shown in the diagram. [2]

Inputs			Output
C	**B**	**A**	**Q**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(ii) Use the table to write down the **unsimplified** Boolean expression for Q in terms of C, B and A.

Q = ... [2]

Examiner only

(b) Explain how a multiplexer can be reconfigured to perform a different logic function. [1]

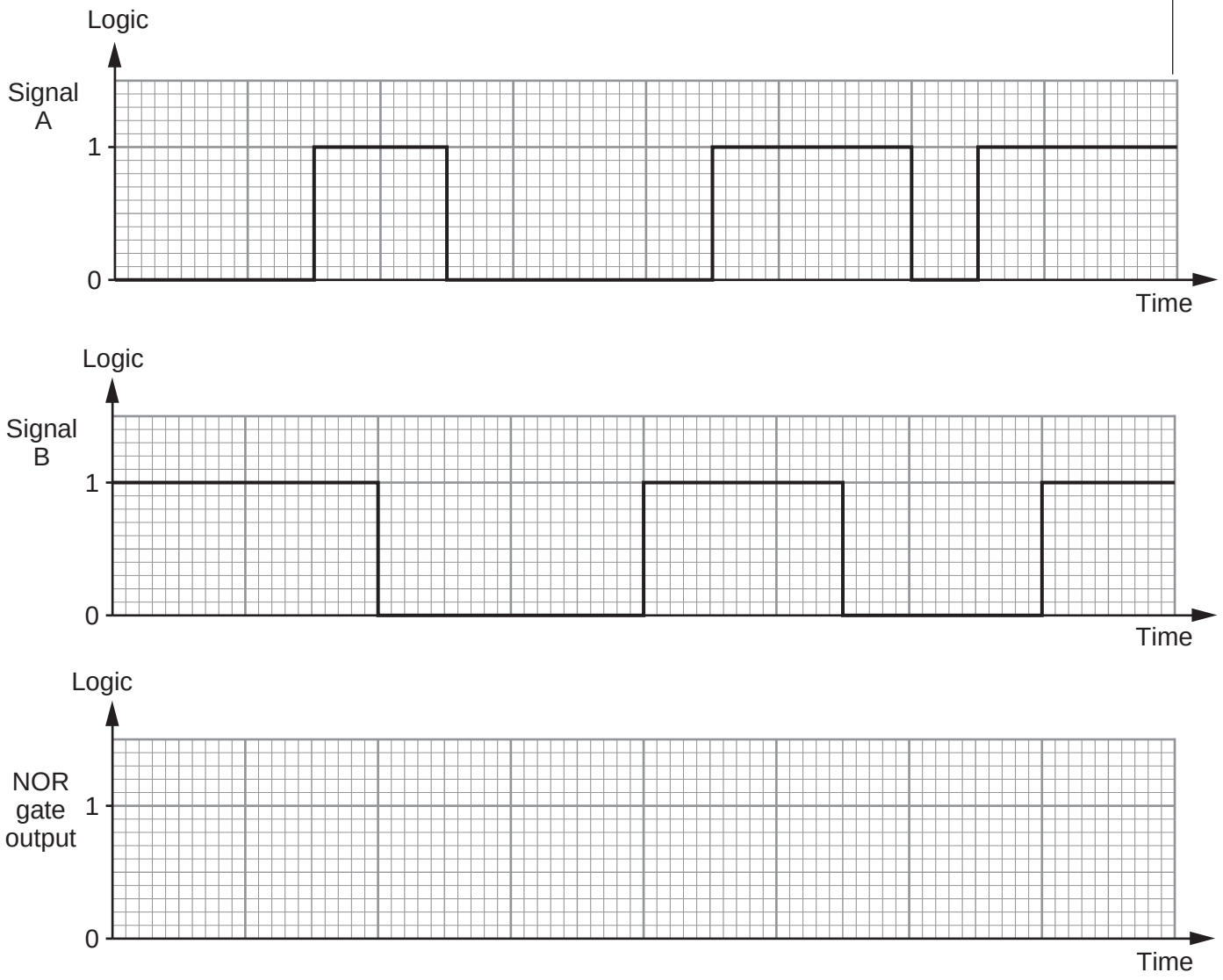
.....

.....

Turn over.

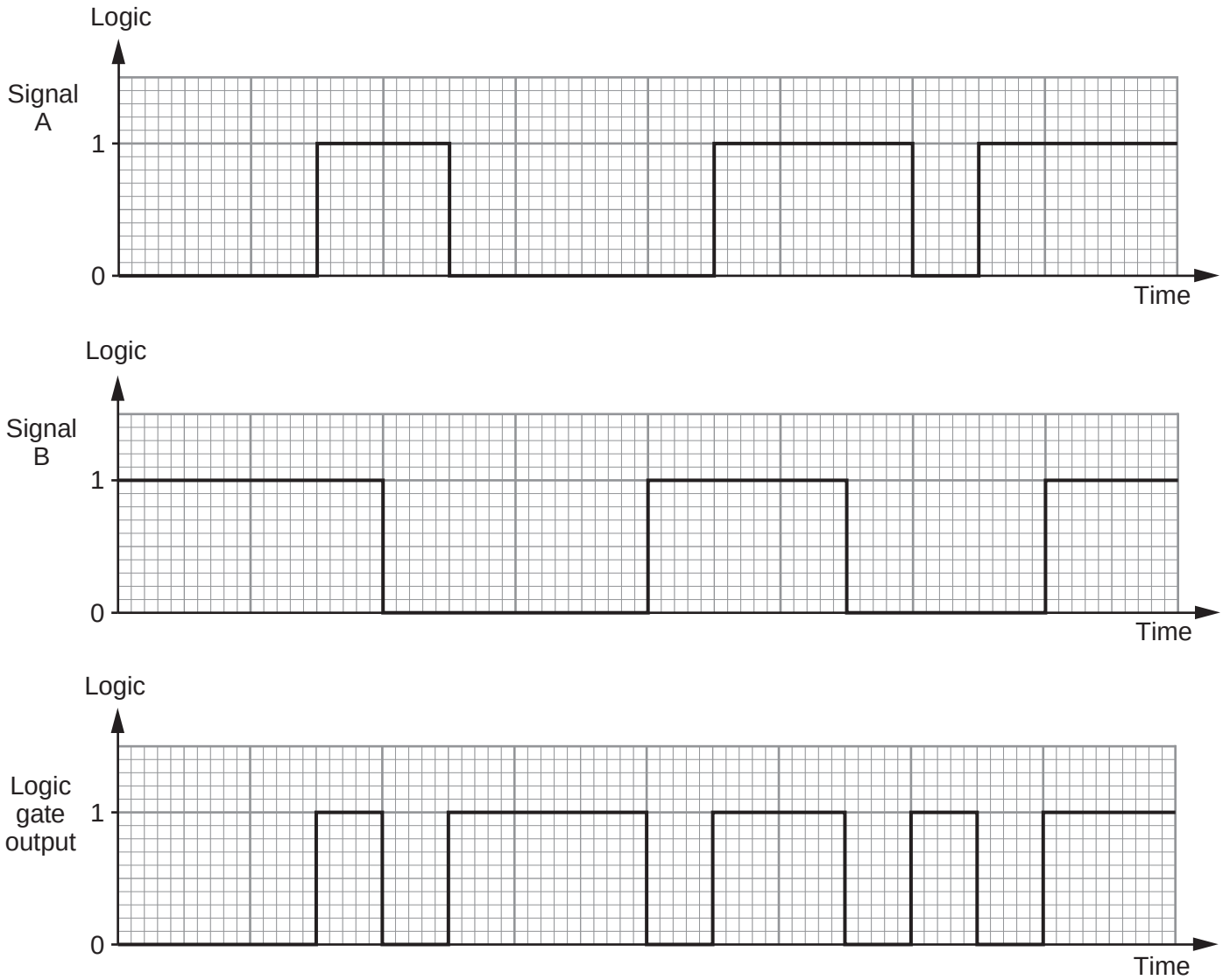
Examiner only

3. *(a)* Signals A and B are applied to the inputs of a 2-input NOR gate. Sketch the output. [2]



Examiner only

(b) Signals A and B are applied to a different 2-input logic gate. What type of logic gate will produce the output signal shown? [1]



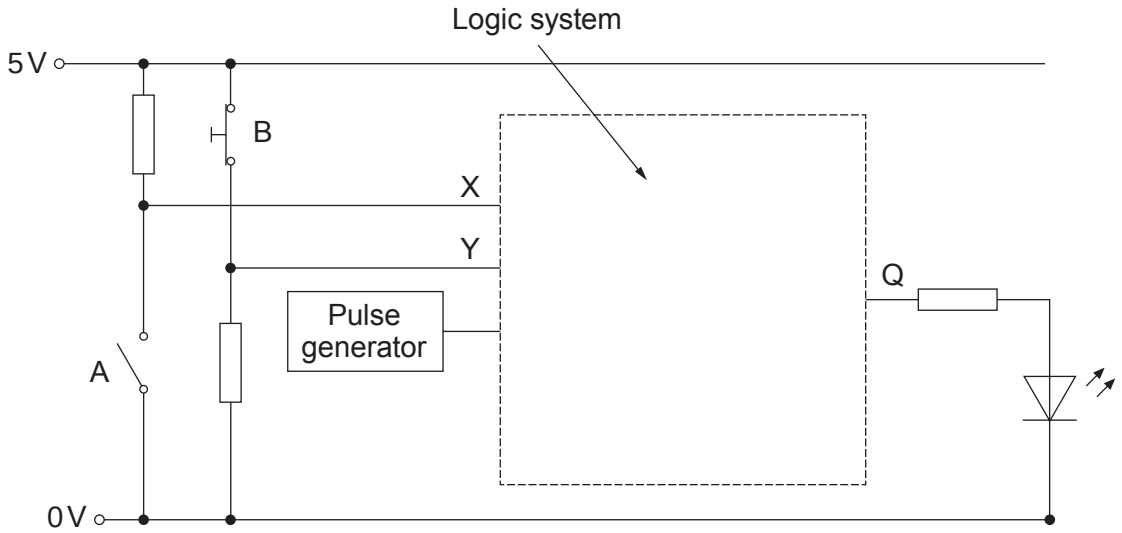
1141 010007

Logic gate .....

Examiner only

4. The diagram shows part of an alarm system used to protect a valuable object.

- Switch A is **closed** to set the alarm.
- If the object is moved switch B **opens**.
- The LED flashes if the object is moved after the system has been set.



(a) Why is a resistor needed with switch A? [1]

.....

.....

(b) What is the logic level at point Y when switch B is open? [1]

Logic level at Y .....

(c) Design a logic system, using **two 2-input** logic gates, such that the LED will flash only if the object is moved after the system has been set. Draw your design in the dotted box above showing the two logic gates and appropriate connections. [3]

Examiner only

5. *(a)* Simplify the following expressions.

(i) $\bar{C}.0$ = ... [1]

(ii) $D + \bar{D}$ = ... [1]

(b) Either using a Karnaugh map or the rules of Boolean algebra simplify the following expression as much as possible. [4]

$$Q = \bar{D}.\bar{C}.B.\bar{A} + C.B.A + \bar{D}.C.\bar{B}.\bar{A} + C.\bar{B}.A + \bar{D}.C.B.\bar{A}$$

.....

.....

.....

.....

.....

DC \ BA	00	01	11	10
00				
01				
11				
10				

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [2]

$$Q = \overline{(\overline{B.\bar{A}}).A}$$

.....

.....

.....

Examiner only

6. *(a)* Convert the number 237 into: [2]

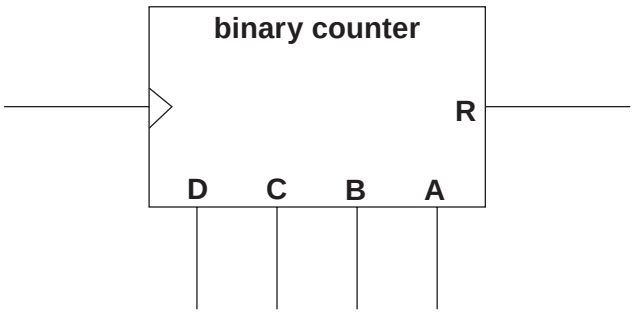
(i) binary;

.....

(ii) BCD.

.....

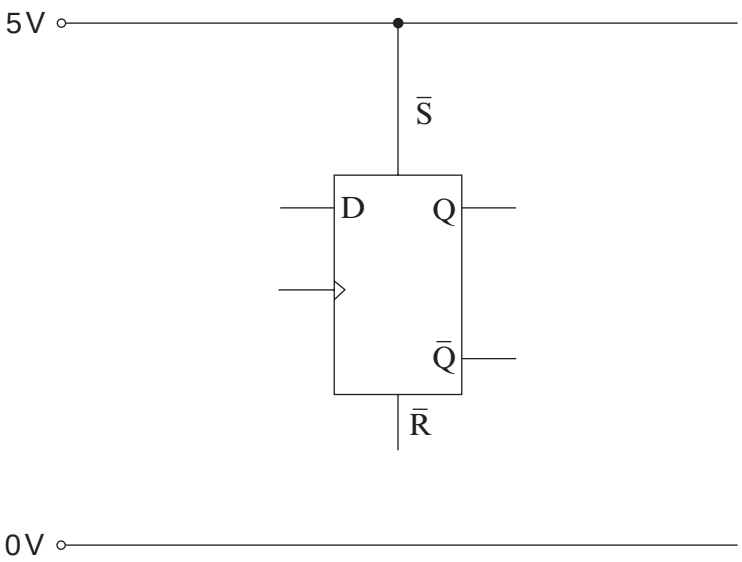
(b) The counter in the following diagram is a 4-bit **binary** counter. Output D is the most significant bit.



Complete the diagram to convert the counter into a BCD counter. [2]

Examiner only

7. A rising-edge-triggered D-type flip flop is shown below.



SET and RESET are active low.

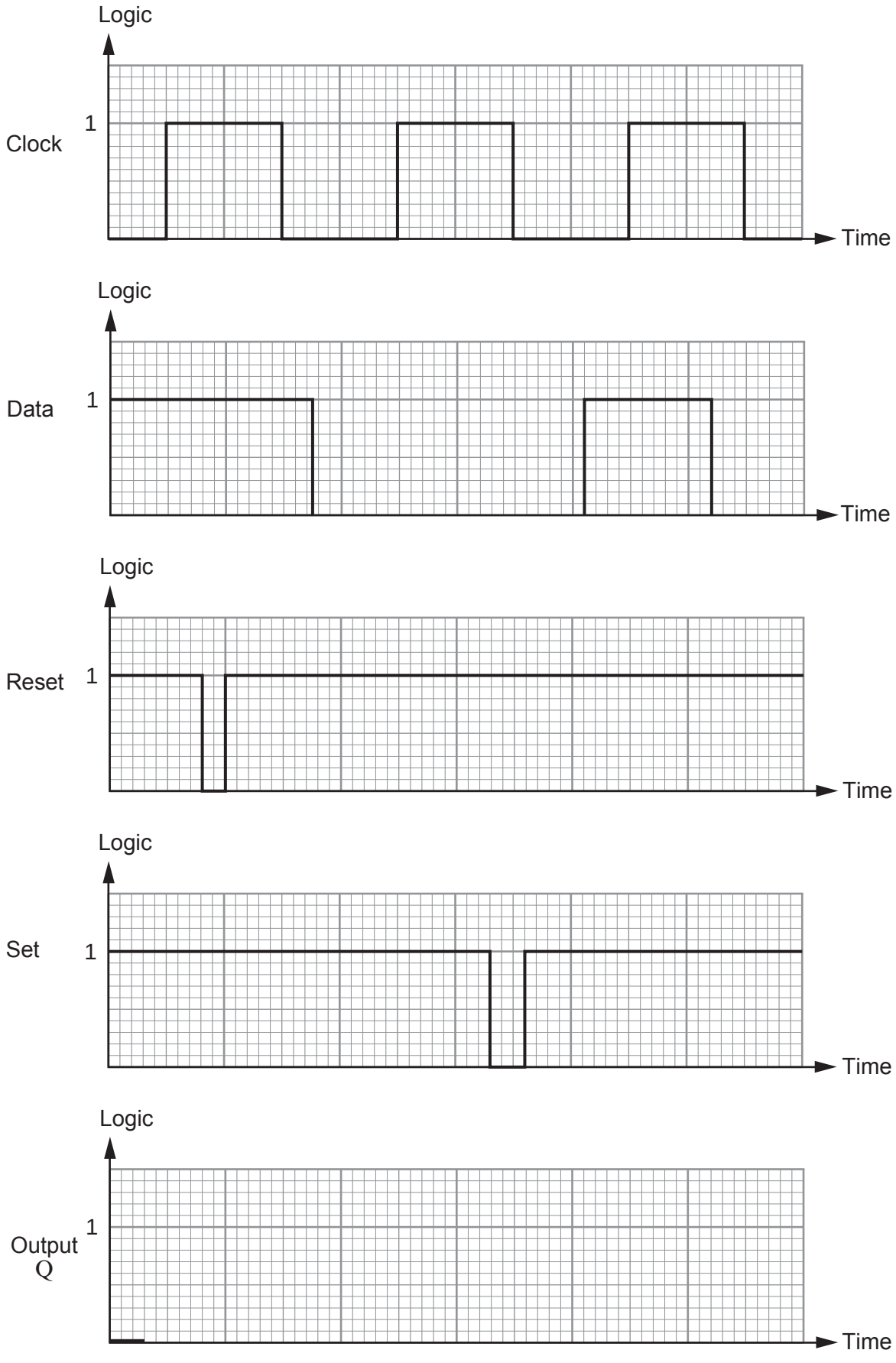
(a) What happens to $\overline{Q}$ if $\overline{R}$ is taken to logic 0? [1]

.....

.....

Examiner only

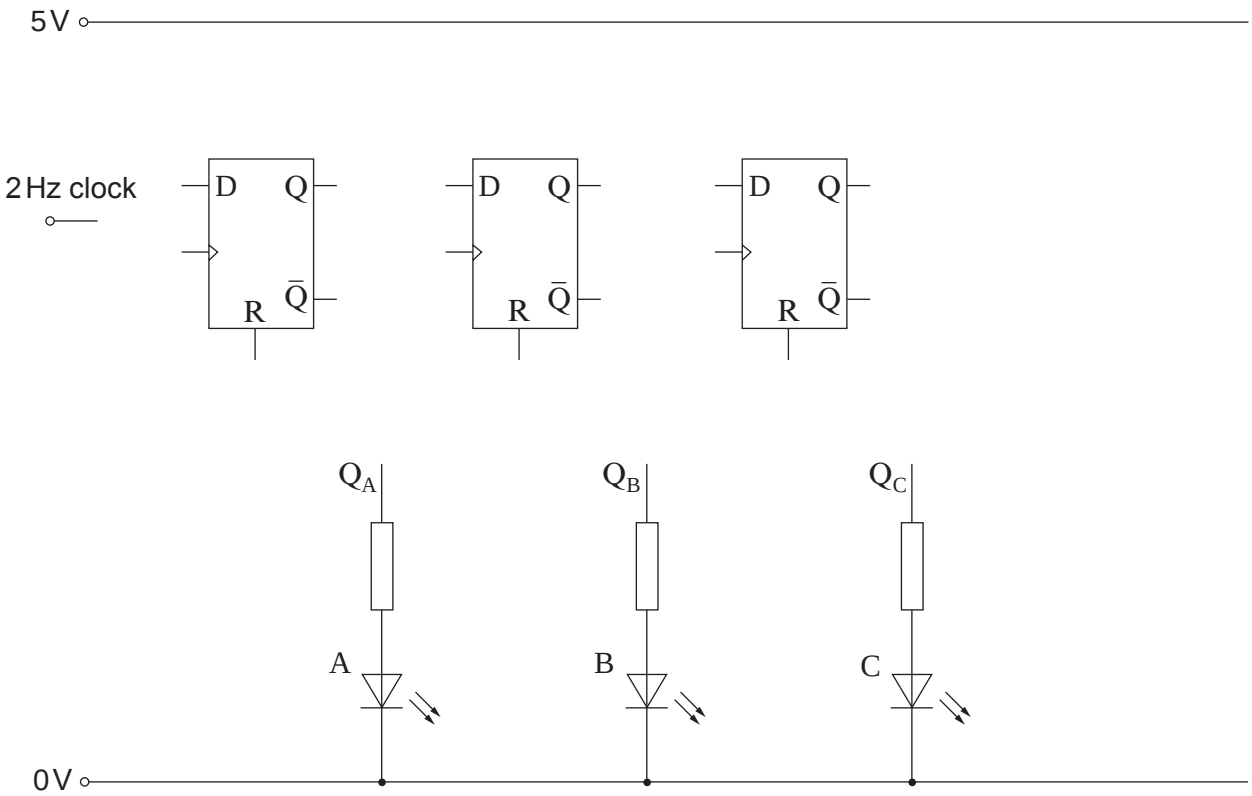
(b) The signals shown in the timing diagrams below are applied to the D-type. Complete the timing diagram for output Q. [4]



Examiner only

8. A system counts pulses and displays the count in binary on 3 LEDs, A, B and C (msb).

(a) Complete the diagram to show how three rising-edge-triggered D-type flip-flops can be connected to make a 3-bit up-counter. [3]



(b) Add the necessary components to the diagram such that the system can be manually **reset** with the press of a switch. [2]

(c) (i) How many pulses does the 2 Hz clock produce in 60 seconds? [1]

.....

(ii) How many times does LED **C** flash in 60 seconds? [1]

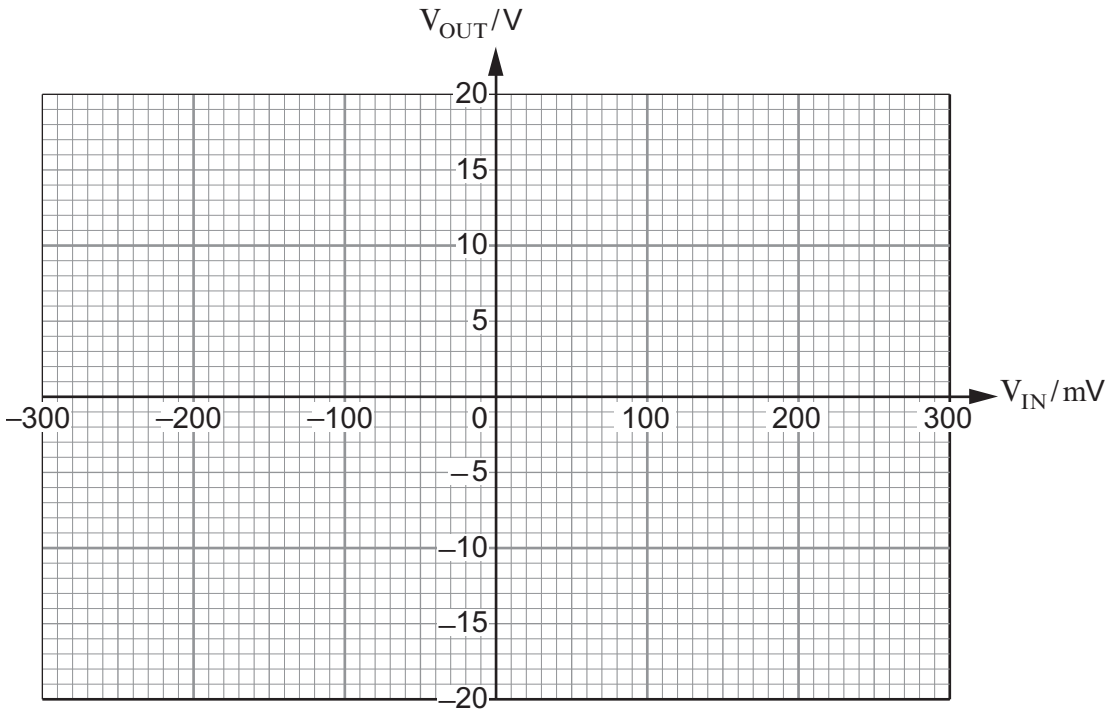
.....

Turn over.

Examiner only

9. A voltage amplifier is designed to have a voltage gain of -75. It uses an op-amp of gain-bandwidth product 3.6 MHz and it saturates at ± 18 V.

(a) Draw the voltage transfer characteristic of this voltage amplifier for input voltages between ± 300 mV. [3]

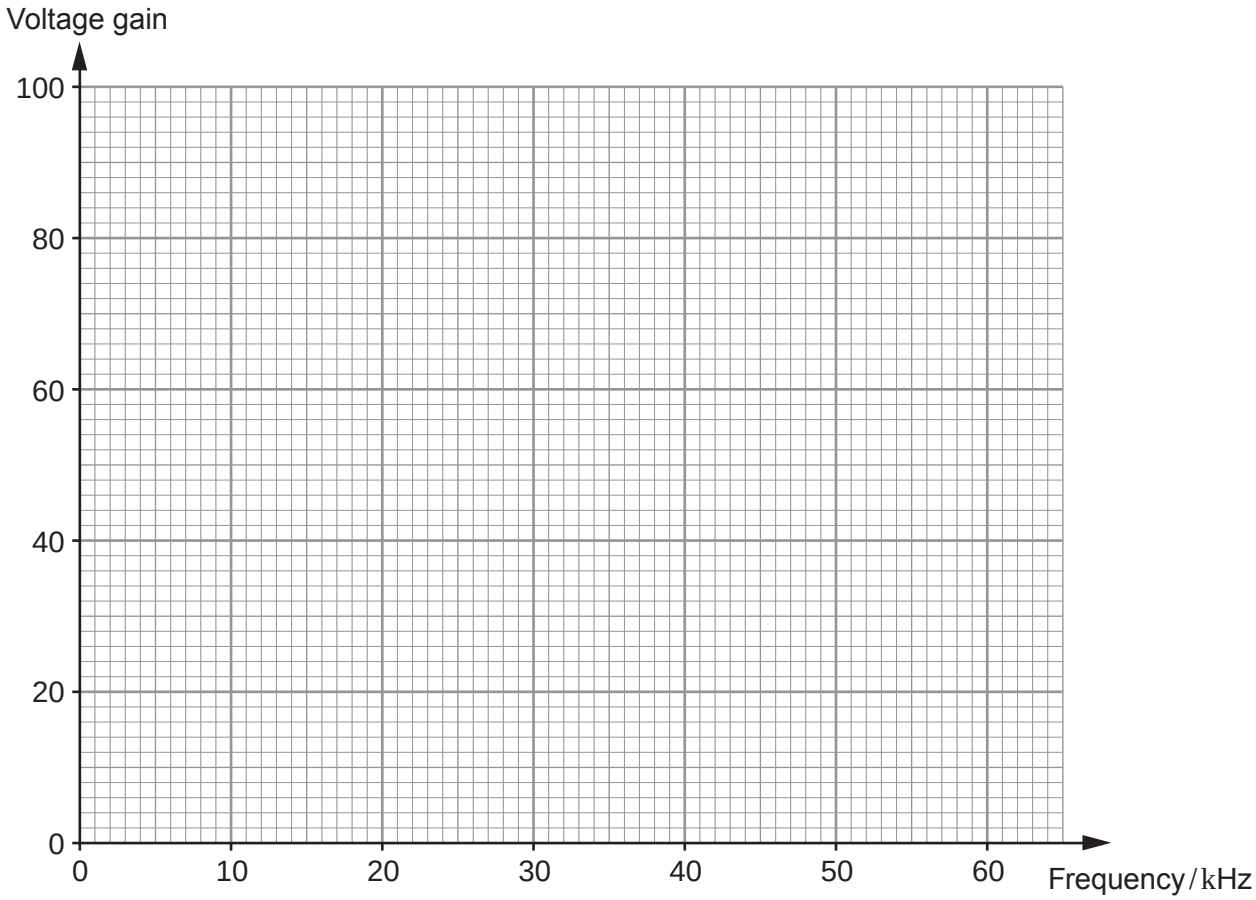


Examiner only

(b) (i) Calculate the bandwidth for a voltage gain of –75. [1]

.....

(ii) Use the axes provided to draw the frequency response of this amplifier. [2]

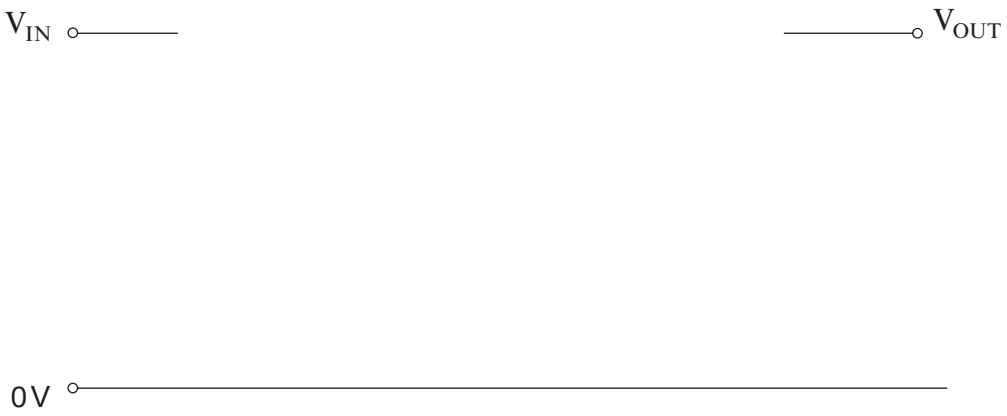


Turn over.

Examiner only

(c) This voltage amplifier can be constructed using an operational amplifier and other components.

(i) Complete the circuit diagram for this voltage amplifier. [3]



(ii) Label the circuit diagram with suitable resistor values to give the amplifier a voltage gain of –75. (Resistor values must be 1 $k\Omega$ or greater.) [2]

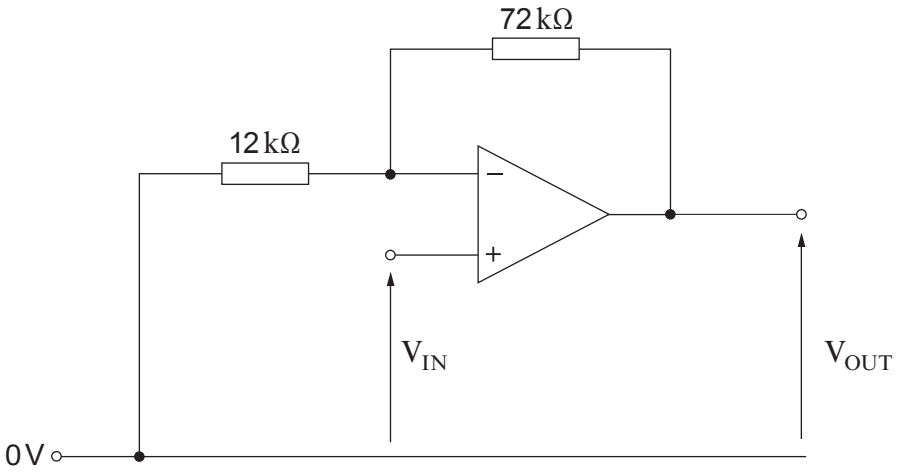
.....

.....

.....

Examiner only

10. The following diagram shows an op-amp set up as a voltage amplifier.



An extract from the data sheet for the op-amp is given below. The op-amp is powered from a ± 14 V supply.

Parameter	**Value**
Open-loop gain	3.0×10^5
Input impedance	$2.0 \times 10^{12} \Omega$
Saturation voltage	± 13.5 V
Slew rate	6 V μs^{-1}
Gain-bandwidth product	5 MHz

(a) Calculate the voltage gain of this amplifier. [1]

.....

(b) What is the input impedance of this voltage amplifier? [1]

.....

Turn over.

Examiner only

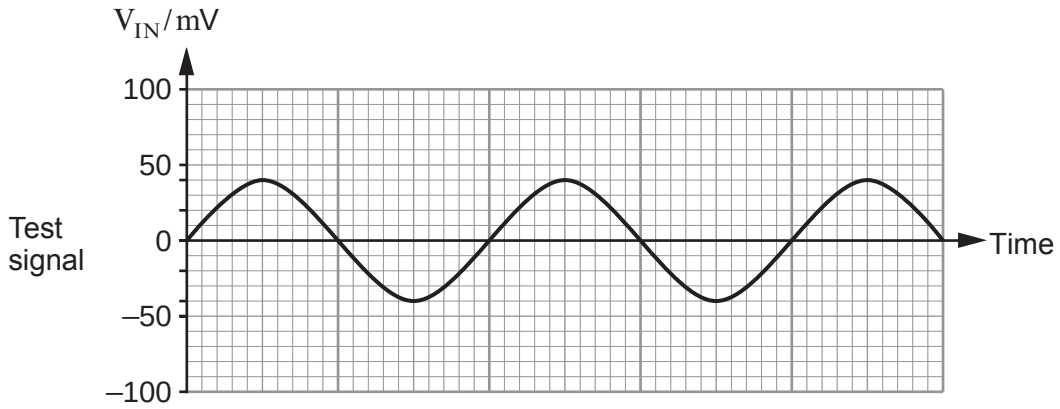
The amplifier is modified to have a voltage gain of 9.

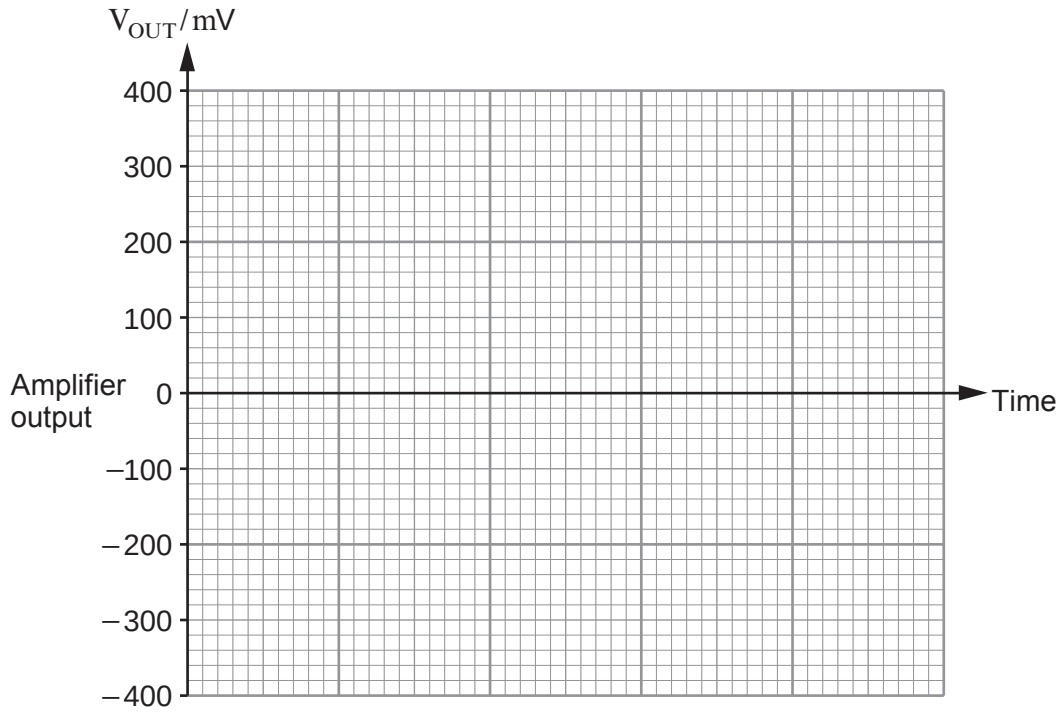
(c) A test signal of amplitude 40 mV is applied to the input.

(i) Calculate the amplitude of the output voltage. [1]

.....

(ii) Complete the graph to show the output voltage. Label the peak voltage. [2]





Examiner only

(d) What is the maximum amplitude of the input voltage, which does not produce clipping distortion? [1]

.....

.....

(e) In response to a large step input, the output of the op-amp changes from –13.5 V to + 13.5 V. Calculate the time taken for this change, giving the appropriate unit. [2]

.....

.....

END OF PAPER