Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS – ET1

A.M. MONDAY, 21 January 2013

1¼ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**5**	
2.	**2**	
3.	**7**	
4.	**8**	
5.	**11**	
6.	**7**	
7.	**8**	
8.	**12**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

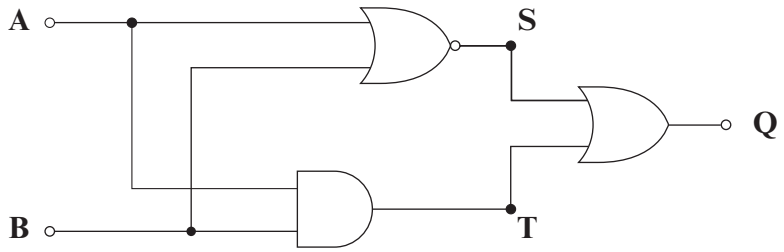
Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

Examiner only

1. The diagram below shows a logic system.



(a) Complete the truth table for the signal at points S, T and Q. [3]

B	A	S	T	Q
0	0			
0	1			
1	0			
1	1			

(b) (i) Name the single gate that can replace the combination of gates above. [1]

.....

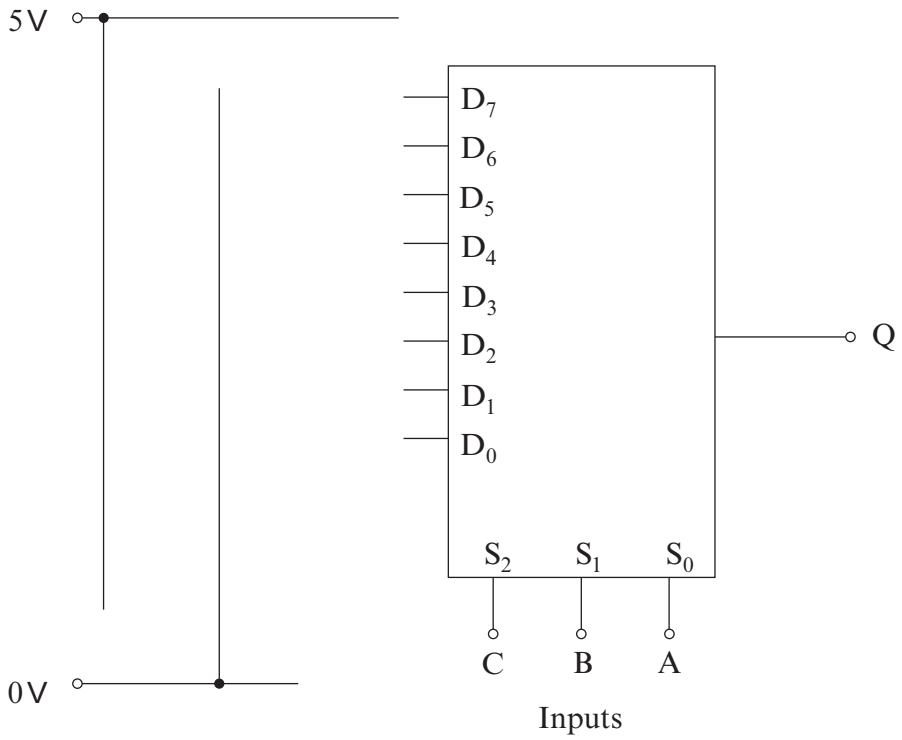
(ii) Draw the logic symbol for this gate. [1]

Turn over.

Examiner only

2. Multiplexers can be used as programmable logic systems. Complete the diagram to show how the 8:1 multiplexer can be used to create the output Q of the truth table. The input S_2 is the **most significant** select input. [2]

C	B	A	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



Examiner only

3. *(a)* Simplify the following Boolean expression.

$\overline{A}.0$ = ... [1]

(b) A Karnaugh map is shown below.

DC \ BA	00	01	11	10
00	1	0	1	1
01	0	0	1	0
11	0	0	1	0
10	1	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show on the Karnaugh map, any groups that you have created in producing this expression. [3]

Q = ...

.....

.....

(c) Apply DeMorgans theorem to the following expression and simplify the result. [3]

$$Q = \overline{A.B + \overline{A}}$$

.....

.....

.....

.....

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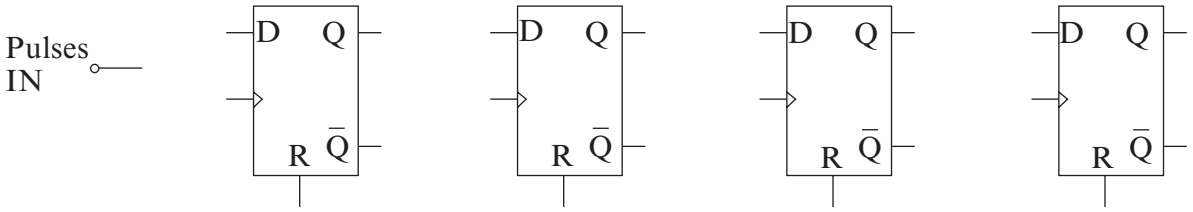
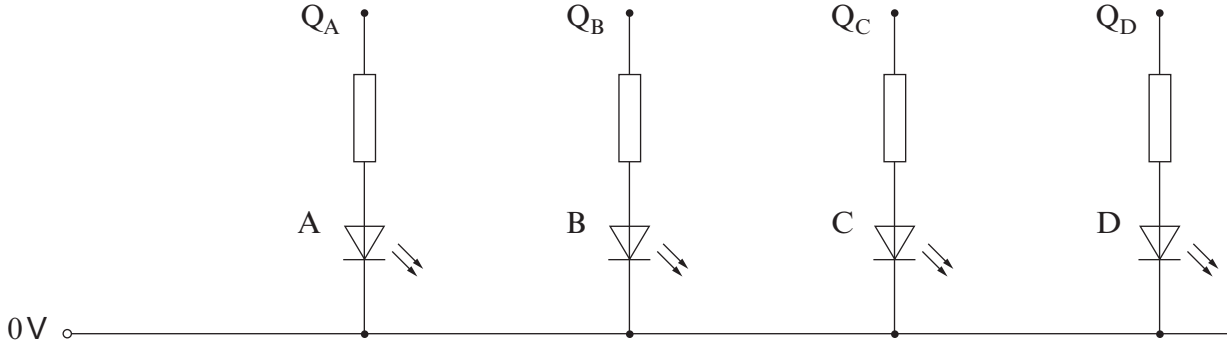
4. A system counts pulses and displays the count in binary on 4 LEDs (A, B, C and D).

(a) Complete the diagram for the 4-bit binary up counter. The least significant bit of the counter must be connected to the LED labelled A. [3]





(b) On the circuit diagram add a logic gate and the connections necessary to make the counter reset on the 10th clock pulse. [3]

(c) Initially all the LEDs are OFF.

(i) How many pulses have been counted if LEDs B and C are on and LEDs A and D are off?

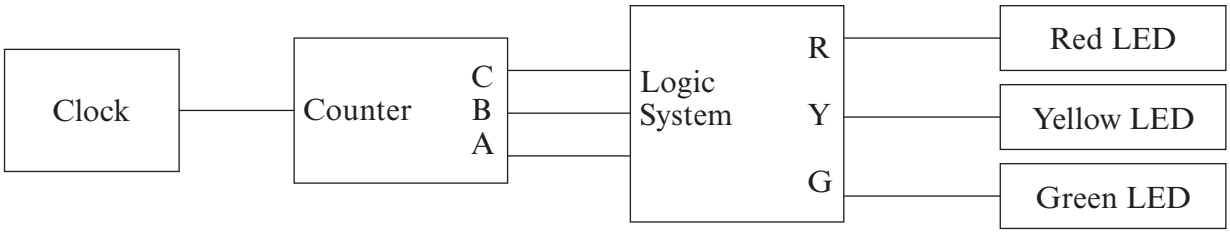
Number of pulses = ... [1]

(ii) What will be the logic levels of the following outputs after 9 pulses?

Q_A = ... Q_B = ... Q_C = ... Q_D = ... [1]

Examiner only

5. Two students design different light sequencers based on the following block diagram.



(a) The first student has a logic system specified by the following Boolean expressions:

$R = \overline{B.A}$

$Y = \overline{B}$

$G = \overline{C}.B + C.\overline{B}.\overline{A}$

Complete the truth table below to show the sequence of outputs produced. [3]

Clock Pulse	C	B	A	R	Y	G
0	0	0	0			
1	0	0	1			
2	0	1	0			
3	0	1	1			
4	1	0	0			
5	1	0	1			
6	1	1	0			
7	1	1	1			

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(b) The second student simulates traffic lights using the following truth table.

Clock Pulse	C	B	A	R	Y	G
0	0	0	0	1	0	0
1	0	0	1	1	0	0
2	0	1	0	1	0	0
3	0	1	1	1	1	0
4	1	0	0	0	0	1
5	1	0	1	0	0	1
6	1	1	0	0	0	1
7	1	1	1	0	1	0

The clock frequency is 0.1 Hz.

(i) Use the table to determine for how long output R is at logic 1. [1]

.....

(ii) Use the table to write down the Boolean expressions for outputs R and Y in terms of inputs A, B and C. [1]

R .....

Y .....

(iii) The student has **partially** simplified the G output to obtain

$$G = C.\overline{A} + C.\overline{B}.A$$

Using either a Karnaugh map or Boolean algebra simplify the expression for G. [3]

.....

.....

.....

.....

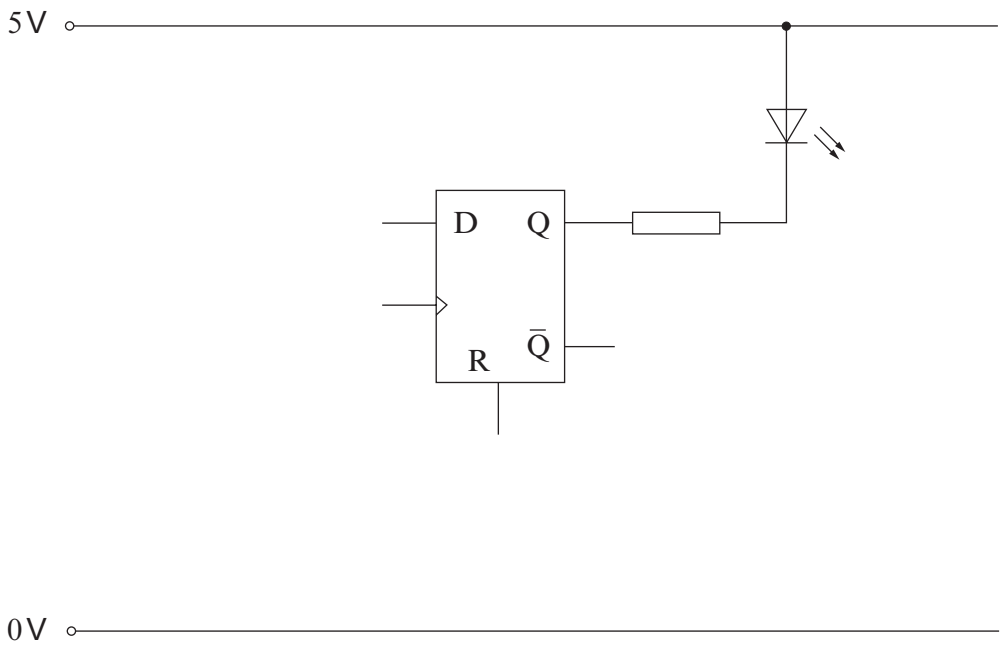
C \ BA	00	01	11	10
0				
1				

Examiner only

(iv) Design a suitable logic system using logic gates. Complete the following diagram with your design. [3]

Examiner only

6. The diagram shows a *rising-edge triggered* D-type flip-flop. R is *active high*.



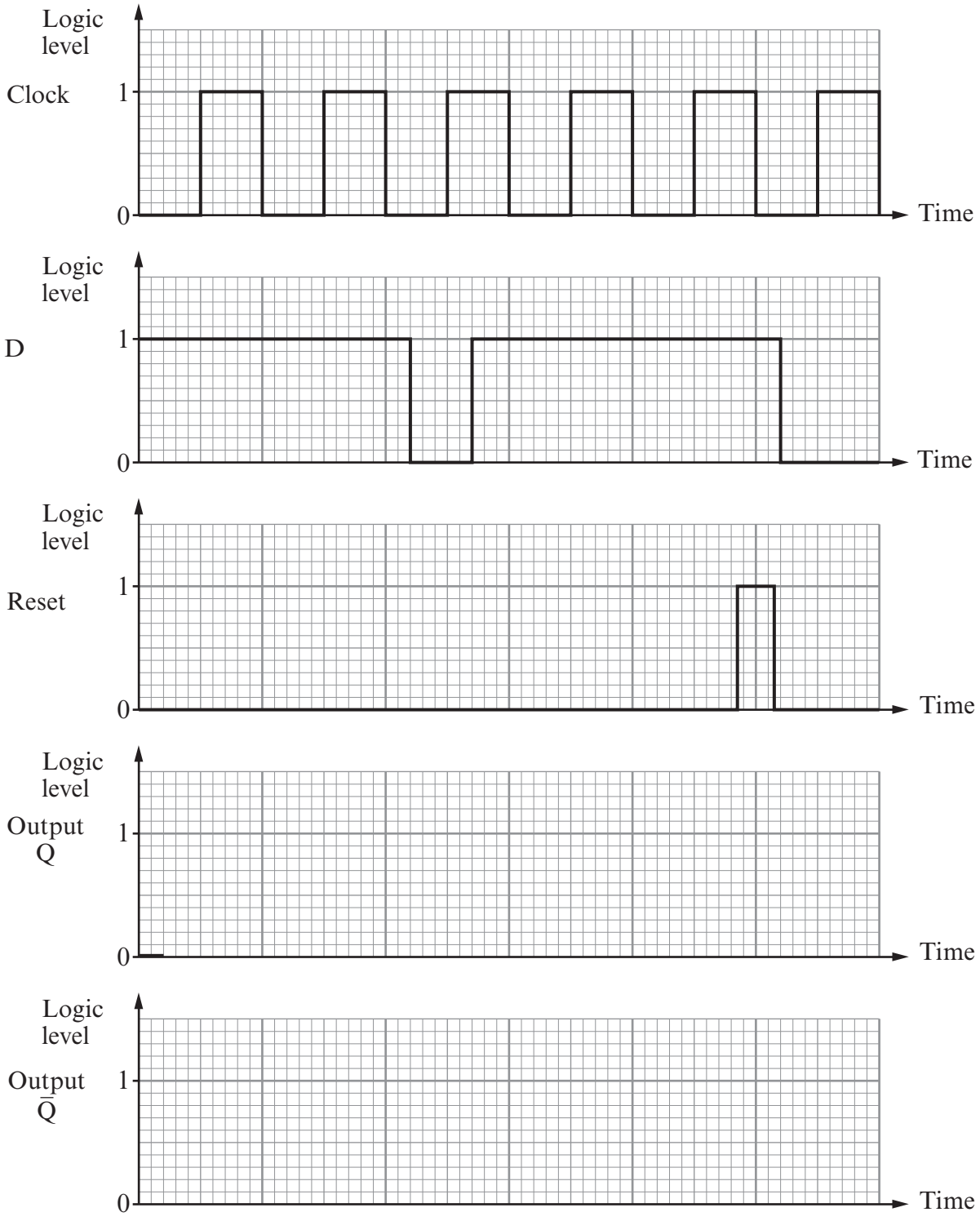
(a) Add the necessary components to the diagram such that the D-type can be **reset** with the momentary press of a switch. [2]

(b) Complete the following sentence. [1]

When the D-type is reset the output Q will be at logic ..... and the LED will be ..... .

Examiner only

(c) The signals shown in the timing diagrams below are applied to the *rising-edge triggered* D-type. Complete the timing diagram for the outputs Q and $\overline{Q}$. [4]
The RESET is *active high*.



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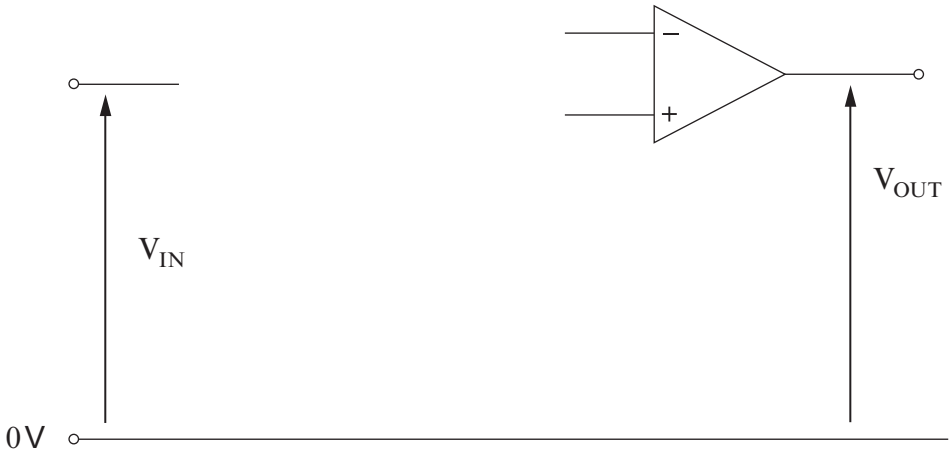
7. *(a)* Complete the circuit diagram for an inverting voltage amplifier. [3]



(b) Label the circuit diagram with suitable resistor values to give an input impedance of 10 kΩ and a voltage gain of –120. [2]

.....

.....

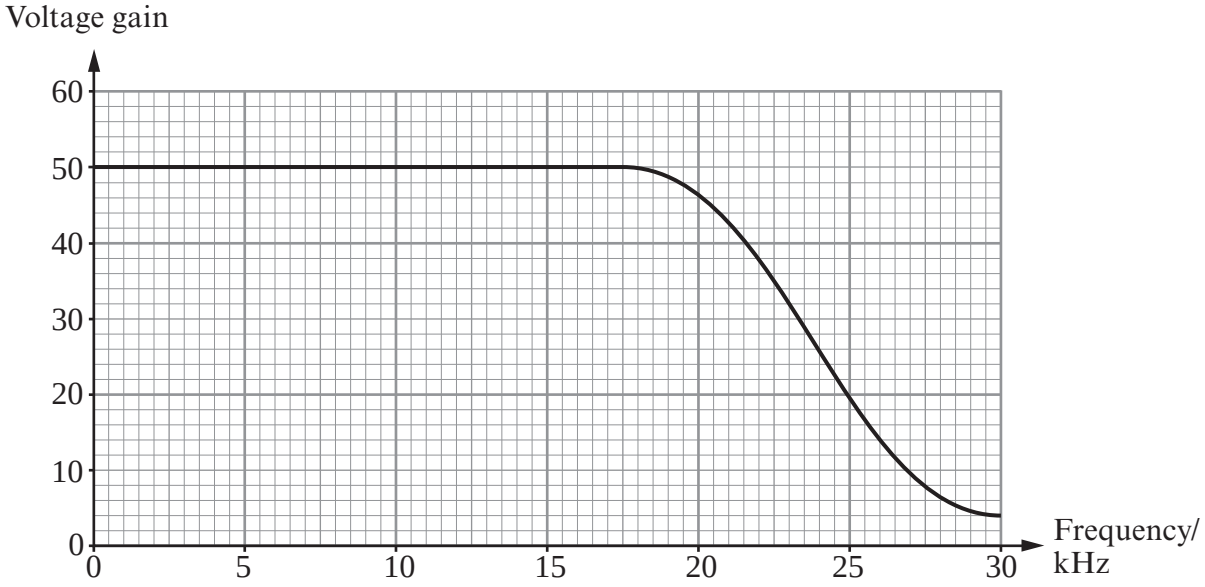
(c) How could the input impedance of the amplifier be changed without changing the gain? [1]

.....

.....

Examiner only

(d) Another amplifier has the frequency response shown below. Use the graph to estimate the bandwidth of this amplifier. Show **on the graph** how you obtained your result. [2]



Bandwidth = ... kHz.

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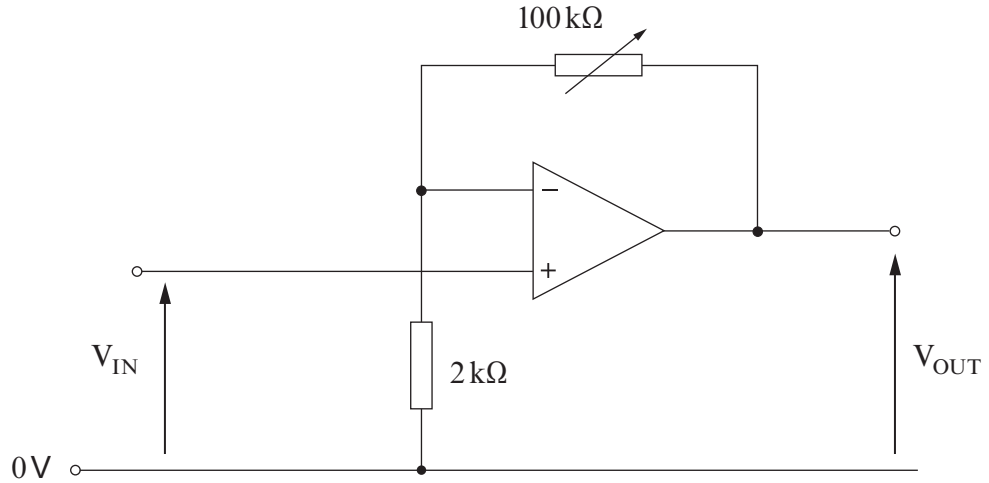
8. An extract from the data sheet of an op-amp is shown in the following table.

Parameter	Value
Input Impedance	10 MΩ
Output Impedance	100 Ω
Open Loop Gain	10^6
Gain Bandwidth Product	1.2 MHz
Slew rate	$5.0\,V\,\mu s^{-1}$

The circuit diagram shows the op-amp set up as a voltage amplifier. The *variable resistor* allows the user to change the gain. The value of this resistor can be altered from 0 to 100 kΩ.



The op-amp is powered from a ± 15 V supply and saturation occurs at ± 14 V.

(a) What is the input impedance of this amplifier? [1]

.....

(b) Calculate the maximum and minimum voltage gain of the amplifier. [2]

Maximum gain = ...

Minimum gain = ...

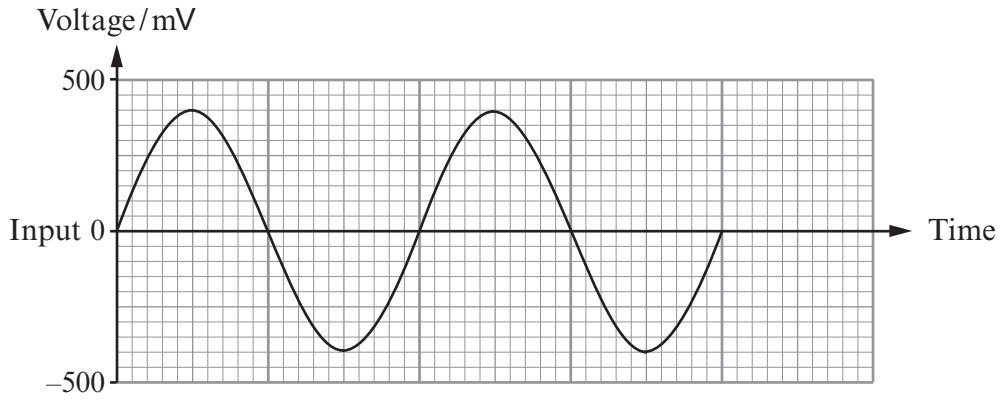
(c) (i) The variable resistor is adjusted to give a voltage gain of 30. Calculate the bandwidth of the amplifier with this gain. [2]

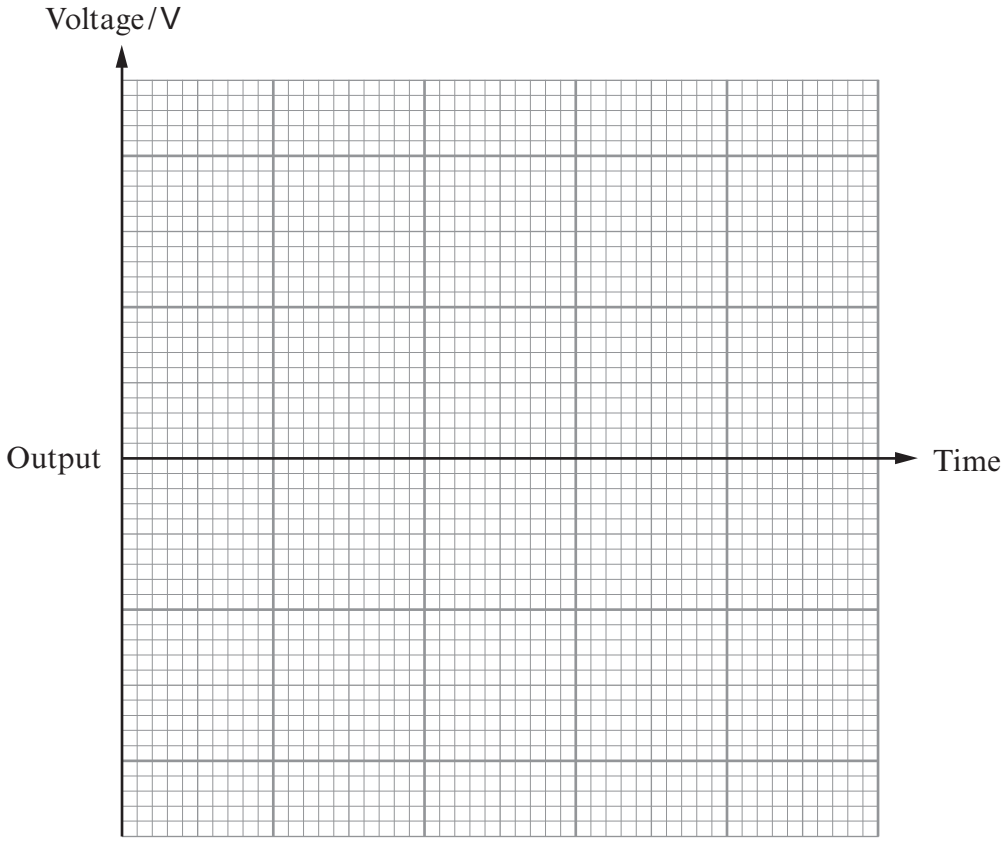
.....

.....

Examiner only

(ii) With the voltage gain set to 30 the following signal is applied to the input. Draw the output signal on the axes provided. Label important voltage values on the axes. [3]





(iii) What would be the maximum input voltage that would avoid clipping distortion? [1]

.....

.....

TURN OVER FOR THE REST OF THE QUESTION

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(d) (i) Calculate the time taken for the output to change from 0 V to 14 V in response to a large step-change in input voltage. Give an appropriate unit. [2]

.....

.....

(ii) Give one advantage of having a high slew rate. [1]

.....

.....

END OF PAPER