Surname	Centre Number	Candidate Number
Other Names		2

GCE A level

1145/01

ELECTRONICS – ET5

A.M. WEDNESDAY, 12 June 2013

1½ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**6**	
2.	**12**	
3.	**8**	
4.	**8**	
5.	**10**	
6.	**10**	
7.	**7**	
8.	**9**	
Total	**70**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 70.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Alternating Voltages $V_o = V_{rms}\sqrt{2}$

Silicon Diode $V_F \approx 0{\cdot}7\,V$

Operational amplifier

$G = -\dfrac{R_F}{R_{IN}}$ Inverting amplifier

$G = 1 + \dfrac{R_F}{R_1}$ Non-inverting amplifier

$V_{OUT} = V_{DIFF}\left(\dfrac{R_F}{R_1}\right)$ Difference amplifier

$V_{OUT} = -R_F\left(\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}\right)$ Summing amplifier

$V_L \approx V_Z\left(1 + \dfrac{R_F}{R_1}\right)$ Stabilised power supply

Emitter follower $V_{OUT} = V_{IN} - 0{\cdot}7\,V$

Filters

$f_b = \dfrac{1}{2\pi RC}$ Break frequency for high pass and low pass filters

$X_C = \dfrac{1}{2\pi fC}$ Capacitive reactance

Thyristor phase control

$\phi = \tan^{-1}\dfrac{R}{X_C}$

$\tan\phi = \dfrac{R}{X_C}$

Signal conversion $\text{resolution} = \dfrac{\text{i/p voltage range}}{2^n}$ ADC

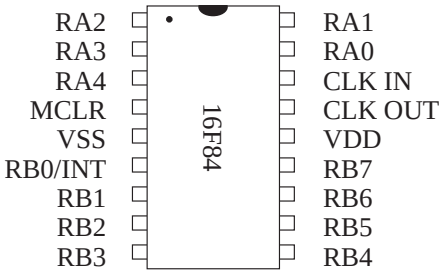
Power amplifier $P_{MAX} = \dfrac{V_S^2}{8R_L}$ where V_S is the rail-to-rail voltage

PIC Information

The PIC programs include 'equate' statements that define the following labels:

Label	Description
PORTA	input / output port A
PORTB	input / output port B
TRISA	the control register for port A
TRISB	the control register for port B
STATUS	the status register
INTCON	the interrupt control register
W	the working register (= h '0')
F	the file register (= h '1')
RP0	the register page selection bit 0
Z	the zero flag status bit
GIE	the global interrupt controller bit
INTE	the external interrupt enable bit

Pin out for 16F84 PIC IC:



List of commands:

Mnemonic	Operands	Description
bcf	f, b	Clear bit b of file f
bsf	f, b	Set bit b of file f
btfss	f, b	Test bit b of file f, skip next instruction if bit is set
call	k	Call subroutine k
clrf	f	Clear file f
goto	k	Branch to label k
movf	f, d	Move file f (to itself if d = 1, or to working register if d = 0)
movlw	k	Move literal k to working register
movwf	f	Move working register to file f
retfie		Return from interrupt service routine and set global interrupt enable bit GIE

Comparison of TASM and MPASM languages:

Version		TASM	MPASM
Number system notation	Decimal	153	d'153'
	Hex	$2B	h'2B' or 0x2B
	Binary	%10010110	b'10010110'
Opcode Notation		.equ	equ
		.org	org
		.end	end
		label:	label

Structure of the INTCON register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF

Structure of the STATUS register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRP	RP1	RP0	TO	PD	Z	DC	C

Turn over.

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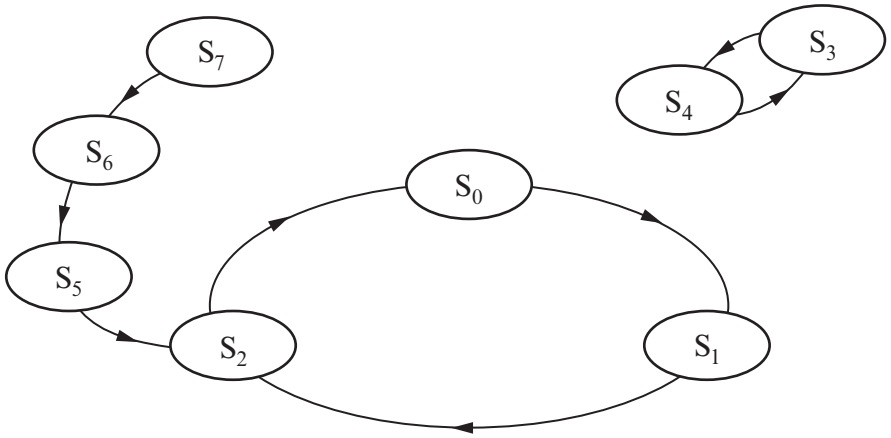
Examiner only

1. The state diagram for a sequence generator is shown in the diagram:



(a) How many states are in the main sequence? ..... [1]

(b) (i) What is meant by the term *unused state*? [1]

.....

.....

(ii) What is meant by the term *stuck state*? [1]

.....

.....

(c) (i) Identify **one** unused state that is not a *stuck state*. ..... [1]

(ii) Identify all the *stuck states*. [1]

.....

(iii) When are *stuck states* likely to be a problem? [1]

.....

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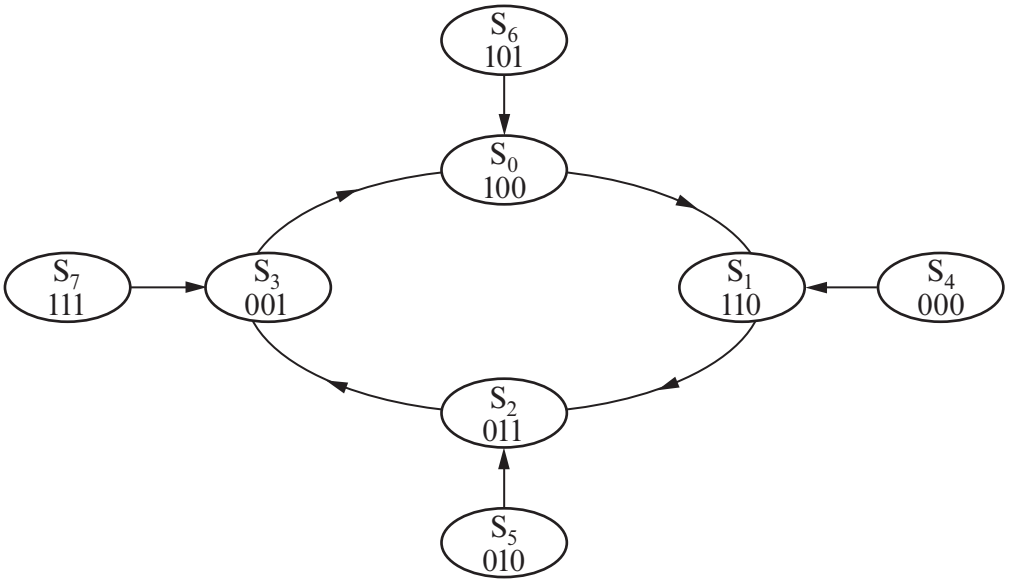
Turn over.

Examiner only

2. A sequence generator is specified by the following state diagram:



(a) Use the information in the state diagram to complete the table. [4]

	Current Outputs			Next Outputs		
State	**C**	**B**	**A**	$\mathbf{D_C}$	$\mathbf{D_B}$	$\mathbf{D_A}$
0						
1						
2						
3						
4						
5						
6						
7						

(b) Use the table to deduce the simplest form of Boolean expressions linking $\mathbf{D_C}$, $\mathbf{D_B}$ and $\mathbf{D_A}$ to the outputs **C**, **B** and **A**. [3]

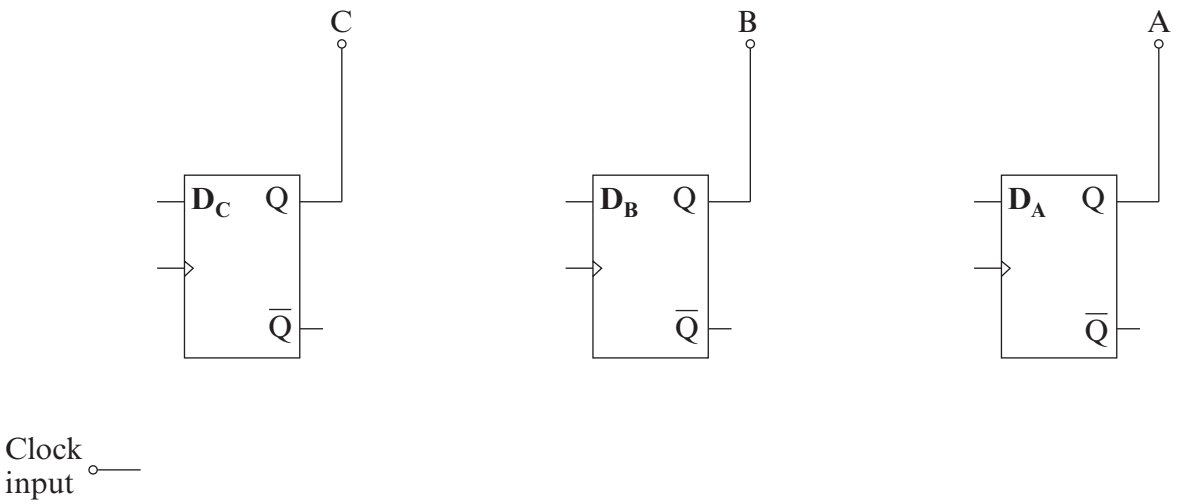
$\mathbf{D_C}$ = ...

$\mathbf{D_B}$ = ...

$\mathbf{D_A}$ = ...

Examiner only

(c) Complete the circuit diagram for this sequence generator.
(Credit will be given for using the minimum number of gates.) [5]



Examiner only

3. *(a)* The following code is written to the data direction registers of a PIC microcontroller:

```
bsf     STATUS,RP0
movlw   b '00100'
movwf   TRISA
movlw   b '11111111'
movwf   TRISB
bcf     STATUS,RP0
```

Describe the effect of this code on PORT A and PORT B of the microcontroller. [2]

PORT A .....

PORT B .....

(b) On page 3, the Information Sheet gives the structure of the INTCON register.

Complete the following instruction to enable the external interrupt on PORT B bit 0. [1]

```
movlw   b '_ _ _ _ _ _ _ _'
movwf   INTCON
```

Examiner only

(c) Complete the template provided below to write an Interrupt Service Routine, identified by the label *alarm*, that:

- saves the contents of the Working Register to the file Wtemp;
- clears the INTF bit in the INTCON register;
- lights an LED connected to bit 4 of PORT A, by setting the bit to logic 1;
- turns on a buzzer connected to bit 3 of PORT A, by setting that bit to logic 1;
- calls the delay subroutine called *fivesec*;
- switches off the LED and the buzzer;
- recovers the contents of the Working Register from the file Wtemp;
- returns to the main program and sets the Global Interrupt Enable bit at the same time. [4]

(The numbers in the left-hand column are line numbers in the program listing.)

```
101  alarm  .....  .....  ; save the contents of the Working Register
102         bcf    INTCON,1  ; reset the External Interrupt Flag
103         .....  .....  ; light the LED connected to bit 4 of PORT A
104         .....  .....  ; turn on the buzzer on bit 3 of PORT A
105         .....  .....  ; call the delay subroutine called fivesec
106         .....  .....  ; switches off the LED and the buzzer
107         .....  .....  ; recover the Working Register from Wtemp
108         .....        ; return to main program / re-enable interrupts
```

(d) Why is it necessary to save the contents of the Working Register when starting the Interrupt Service Routine? [1]

.....

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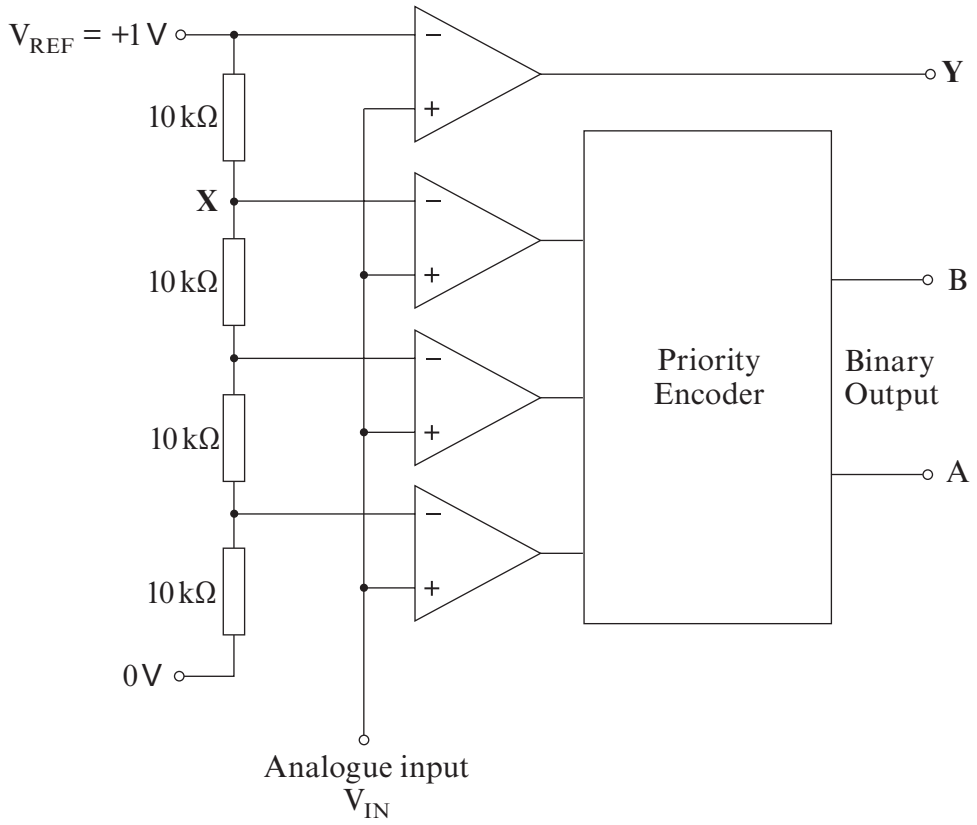
4. *(a)* The circuit diagram for a two-bit flash ADC is shown below:



(i) What is the voltage at input **X**? [1]

.....

(ii) What is the purpose of output **Y**? [1]

.....

(b) A **different** flash ADC has an input voltage range of 2 V and a three-bit output.

(i) Calculate the resolution of the new ADC. [1]

.....

(ii) What reference voltage V_{REF} will be needed? [1]

.....

(iii) How many resistors are needed in the resistor chain? [1]

.....

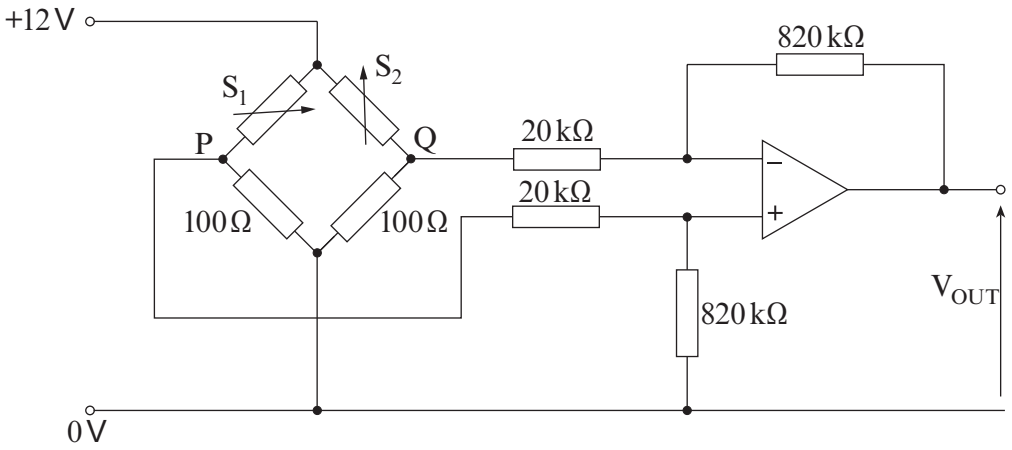
Examiner only

(iv) The outputs of the comparators are connected to inputs P, Q, R, S, T, U and V of the new priority encoder. Complete the table for the new priority encoder. [3]

Inputs							Outputs		
P	**Q**	**R**	**S**	**T**	**U**	**V**	**C**	**B**	**A**
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1

Examiner only

5. A bridge circuit is used to monitor strain in part of a crane when it is loaded. It uses two identical strain gauges, S_1 and S_2, and a difference amplifier.



Under test conditions, the strain gauge S_1 has a resistance of 121.5 Ω and S_2 has a resistance of 120.0 Ω.

(a) Explain why the strain gauges have different resistances. [1]

.....

.....

(b) Under these conditions, calculate:

(i) the voltage at point P (relative to 0 V); [1]

.....

(ii) the voltage at point Q (relative to 0 V); [1]

.....

(iii) the voltage gain of the difference amplifier; [1]

.....

(iv) the output voltage of the amplifier, V_{OUT}. [2]

.....

.....

.....

Examiner only

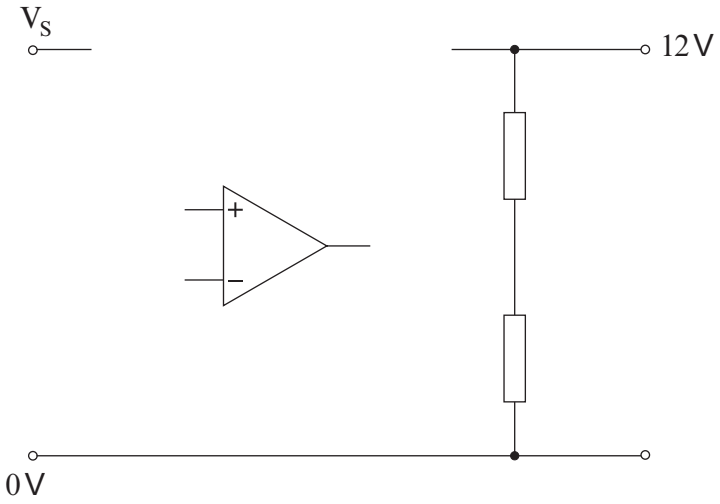
(c) Why is V_{OUT} unaffected by temperature variation? [1]

.....

.....

.....

(d) The 12V power supply is obtained from a voltage regulator. It consists of a zener diode, an emitter follower and a non-inverting amplifier. Complete the circuit diagram for this voltage regulator. [3]



Examiner only

6. *(a)* State **one** condition needed at the gate of a forward-biased thyristor to make it conduct. [1]

.....

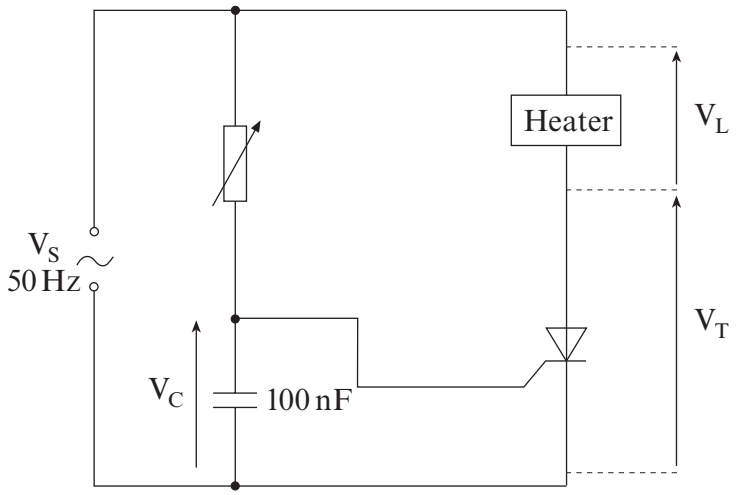
.....

(b) What is meant by the term *holding current* when related to a thyristor? [1]

.....

.....

(c) The circuit diagram shows a thyristor controlling the output of a heater, using phase control.



(i) Modify the circuit diagram by adding a diac so that it improves the rise-time of the gate signal. [1]

(ii) Calculate the phase angle between the power supply voltage, V_S, and the voltage across the capacitor, V_C, when the variable resistor is set to a resistance of 15 kΩ. [2]

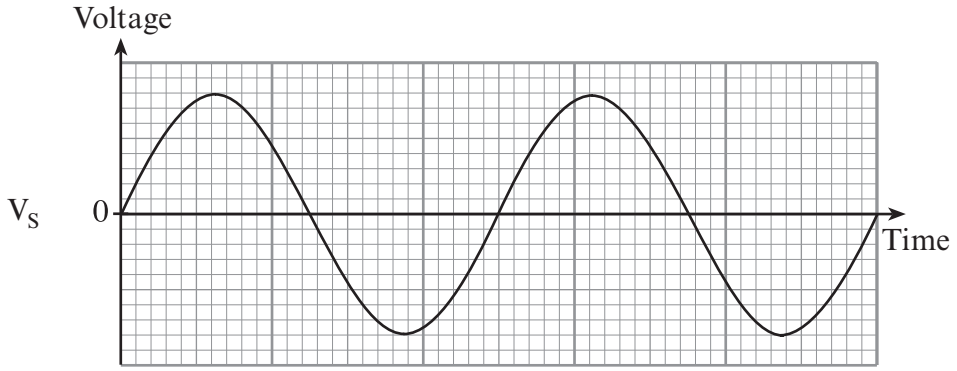
.....

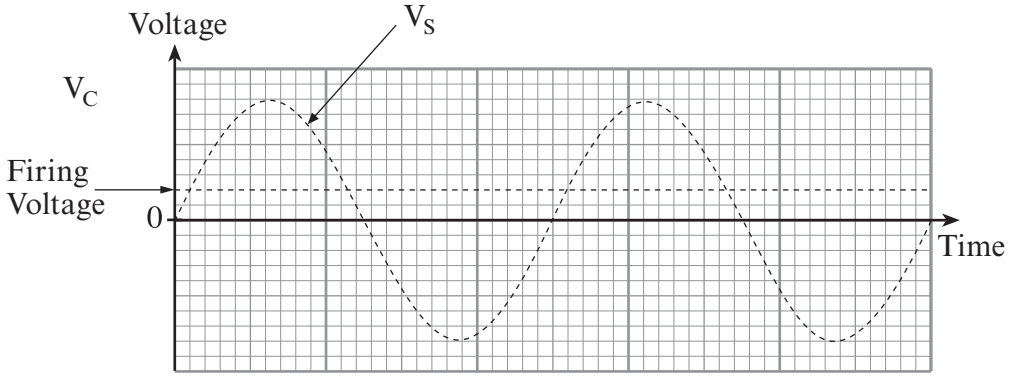
.....

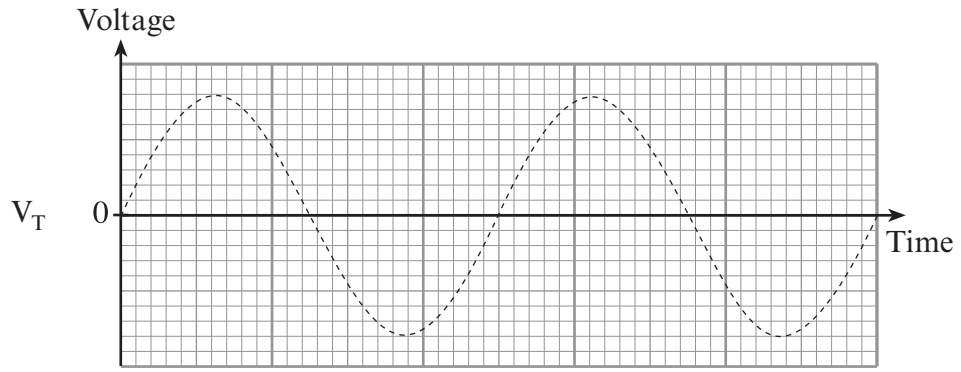
Examiner only

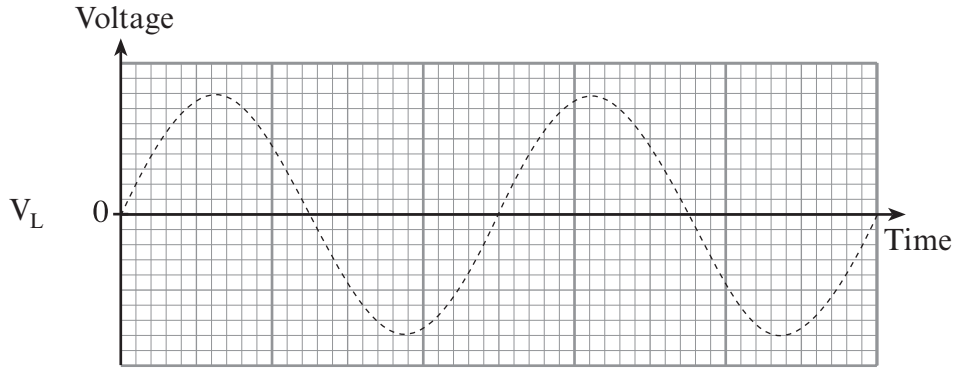
(iii) Use the axes and information given to sketch graphs of the following signals: [5]

- the voltage across the capacitor, V_C;
- the voltage across the thyristor, V_T;
- the voltage across the heater, V_L.



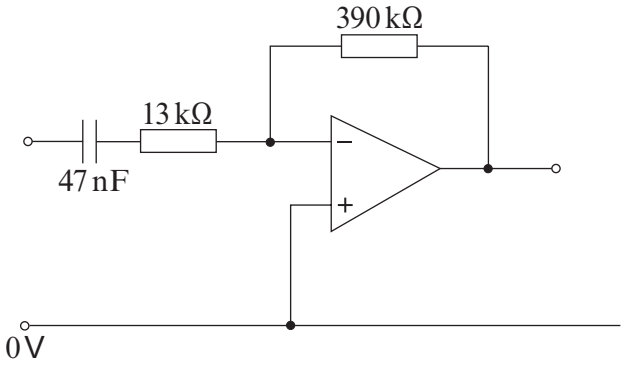






Examiner only

7. An audio system includes the following tone control circuit, based on an active filter.



(a) What type of filter is this? ..... [1]

(b) Calculate the break frequency of this filter. [3]

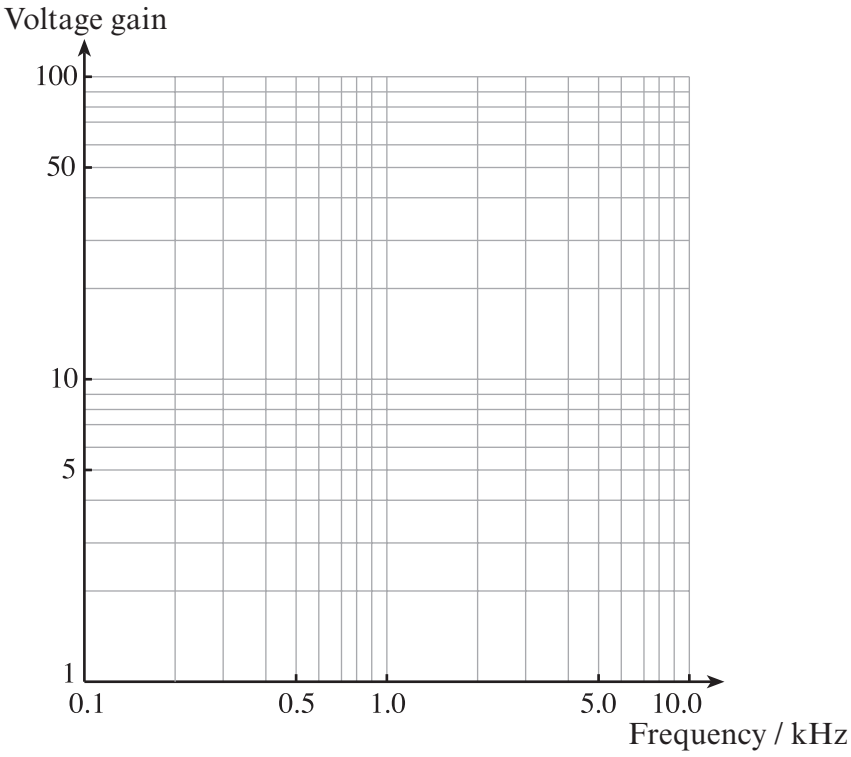
.....

.....

.....

.....

(c) Use the axes provided to sketch the frequency response of this filter. [3]



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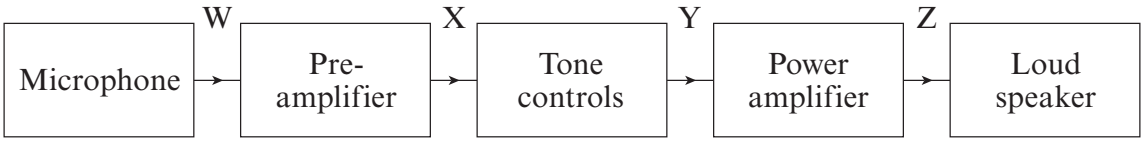
8. The block diagram for an audio system is shown below:

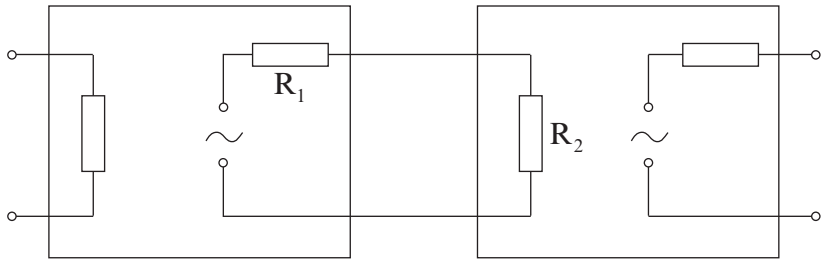


The links between sub-systems are labelled W, X, Y and Z.

(a) Which link(s) should be designed to maximise power transfer between sub-systems? [1]

.....

(b) The diagram shows the equivalent circuit for two sub-systems within this audio system:



What is the relationship between R_1 and R_2 in order to maximise power transfer between the sub-systems? [1]

.....

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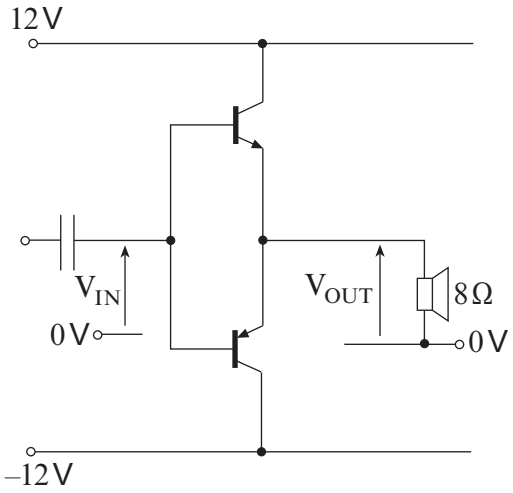
(c) A power amplifier circuit is shown below.



(i) Calculate the maximum power dissipation in the 8 Ω loudspeaker. [1]

.....

(ii) What is the advantage of this arrangement over an emitter follower which uses resistor bias to split a single rail power supply? [1]

.....

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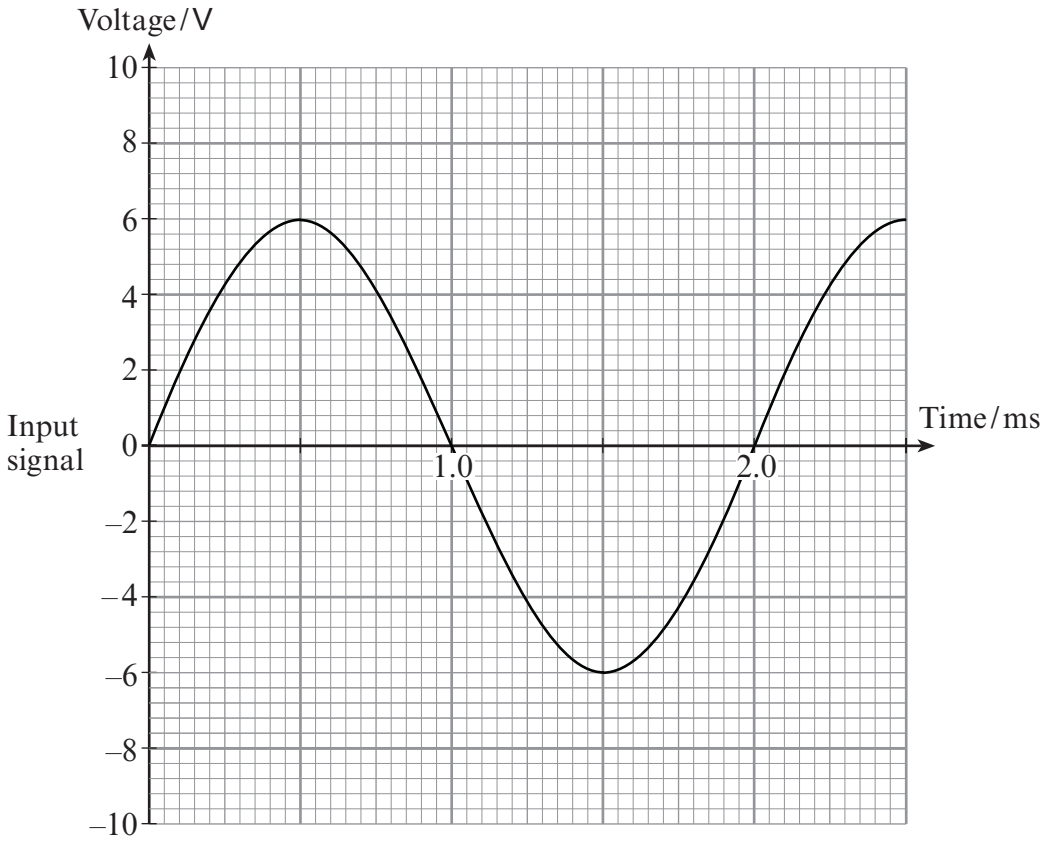
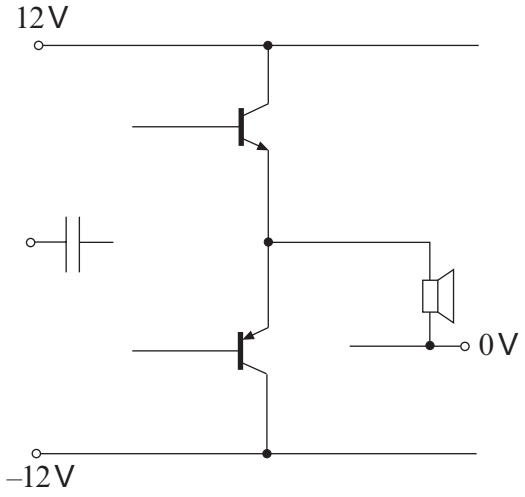
(iii) The graph shows a test signal applied to the power amplifier. On the same axes, sketch the signal, V_{OUT}. Ignore any reactive effects. [3]



(iv) The power amplifier can be modified to eliminate cross-over distortion.

Complete the circuit diagram to show this modification. [2]



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