GCE MARKING SCHEME

ELECTRONICS
AS/Advanced

SUMMER 2012

INTRODUCTION

The marking schemes which follow were those used by WJEC for the Summer 2012 examination in GCE ELECTRONICS. They were finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conferences were held shortly after the papers were taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conferences was to ensure that the marking schemes were interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conferences, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about these marking schemes.

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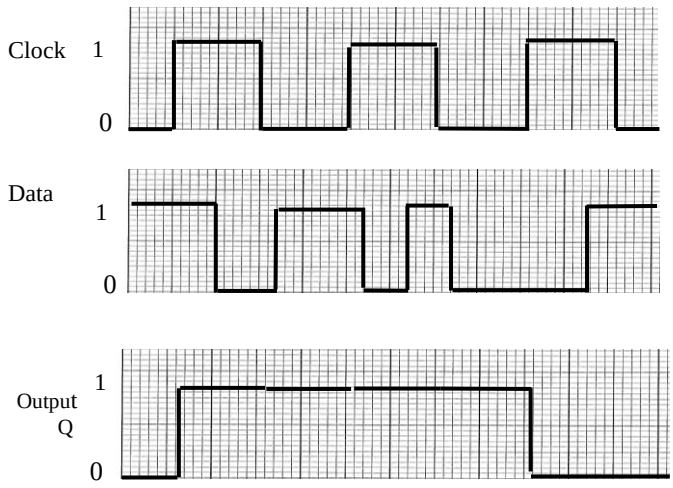
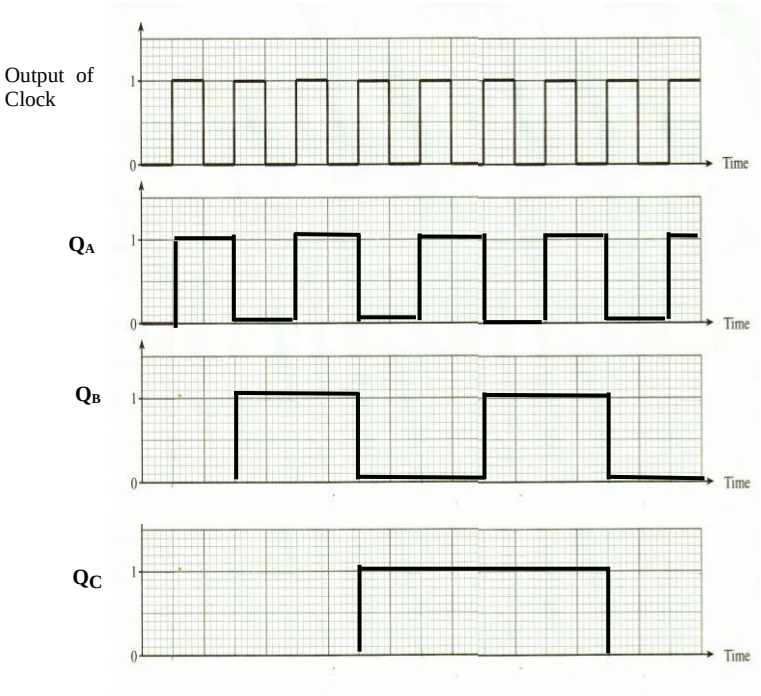
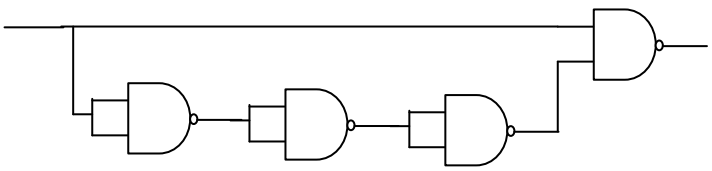
<table>
<tr><th colspan="3">Question</th><th>Marking details</th><th>Marks Available</th></tr>
<tr><td>1.</td><td>(a)</td><td>(i)</td><td>
<table>
<tr><td>B</td><td>A</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>$Q = B \oplus A$ or $\overline{B}.A + B.\overline{A}$</td><td>1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>NAND gate</td><td>1</td></tr>
<tr><td></td><td>(c)</td><td>(i)</td><td>
<table>
<tr><td>X</td><td>Y</td><td>W</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
One mark each correct column. ecf from a(i)
</td><td>2</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Logic gate EXNOR ecf from (c)(i) column Q (single gate)</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[6]</td></tr>
<tr><td>2.</td><td>(a)</td><td></td><td>Correct replacement of AND by NAND (1)
Correct replacement of NOR by NAND (1)
Correct replacement of OR by NAND (1)</td><td>3</td></tr>
<tr><td></td><td>(b)</td><td></td><td>Two pairs of redundant gates clearly identified and crossed out</td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td>[5]</td></tr>
</table>

Question			Marking details	Marks Available
3	*(a)*		To pull the input up [to logic 1 when the switch is open] **or** to prevent 'short circuiting' power supply when switches are pressed.	1
	(b)		Logic 1 **or** high (not 5 V)	1
	(c)		Logic 1 **or** high (not 5 V)	1
	(d)		X and Y to NOR gate or NOT X NOT Y to AND (1) Output of NOR gate and Pulse producer to AND (1) Output on AND to Q (1) (other correct solutions accepted)	3
				[6]
4	*(a)*	(i)	$\overline{A}$	1
		(ii)	$B.\overline{A} + B.\overline{B}$ (1) $B.\overline{A}$ (1)	2
	(b)		3 groups identified (including 2 groups of 4) (1) $Q = \overline{C}.B + \overline{D}.B.\overline{A} + .\overline{C}.\overline{A}$ (1 mark each correct term from map)	4
	(c)		$Q = \overline{B} + \overline{\overline{A}.B}$ $= \overline{B} + A.B$ $= \overline{B} + A$	3
				[10]

Question			Marking details	Marks Available
5.	*(a)*		<table><tr><th>A</th><th>B</th><th>X</th><th>Y</th></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr></table> Setting/resetting correct (lines 2+4) (1) Latching correct (lines 3+5) (1) Forbidden combination (line 6) (1)	3
	(b)		 $\overline{Q}$ is INVERSE of Q	2 1 **[6]**

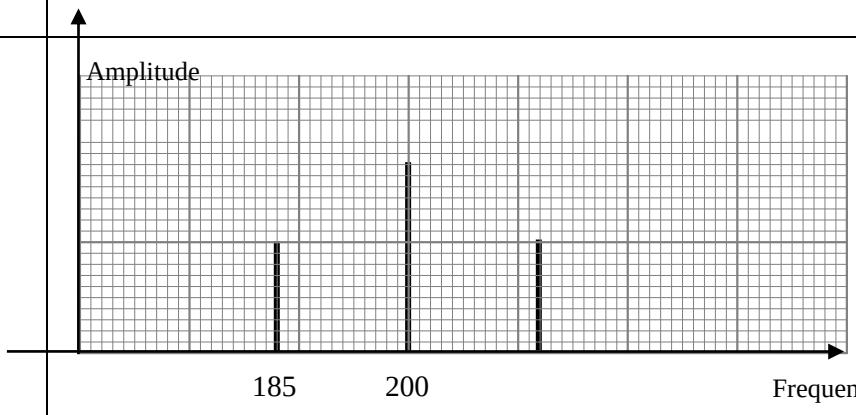
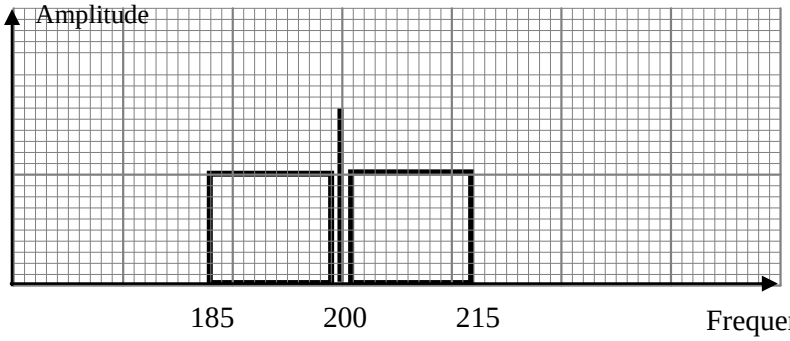
Question			Marking details	Marks Available
6.	*(a)*		500 k[Hz] or 0.5 M[Hz] or 500 000 [Hz]	1
	(b)		Output Q_C **or** $\overline{Q}_C$	1
	(c)			
			Q_A correct in all respects (1) Q_B and Q_C duration correct (1) Q_B and Q_C timing correct (1)	3
				[5]
7.	*(a)*	(i)		
			Odd no. of NAND inverters (1) Correct connections to 2-input NAND gate (1)	2
	(b)		Makes it edge-triggered	1
				[3]

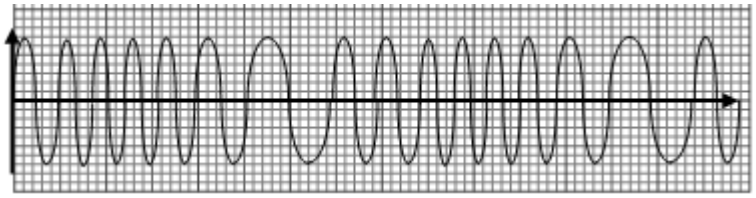
Question			Marking details	Marks Available
8.	*(a)*		<table><tr><th>Frequency/kHz</th><th>V_{IN}/V</th><th>V_{OUT}/V</th><th>Voltage gain</th></tr><tr><td>5</td><td>0.5</td><td>15.0</td><td>30.0</td></tr><tr><td>10</td><td>0.5</td><td>15.0</td><td>30.0</td></tr><tr><td>15</td><td>0.5</td><td>15.0</td><td>30.0</td></tr><tr><td>20</td><td>0.5</td><td>14.1</td><td>28.2</td></tr><tr><td>25</td><td>0.5</td><td>12.5</td><td>25.0</td></tr><tr><td>30</td><td>0.5</td><td>10.0</td><td>20.0</td></tr><tr><td>35</td><td>0.5</td><td>7.2</td><td>14.4</td></tr><tr><td>40</td><td>0.5</td><td>4.4</td><td>8.8</td></tr></table> Gain completely correct	1
	(b)		Suitable scales drawn Correctly plotted points Suitable line of best fit Allow ecf on all marking points from (a)	3
	(c)		Bandwidth measured at gain of 0.7 x 30 = 21 (1) or indicated on the graph 29 [kHz] (range 28.5-29.5) (1)	2
	(d)		GBWP = 29x30 = 870 (1) (Range 855 – 885) kHz (1) <u>unit mark</u> allow ecf from part (c)	2
				[8]
9.	*(a)*		<table><tr><th>High value (1)</th><th>Low value (1)</th></tr><tr><td>Input impedance Slew-rate Open loop gain</td><td>Output impedance</td></tr></table>	2
	(b)	(i)	– 12 [minus sign (1); 12 (1) – ignore any units given]	2
		(ii)	Feedback resistor to inverting input(1) non-inverting input to 0 V (1) input resistor between V_{IN} and inverting input. (1) ecf b(i)	3
	(c)	(iii)	Resistors in ratio 12:1 (1) e.c.f. and ≥ 1 kΩ (1) ecf b(ii)	2
			SR = $\frac{24}{5}$ = 4.8 (1) V μs^{-1}(1) unit mark Or 4 800 000 V s^{-1} award 2 marks	2
				[11]

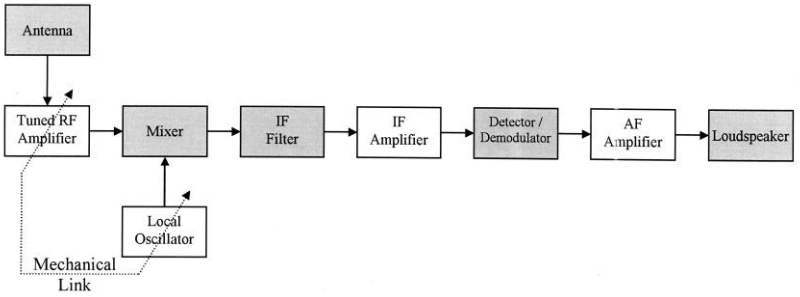
Question			Answers/Explanatory Notes	Marks Available
1.	*(a)*	(i)	15 kΩ (1)	2
		(ii)	45 kΩ (1) ecf from (i)	
	(b)	(i)	Voltage across resistors = 11.3 V (1) Voltage across 5.1 kΩ resistor = 6.4 V (1) V_{OUT} = 7.1 V (1)	3
		(ii)	12 V (1)	1
			Total question mark	**[6]**
2.	*(a)*	(i)	Debounces the signal from the switch	1
		(ii)	Astable [accept clock/pulse generator/relaxation oscillator]	1
	(b)		Switching thresholds at 2 s and 4 s (1) x 2 Inverted o/p + saturating at 0 V and 5 V (1) (-1) for any additional switching	3
			Total question mark	**[5]**
3.	*(a)*	(i)	V_{OC} = 12.75 V (1)	3
		(ii)	I_{SC} = 0.125 A (1)	
		(iii)	R_O = 102 Ω (1) ecf from (i) & (ii)	
	(b)	(i)	Equivalent cct with correct values from part (a) (1)	4
		(ii)	Voltage drop across 102 Ω resistor = 2.75 V (1) Current through 102 Ω resistor = 0.027 A (1) Minimum value of load resistance = 371 Ω (1)	
			Total question mark	**[7]**
4.	*(a)*	(i)	Graph 3 (1)	3
		(ii)	Graph 1 (1)	
		(iii)	Graph 4 (1)	
	(b)		Correct position and symbol for components (1) x 3	3
			Total question mark	**[6]**

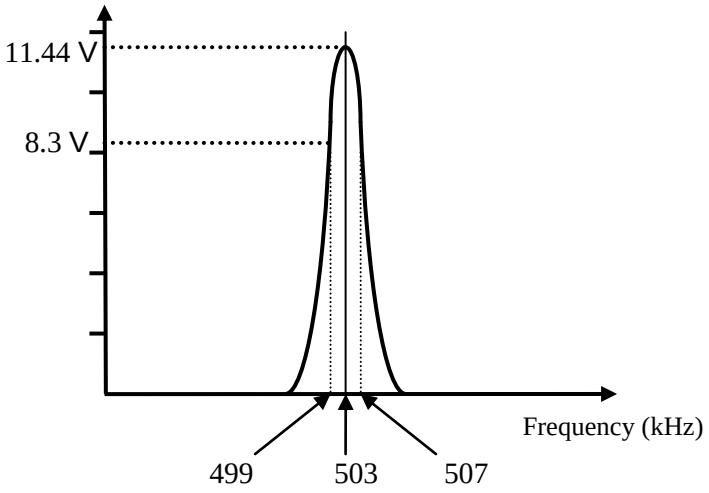
Question			Answers/Explanatory Notes	Marks Available
5.	*(a)*		LED off because logic level at o/p of second inverter = logic level at i/p of first inverter = 0	1
	(b)	(i)	9 V (1)	3
		(ii)	Substitution/multipliers (1) time taken = 10.4 s (1)	
		(iii)	LED comes on immediately (1) LED stays on for 10.4 s (1)	2
	(c)	(i)	7 V (1)	3
		(ii)	280 Ω (1) ecf from (i)	
		(iii)	300 Ω because 270 Ω would give a current of more than 25 mA (1)	
			Total question mark	**[9]**
6.	*(a)*		Substitution/multipliers (1) Mark = 46.2 ms (1) Space = 30.8 ms (1)	3
	(b)		Correct shape (1) Correct labels and M/S ratio (1)	2
	(c)		Period = 46.2 + 30.8 = 77 ms (1) ecf from (a) Frequency = $\frac{1}{77ms}$ = 13 Hz (1) [or substitution into frequency formula/multipliers (1), correct answer (1)]	2
			Total question mark	**[7]**
7.			Two resistors greater than 1 kΩ (1) Ratio resistors 1:2 e.g. 1 kΩ at top and 2 kΩ at bottom (1) Thermistor – correct symbol (1) Variable resistor (1) Motor connected between output and corresponding voltage rail to give correct switching action e.g. if thermistor is at the top of sensing sub system then the motor will be connected to 0 V rail and vice versa (1)	5
			Total question mark	**[5]**

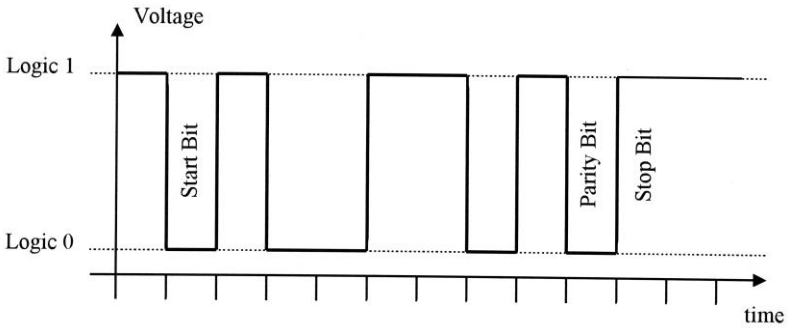
Question			Answers/Explanatory Notes	Marks Available
8.	*(a)*	(i)	Appropriate scales (1) Quality of curve (1) At least 7 accurate points (1)	3
		(ii)	V_{IN} = 1.75 V ecf from (i)	1
		(iii)	Voltage across base resistor 1.75 – 0.7 =1.05 V (1) $I_B = \frac{1.05}{1k\Omega}$ = 1.05 mA (1) ecf from previous step	2
	(b)		$I_c = \frac{6}{100}$ = 60 mA (1) $h_{FE} = \frac{60}{1.05}$ = 57 (1) ecf	2
			Total question mark	**[8]**
9.	*(a)*		12 – 4.7 = 7.3 V (1) $\frac{7.3}{25}$ = 0.292 A = 292 mA (1)	2
	(b)		7.3 x 0.292 (1) ecf from (a) = 2.132 W (1)	2
	(c)		292 – 7 =285 mA ecf from (a)	1
	(d)		Horizontal line at 4.7 V until I = 285 mA (1) Gradual downward slope thereafter (1)	2
			Total question mark	**[7]**
			TOTAL	**60**

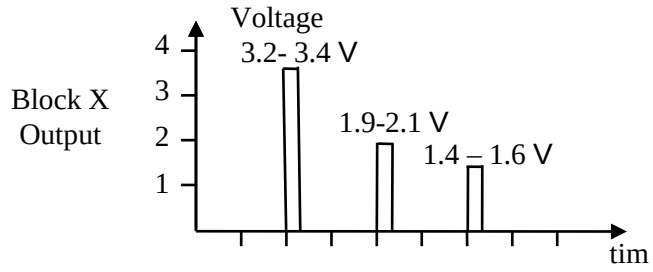
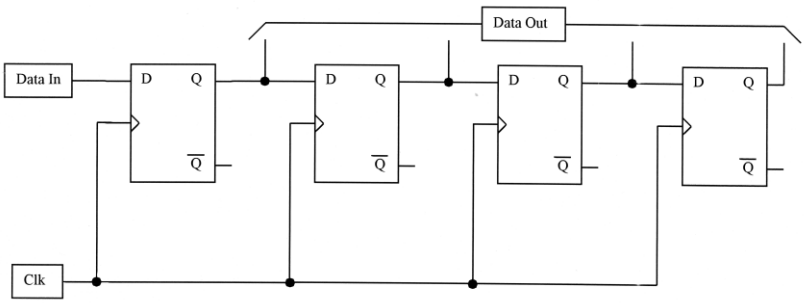
Question			Marking details	Marks Available
1	*(a)*		D	1
	(b)		E	1
	(c)		A	1
	(d)		B & C	1
				[4]
2	*(a)*		 Line spectrum (1) Correct carrier frequency (1) Correct side band frequencies (1)	3
	(b)	(i)	 Continuous Band spectrum	1
		(ii)	30 kHz	1
				[5]

Question			Marking details	Marks Available
3.	*(a)*		 Any reasonable frequency modulated signal (1) Accurate FM signal consistent with test signal (1)	2
	(b)	(i)	$\beta = \frac{\Delta f_c}{f_i}$ $\Delta f_c = \beta \times f_i$ $= 3 \times 15 \text{ kHz}$ $= 45 \text{ kHz}$	1
		(ii)	Bandwidth $= 2(1+\beta) f_i$ $= 2(1+3) \times 15 \text{ kHz}$ $= 120 \text{ kHz}$ *or* Bandwidth $= 2(\Delta f_c + f_i)$ $= 2(45 \text{ kHz} + 15 \text{ kHz})$ $= 120 \text{ kHz}$	1
				[4]
4.	*(a)*	(i)	$\frac{9 - V_{IN}}{57} = \frac{9-2}{47}$ $9 - V_{IN} = \frac{7 \times 57}{47}$ $9 - V_{IN} = 8.49$ $V_{IN} = 9 - 8.49 = 0.51 \text{V}$ correct formula / substitution (1) correct answer (1)	2
		(ii)	$\frac{-9 - V_{IN}}{57} = \frac{-9-2}{47}$ $-9 - V_{IN} = \frac{-11 \times 57}{47}$ $-9 - V_{IN} = -13.34$ $V_{IN} = -9 + 13.34 = 4.34 \text{V}$ correct formula / substitution (1) correct answer (1)	2
	(b)		Noise, Distortion or Attenuation.	1
				[5]

Question			Marking details	Marks Available
5.	*(a)*		 4 correct boxes - 3 marks 3 correct boxes - 2 marks 1 or 2 correct boxes - 1 mark	3
	(b)	(i)	$f_0 = \dfrac{1}{2\pi\sqrt{LC}}$ $= \dfrac{1}{2\pi\sqrt{0.05\times10^{-3}\times2\times10^{-9}}} = 503292 \text{ Hz} \cong 500 \text{ kHz}$ Multipliers (1) Answer (1)	2
		(ii)	$R_D = \dfrac{L}{r_L C}$ $R_D = \dfrac{0.05\times10^{-3}}{2.6\times2\times10^{-9}} = 9615.38\ \Omega \cong 9.6\ \text{k}\Omega$ correct substitution in correct formula (1) answer (1)	2
		(iii)	$V_{OUT} = \dfrac{12\times9615}{470+9615} = 11.44 \text{ V}$ Substitution in formula (1) Answer (1)	2
		(iv)	$Q = \dfrac{2\pi f_0 L}{r_L}$ $Q = \dfrac{2\pi\times506000\times0.05\times10^{-3}}{2.6} = 61.14 \cong 61$ Substitution in formula (1) Answer (1)	2

Question			Marking details	Marks Available
5.	*(b)*	(v)	$bandwidth = \frac{f_0}{Q} = \frac{506000}{61.14} = 8276 \text{ Hz} \cong 8.3 \text{ kHz}$ answer only	1
		(vi)	 • Shape • Peak output voltage 11.44 V • Use of bandwidth ~8.3 kHz at 0.707 V_{Pk} • Correct resonant frequency All 4 correct – 3 marks 2 or 3 correct – 2 marks 1 correct – 1 mark	3
				[**15**]

Question			Marking details	Marks Available
6.	*(a)*	(i)	The parity bit is a simple form of error checking. (Any reference to error correction = 0 marks)	1
		(ii)	Parity bit = 1	1
	(b)	(i)	 All 3 labels correct (1) 1 label correct (1)	2
		(ii)	Y	1
	(c)		The parity check still passes for this signal. The receiving equipment would not recognise that an error had occurred.	1
				[**6**]

Question			Marking details	Marks Available
7.	*(a)*		 All three levels correct – 2 marks Any one level correct – 1 mark	2
	(b)	(i)	The sampling frequency must be **twice / double** the **highest** frequency present in the input signal. [according to Nyquist sampling theorem]	1
		(ii)	The minimum frequency that can be used for Clock A is 36 kHz.	1
	(c)		Clock B must operate at a higher frequency than Clock A because the 16 bit output from the ADC must be output before the next sample is taken.	1
	(d)		$\text{resolution} = \frac{12}{2^{16}} = \frac{12}{65536} = 183.10\ \mu\text{V}$ correct use of 2^{16} (1) answer (1)	2
	(e)		 Common clock (1) Q - D x 3 (1) Data In marked (1) Data Out Marked (1)	4
				[11]

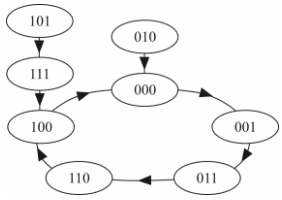
ET5

1. *(a)* Synchronous counters can count at high pulse frequency 1

(b) (i) Unused states - do not form part of the desired sequence (1) 2
Stuck states -prevent the system from ever reaching the desired sequence. (1)

(ii) On power up. 1

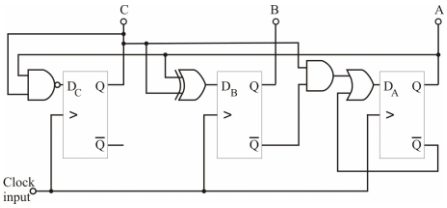
(c)



Main sequence (1) 2
Unused states connected correctly (1)

Total for Q1 **6**

2. *(a)*



One mark for each correct data input 3
One mark for using Q bar instead of NOT gates 1
One mark for correct clock inputs 1

(b)

Step	Current outputs			Next Outputs		
	C	B	A	D_C	D_B	D_A
0	0	0	0	1	0	1
1	1	0	1	0	0	1
2	0	0	1	1	1	0
3	1	1	0	1	1	1
4	1	1	1	0	0	0
5	0	1	0	1	0	1
6	0	1	1	1	1	0
7	1	0	0	1	1	1

All eight states correct, with correct subsequent state 4
Seven states correct, with correct subsequent state – 3 marks
Six states correct, with correct subsequent state – 2 marks
Five states correct, with correct subsequent state – 1 mark

Total for Q2 **9**

3. *(a)* Three least significant bits are inputs. The rest are outputs. 1

(b) The processor reads the contents of the interrupt vector address 1

(c) (i) These lines protect and recover the contents of the Working register when an interrupt occurs. 1

(ii) LEDs attached to bits 7, 6, 3 and 2 light (1) 3
for three seconds and then go out for three seconds. (1)
The processor checks to see if the reset switch has been closed. (1)

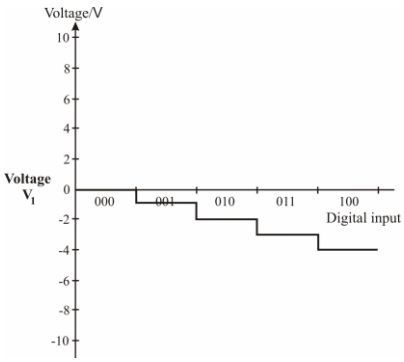
(iii) If so, it recovers the working register and goes back to the main program. (1) 2
Otherwise it goes back to the point labelled 'loop' and the sequence repeats.(1)

Total for Q3 **8**

4. *(a)* $V_1 = -1$ V 1

(b) $V_1 = -7$ V 1

(c)



Staircase waveform with equal height steps (1) 2
Step height equal to value given in *(a)*(1)

(d) Second amplifier is:

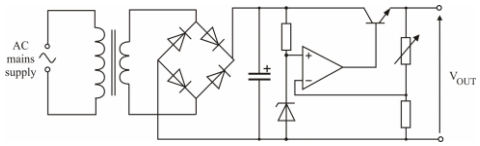
- Inverting – correct circuit diagram; (1) 2
- unity gain – correct resistor ratio and values > 1 kΩ. (1)

Total for Q4 **6**

5. *(a)* Power supply output voltage should remain constant (1) 3
Line regulation – when input voltage changes (1)
Load regulation – when output current changes, or equivalents (1)

(b) $V_{OUT} = 8.5$ V 1

(c)



V_Z to non-inverting input (1) 4
Voltage divider across output (1)
Centre of voltage divider to inverting input (1)
Output voltage variable (1)

Total for Q5 **8**

6. *(a)* Binary can produce false readings on transition from one segment to another 1

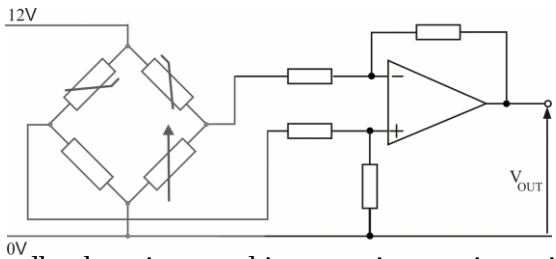
(b) $C = Z$ (1) 3
$B = Y \oplus Z$ (or $Y \cdot \overline{Z} + \overline{Y} \cdot Z$) (2)

Total for Q6 **4**

7. *(a)* $V_{OUT} = 0$ V 1

(b) Voltage at X = 7.0 V or voltage at Y = 7.5 V, or equivalent (1) 2
$V_{OUT} = 0.5$ V (1)

(c)



Feedback resistor and input resistor to inverting input (1) 2
Resistor from non-inverting input to 0 V and input resistor (1)

(d) Feedback resistor = 40 × input resistor (1) 3
All resistors > 1 kΩ (1)
Identical resistors in inverting input and non-inverting input connections (1)

Total for Q7 **8**

8. *(a)* (i) X = diac 1

(ii) Improve rise time for the gate signal, or equivalent 1

(b) (i) Y = Thyristor 1

(ii) Between P and Q: thyristor is switched on, or equivalent (1) 2
Elsewhere: thyristor is switched off, or equivalent (1)

(iii) Z = capacitor 1

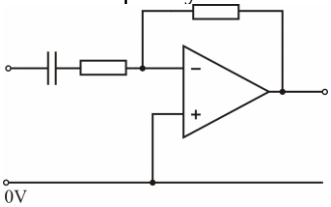
(iv) Mention of phase lag, or equivalent (1) 2
Charge/discharge of capacitor slowed by effect of series resistor, or equivalent (1)

Total for Q8 **8**

9. *(a)* (i) Bass cut filter 1

(ii) Break frequency = 90 Hz 1

(iii)



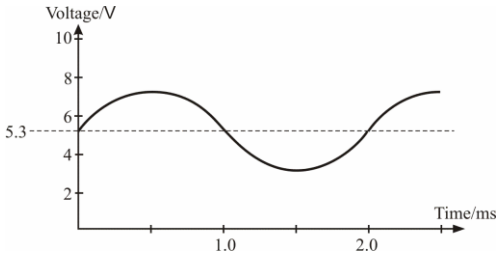
Resistor and capacitor in series (1) 3
RC network in input circuit (1)
Remainder of circuit correct (1)

(iv) Voltage gain greater than 1 (1) 2

(b) Break frequency = 970 Hz (1)

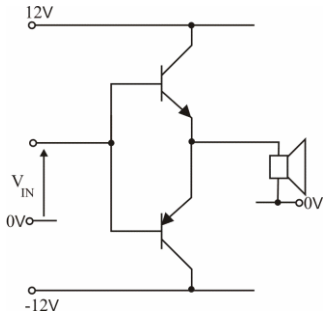
Total for Q9 **7**

10. *(a)*



Sitting on 5.3 V (1) 2
Amplitude = 2 V (1)

(b)



Common base connection to V_{IN}
Common emitter connection to speaker
Collectors to power rails
Correct symbols
All four elements correct 3
Any three elements correct - 2 marks only
Any two elements correct - 1 mark only

(c) Advantage such as lower quiescent power dissipation 1

Total for Q10 **6**

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