Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS

ET1

A.M. TUESDAY, 15 May 2012

1¼ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**6**	
2.	**5**	
3.	**6**	
4.	**10**	
5.	**6**	
6.	**5**	
7.	**3**	
8.	**8**	
9.	**11**	
Total	**60**	

1141
010001

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Boolean identities

$$A+\overline{A}.B = A+B$$

$$A.B + A = A.(B+1) = A$$

Operational amplifier

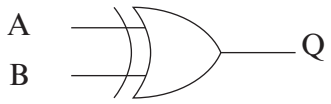
$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1+\frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Answer **all** *questions.*

1. *(a)* (i) Complete the truth table for the two-input EXOR gate shown below.



B	A	Q
0	0	
0	1	
1	0	
1	1	

[1]

(ii) Write down the Boolean expression for the output Q.

Q = ... [1]

(b) Here is the truth table for a **different** two-input logic gate.

B	A	Q
0	0	1
0	1	1
1	0	1
1	1	0

Identify the logic gate.

Logic gate = ... [1]

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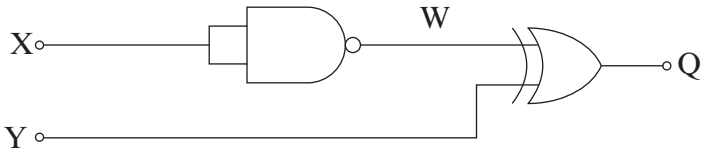
(c) (i) Complete the truth table for this circuit.



X	Y	W	Q
0	0		
1	0		
0	1		
1	1		

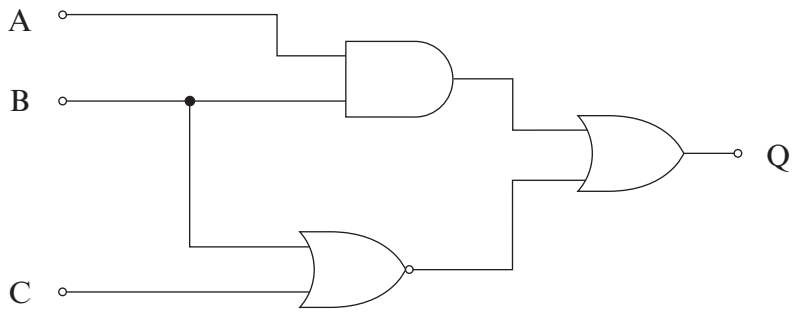
[2]

(ii) What single logic gate will produce the same output as Q?

.....

[1]

2. The diagram shows a logic system.



(a) In the space below, draw the same logic system, but with the logic gates replaced by their NAND equivalents. [3]

(b) Draw a line through all redundant gates. [2]

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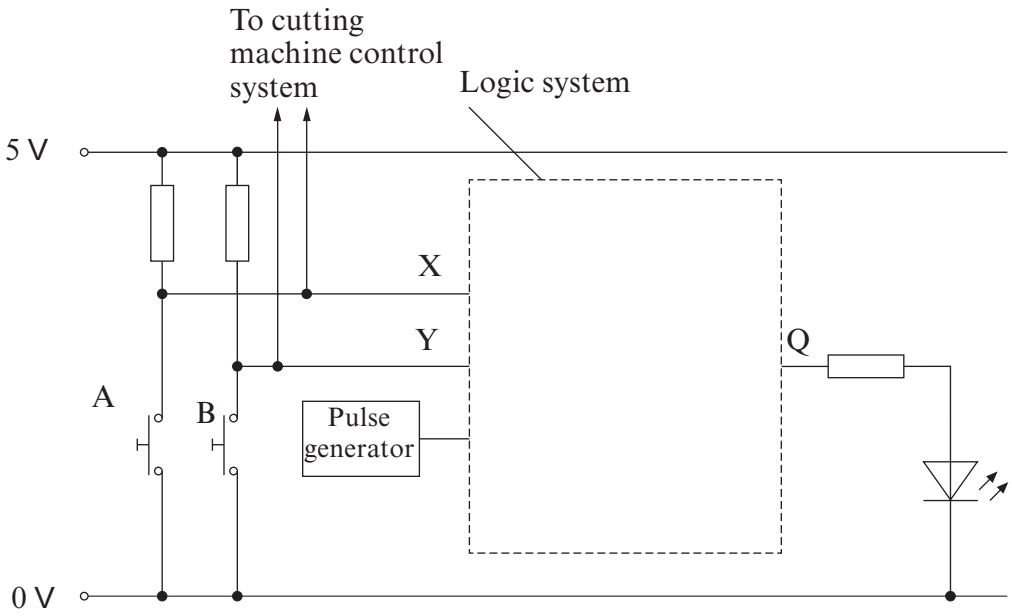
3. The diagram shows a warning system for a cutting machine.

- The operator closes switch A to operate the machine.
- The machine will not start until a safety shield has automatically closed switch B.
- The LED flashes when both switches are closed to warn that the machine is in use.



(a) Why are resistors needed with the switches?

.....

.....

[1]

(b) What is the logic level at point Y when switch B is open?

Logic level at Y = ... [1]

(c) What logic level at output Q causes the LED to light?

Logic level at Q = ... [1]

(d) Design a logic system, to make the LED flash only when both switches are closed. Draw your design in the dotted box in the diagram. [3]

Examiner only

4. *(a)* Simplify the following expressions.

(i) $\overline{A} + 0 =$ ..... [1]

(ii) $B.(\overline{A} + \overline{B}) =$ ..... [2]

(b) In designing a logic system, a student has produced the Karnaugh map shown below.

DC \ BA	00	01	11	10
00	1	0	1	1
01	1	0	0	0
11	0	0	0	0
10	1	0	1	1

Give the simplest Boolean expression for the output Q of this logic system.
Show on the map the groups that you created.

Q = ... [4]

(c) Apply DeMorgan's theorem to the following expression **and** simplify it.

$$Q = \overline{B.A.B}$$

.....

.....

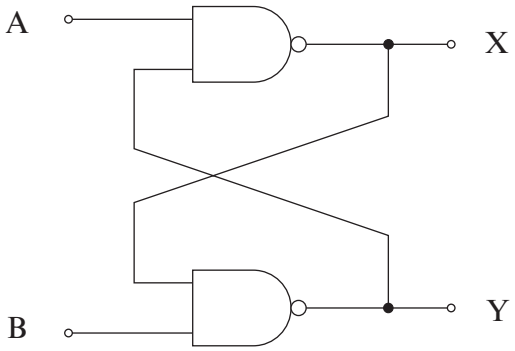
.....

.....

.....

..... [3]

5. *(a)* The following circuit shows a NAND gate bistable.



Complete the truth table to show the sequence of outputs at X and Y, for the given sequence of inputs A and B. [3]

A	B	X	Y
1	1	0	1
0	1		
1	1		
1	0		
1	1		
0	0		

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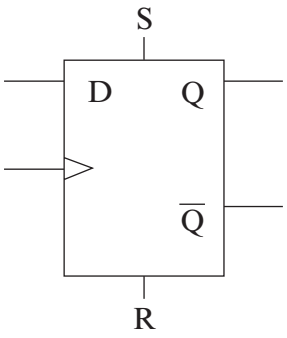
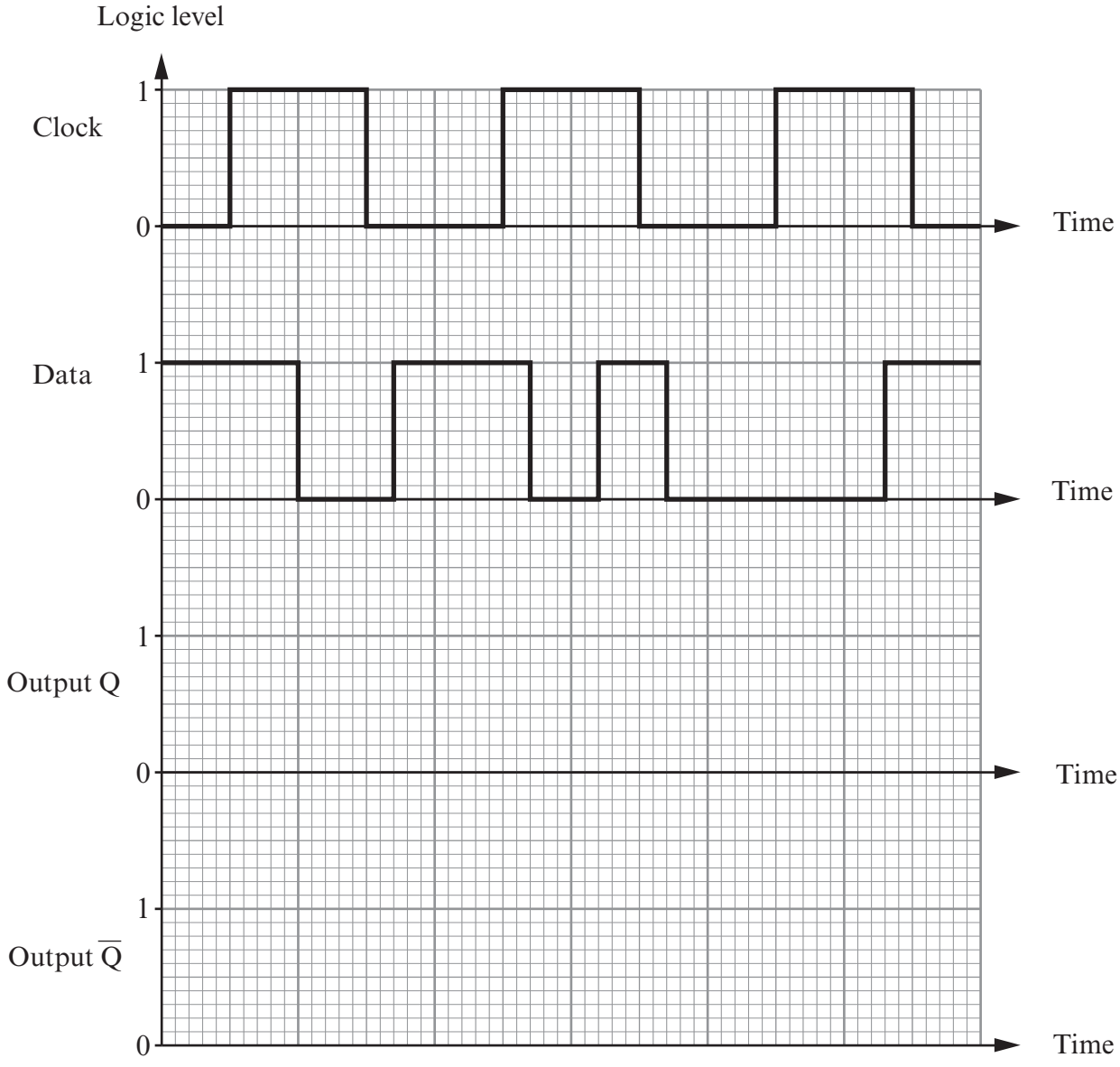
(b) The D-type flip-flop in the diagram is rising-edge triggered.



The signals applied to the clock and data inputs are shown below.
Complete the timing diagram for the Q and $\overline{Q}$ outputs.



[3]

Turn over.

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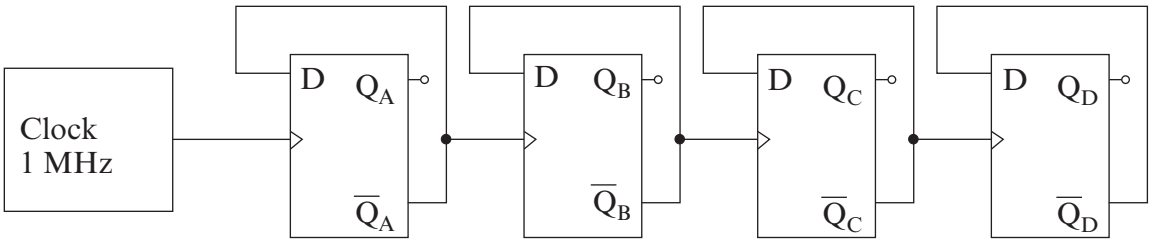
6. The clock in the following diagram produces a square wave output of frequency 1 MHz. This is fed into the series of 4 D-type flip-flops shown here. The D-type flip-flops are rising-edge triggered.



(a) What is the frequency at the output Q_A?

.....

[1]

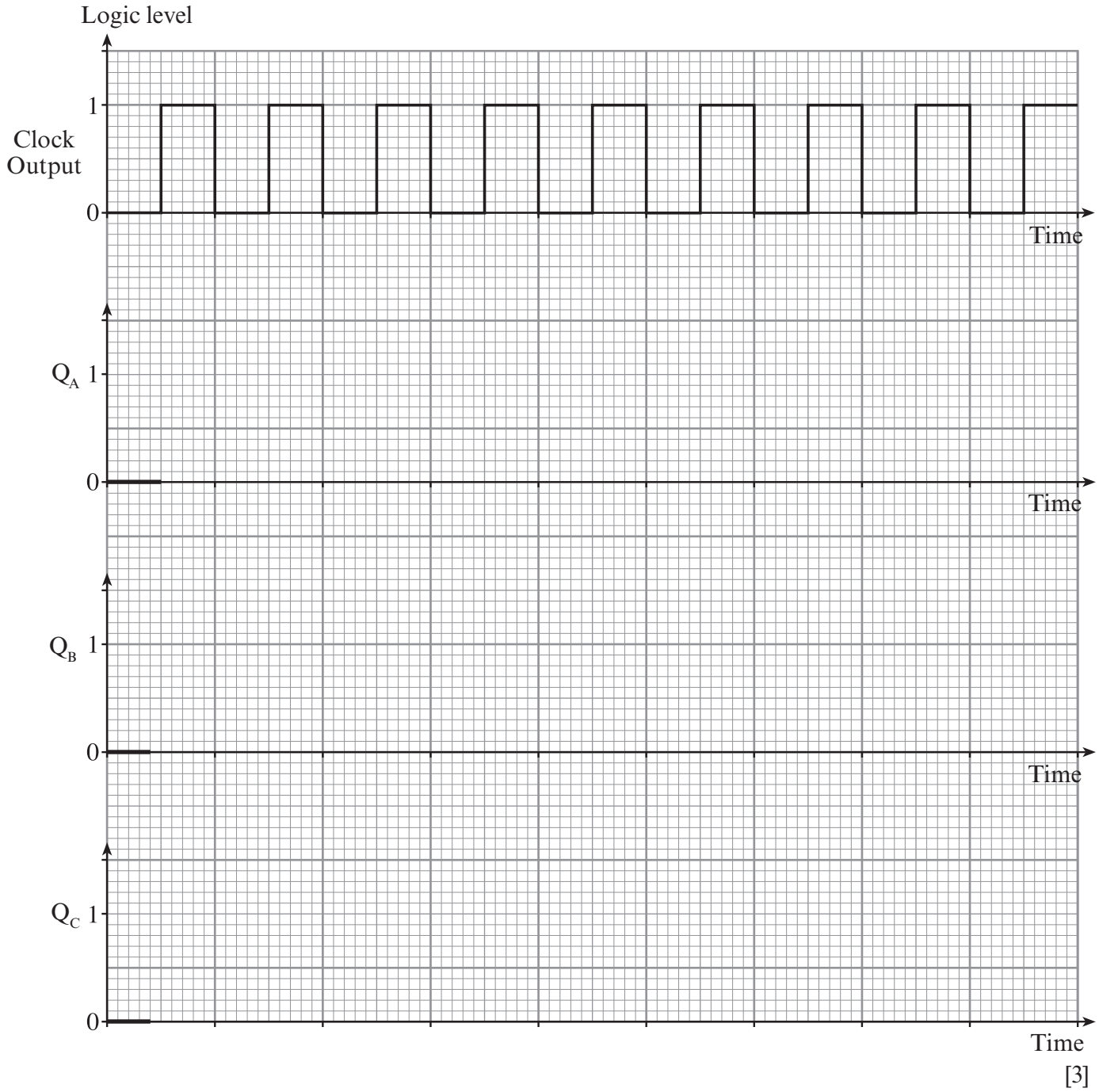
(b) Which output will produce a frequency of 125 kHz?

.....

[1]

Examiner only

(c) The timing diagram below shows the output from the clock.
Complete the diagram to show the signal at outputs Q_A, Q_B and Q_C.



[3]

Examiner only

7. A D-type flip-flop contains a transition gate made of NAND gates.

(a) In the space below draw a transition gate using 2-input NAND gates.

[2]

(b) What function does the transition gate perform within the D-type flip-flop?

.....

.....

.....

[1]

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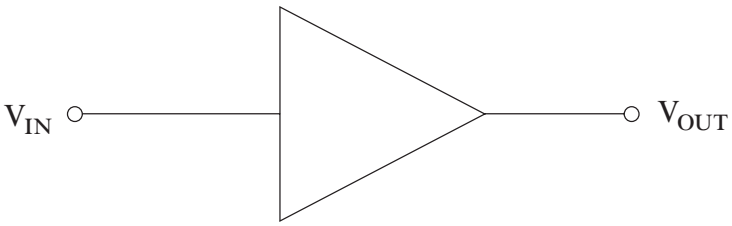
8. A student investigates the frequency response of a voltage amplifier based on an op-amp.



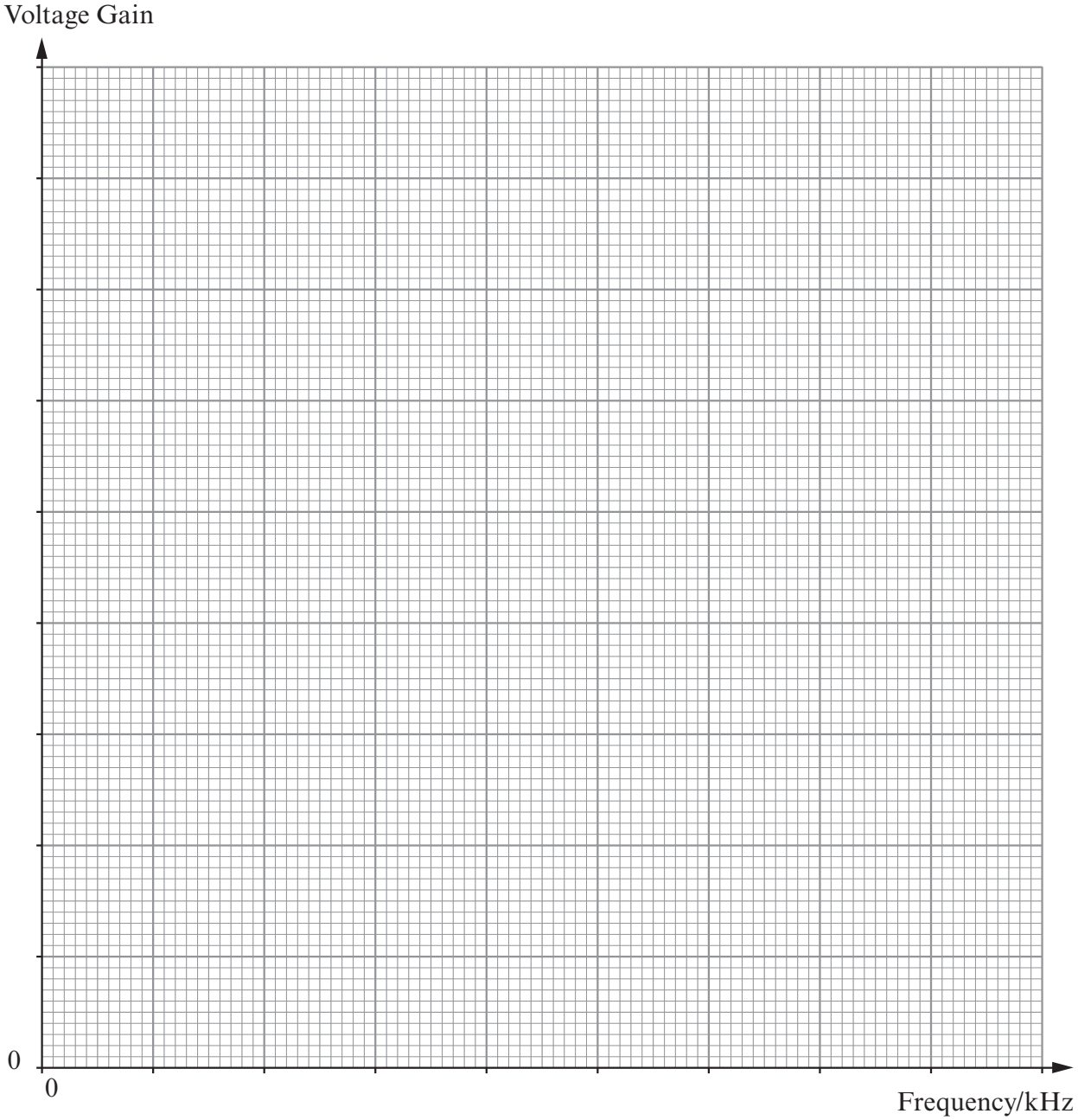
The following results were collected:

Frequency/kHz	V_{IN}/V	V_{OUT}/V	Voltage gain
5	0.5	15.0	
10	0.5	15.0	
15	0.5	15.0	
20	0.5	14.1	
25	0.5	12.5	
30	0.5	10.0	
35	0.5	7.2	
40	0.5	4.4	

(a) Complete the voltage gain column of the table. [1]

Examiner only

(b) Use the results to plot a graph of voltage gain against frequency. [3]



(c) Use the graph to estimate the bandwidth.
Show **on the graph** how you obtained your answer.

Bandwidth = ... [2]

(d) Determine the gain-bandwidth product of the voltage amplifier.

.....

.....

..... [2]

Turn over.

Examiner only

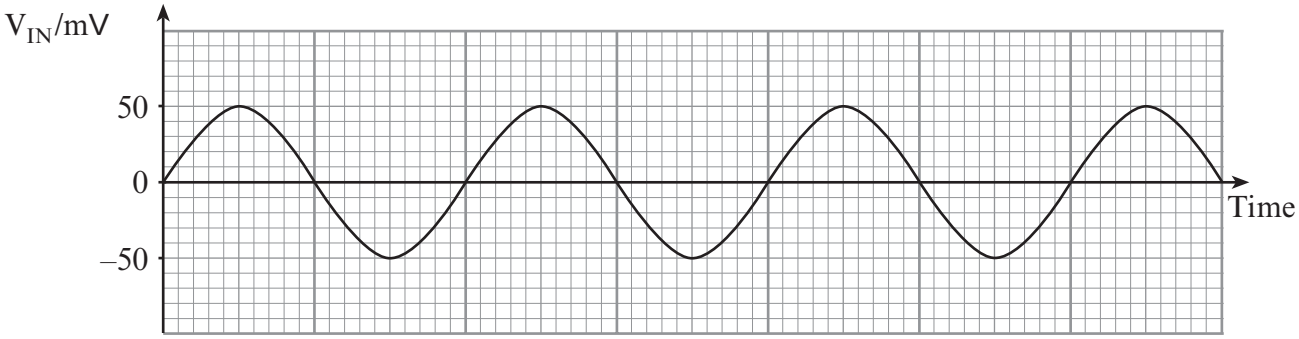
9. *(a)* Some op-amp parameters have a very high value and some a very low value.

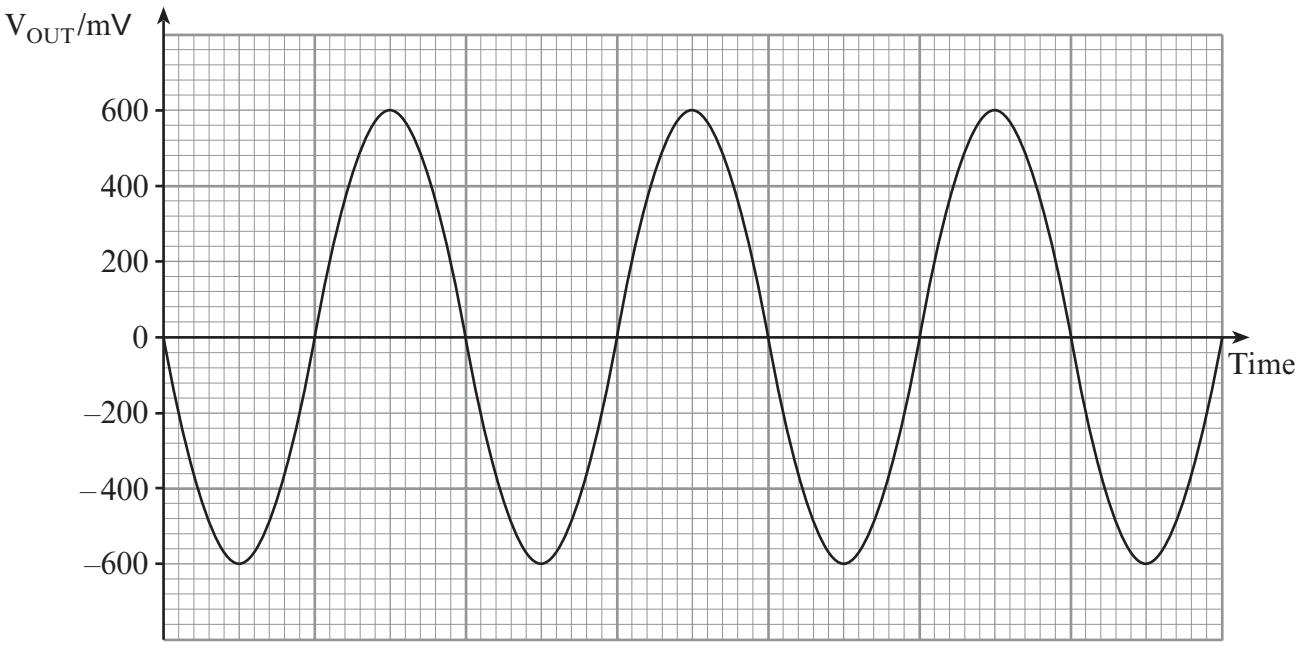
Place **each** of the following parameters in the correct column of the table. [2]

Input impedance Output impedance Slew rate Open loop gain

High value	Low value

(b) An op-amp voltage amplifier has the following input and output signals.





(i) What is the voltage gain of the amplifier? [2]

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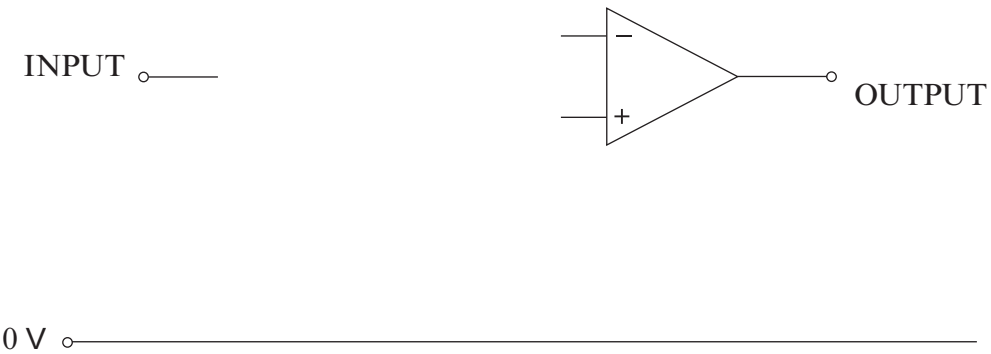
(ii) Draw the circuit diagram for the amplifier to give this voltage gain.



[3]

(iii) Calculate suitable resistor values to give the voltage gain in *(b)*(i) and write these on the diagram.

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[2]

(c) In response to a large step input, the output of the op-amp changes from –12 V to +12 V in a time of 5.0 μs. Calculate the slew rate, giving the appropriate unit.

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.....

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[2]

THERE ARE NO MORE QUESTIONS IN THE EXAMINATION.