Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

ELECTRONICS
ET1

P.M. TUESDAY, 10 January 2012

1¼ hours

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**9**	
2.	**8**	
3.	**4**	
4.	**6**	
5.	**6**	
6.	**7**	
7.	**8**	
8.	**12**	
Total	**60**	

1141
010001

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES IN ET1

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities

$$A + \overline{A}.B = A + B$$

$$A.B + A = A.(B+1) = A$$

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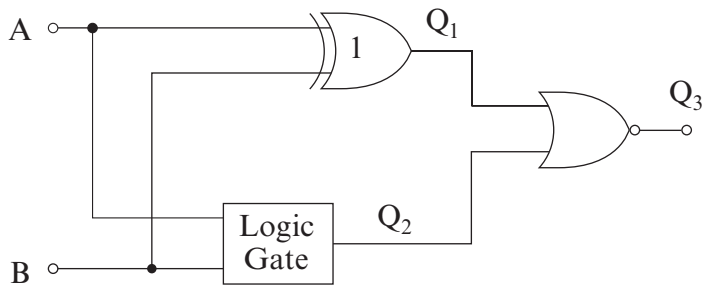
Examiner only

1. The following diagram shows a logic system.



(a) Identify Gate 1 ..... [1]

(b) The partially completed truth table for the logic system is shown below.

INPUTS		OUTPUTS		
B	**A**	**Q_1**	**Q_2**	**Q_3**
0	**0**		**1**	
0	**1**		**1**	
1	**0**		**1**	
1	**1**		**0**	

(i) Identify the logic gate that gives output Q_2.

Gate ..... [1]

(ii) Complete the truth table for the outputs Q_1 and Q_3. [2]

(c) Give the Boolean expression for **each** of the outputs Q_1, Q_2 and Q_3 in terms of A and B.

Q_1 = ...

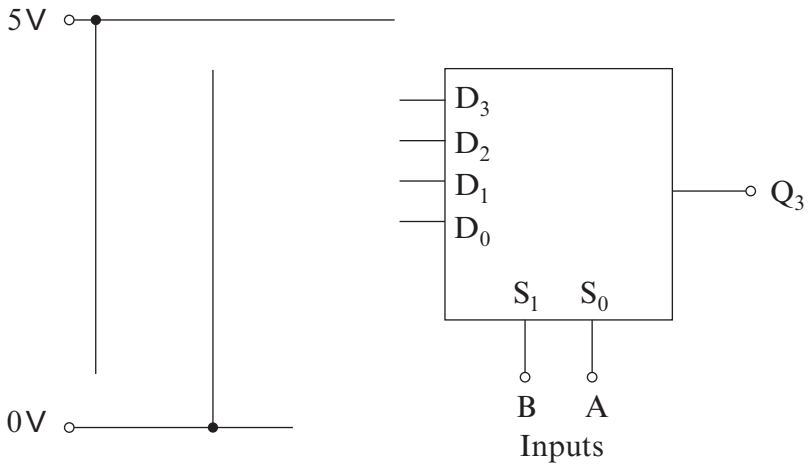
Q_2 = ...

Q_3 = ... [3]

(d) Name the single gate that would produce the same output as Q_3.

..... [1]

(e) Show on the following diagram how the same output Q_3 could be generated using a multiplexer.



[1]

Examiner only

2. A logic system gives the following truth table.

C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(a) (i) Use the table to write down the unsimplified Boolean expression for Q in terms of C, B and A.

Q = ... [2]

(ii) Fully simplify the expression using a Karnaugh map and/or the rules of Boolean algebra.

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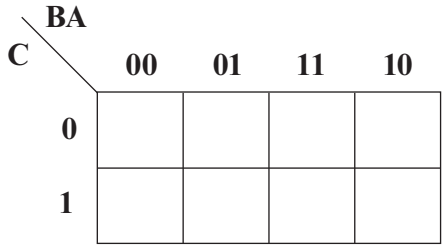
.....



[3]

(b) Apply DeMorgan's theorem to the following expression **and** simplify the result.

$$Q = \overline{\overline{(\overline{A}+B)}.A.\overline{B}}$$

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.....

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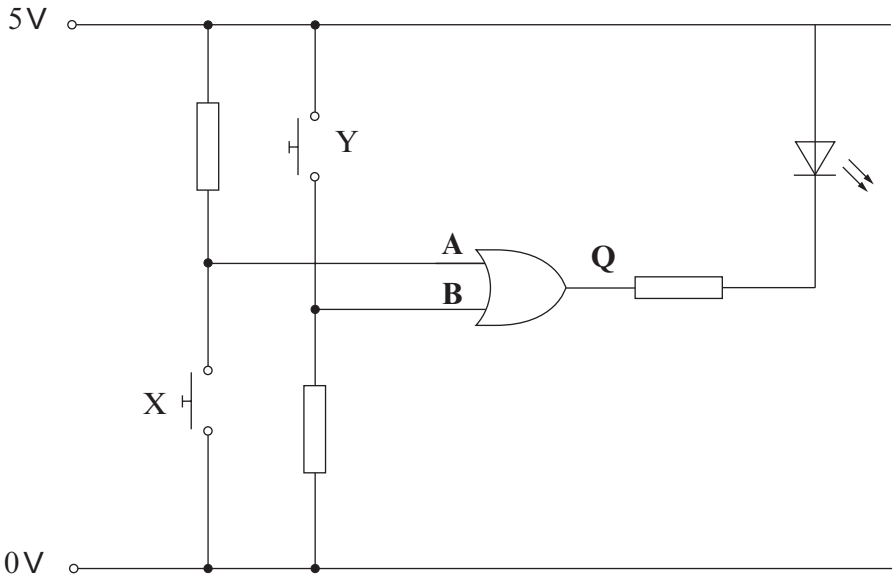
[3]

3. A warning system has two switches, X and Y, which are used as sensors.



The table below shows the four possible settings of switches X and Y.
Complete the table by adding:

- the correct logic level for points **A**, **B** and **Q**.
- the word **'OFF'** or **'ON'** to indicate the state of the LED in **each** case.

Switch X	Switch Y	Input A	Input B	Output Q	State of LED
Open	Open				
Open	Closed				
Closed	Open				
Closed	Closed				

[4]

4. The truth table for a logic gate is given below.

B	A	Q
0	0	1
0	1	0
1	0	0
1	1	1

(a) Using only AND, OR and NOT gates, draw a diagram of a logic system that will produce this truth table.

[1]

(b) Redraw your system in part *(a)* using only NAND gates.

[3]

(c) Draw a line through all redundant gates. [2]

Examiner only

5. *(a)* (i) Convert the decimal number 53 to

BCD .....

Binary ..... [2]

(ii) Give **one** advantage of coding information using BCD rather than Binary.

.....

[1]

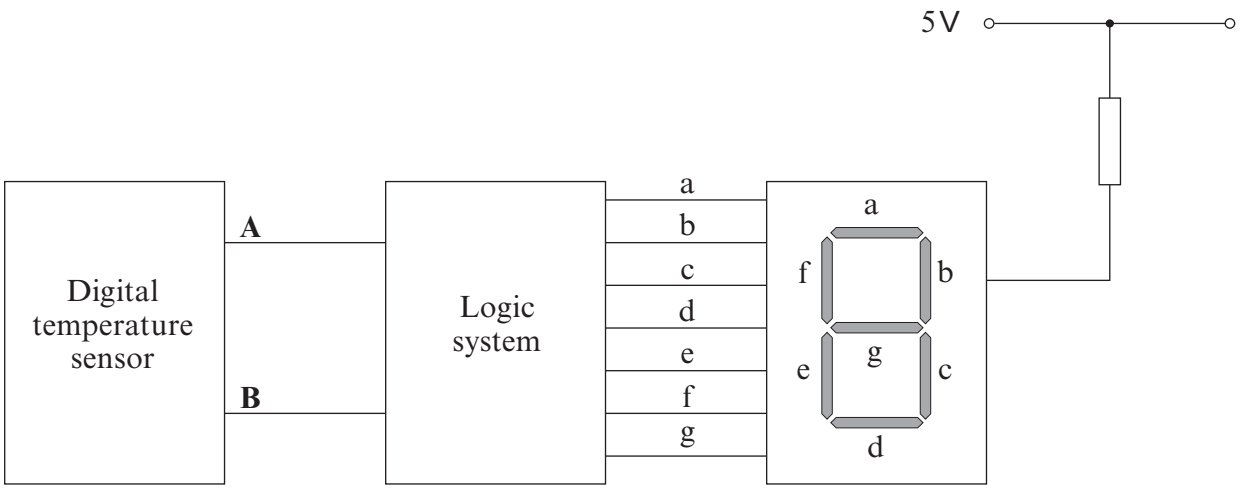
(b) A car engine is fitted with a temperature sensor that produces a 2-bit output. The sensor is connected through a logic system to a **common-anode** 7-segment display.

If it is too hot the display shows the letter 

If the temperature is satisfactory it displays the letter 

If it is too cold the display shows the letter 

A block diagram for the system is shown below.



The sensor produces the digital signals shown in the table.

Temperature	A	B
too hot	0	0
satisfactory	0	1
	1	0
too cold	1	1

(i) Complete the following table to show the seven signals, **a** to **g**, needed to light each display. **Logic 0 from the logic system will light each segment**. [2]

Display	A B	a	b	c	d	e	f	g
	0 0							
	0 1							
	1 0							
	1 1							

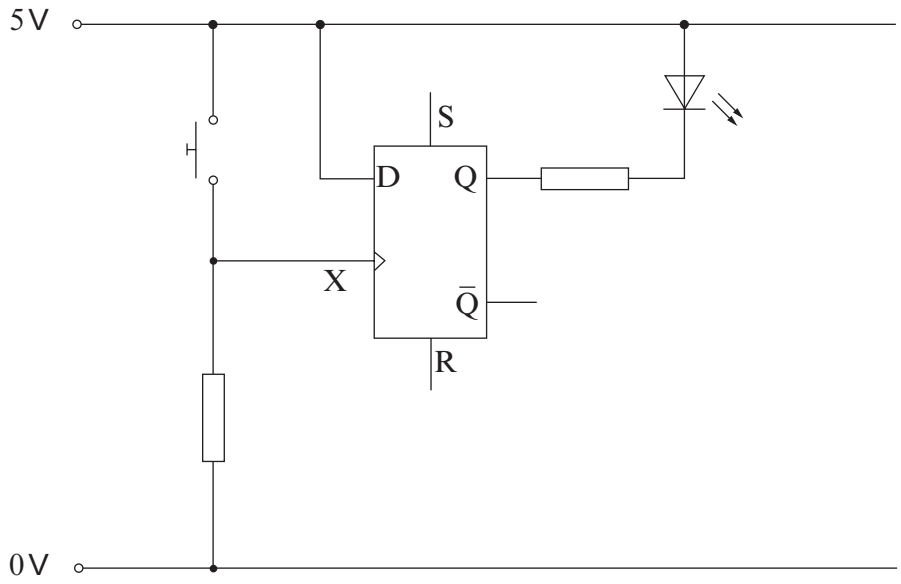
(ii) What single logic gate in the logic system would generate the required signal for segment d?

.....

[1]

Examiner only

6. The diagram shows a circuit containing a *rising-edge-triggered* D-type flip-flop.



(a) (i) The reset is *active high*. What does this mean?

.....

.....

[1]

(ii) Add the necessary components to the diagram such that the D-type can be **reset** with the momentary press of a switch. [2]

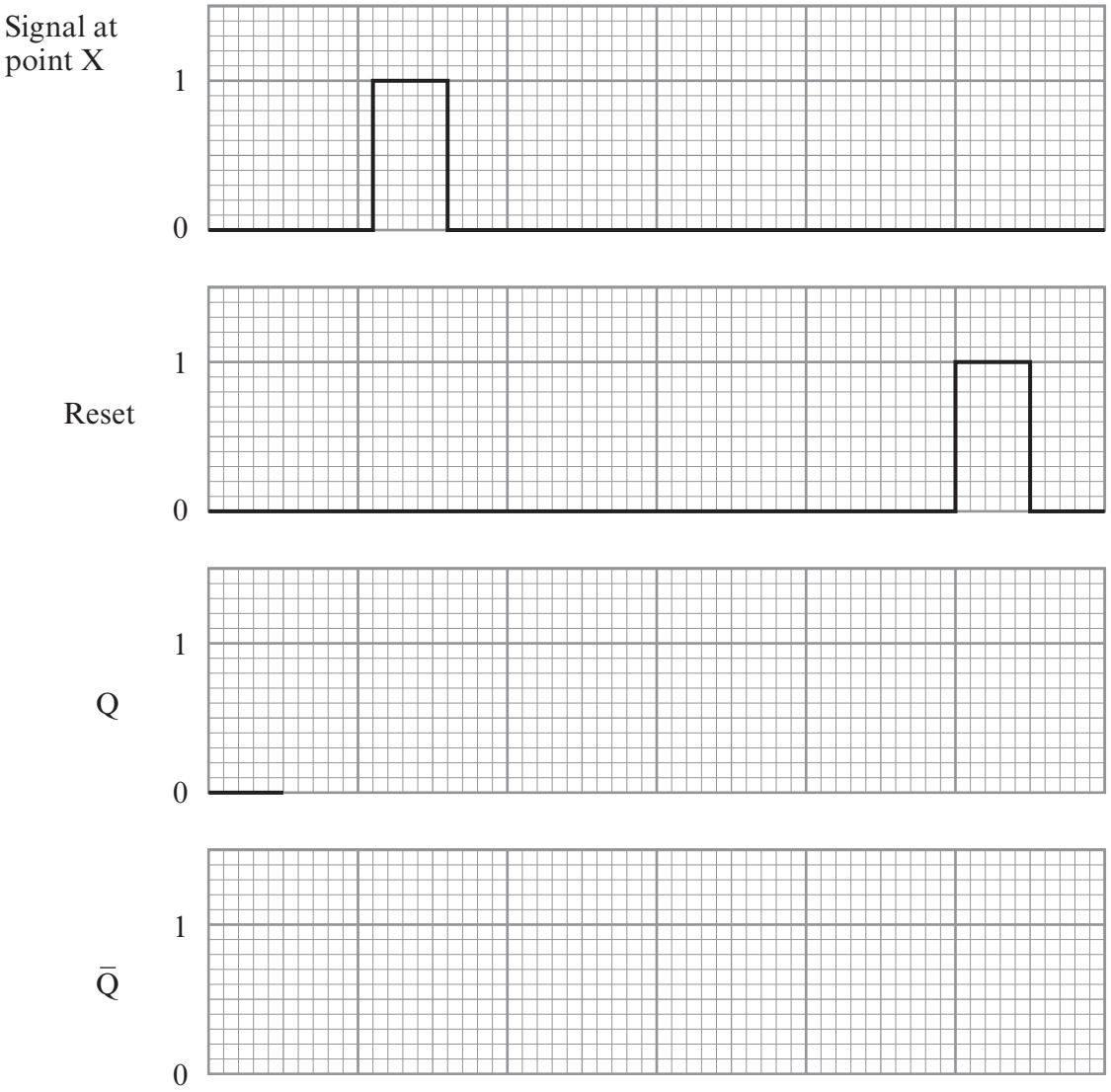
(b) Complete the following sentence.

When the D-type is reset, the output Q will be at logic ..... and the LED will be ..... .

[1]

Examiner only

(c) The *rising-edge-triggered* D-type is initially reset. The signals shown in the timing diagrams below are applied to the D-type. Complete the timing diagram for the outputs Q and $\overline{Q}$.



[3]

Turn over.

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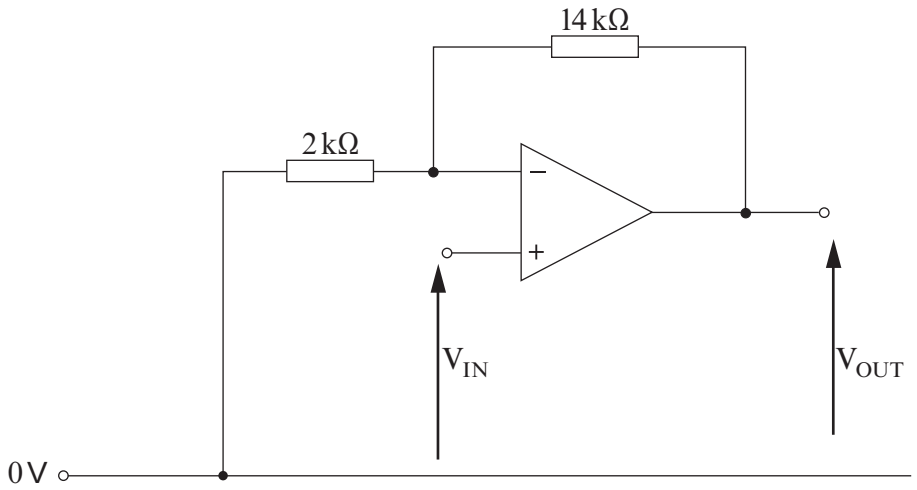
7. The following diagram shows an op-amp set up as a voltage amplifier. The op-amp is powered from a ± 15 V supply. It saturates at ± 14 V.



(a) (i) Calculate the voltage gain of the amplifier.

.....

.....

[1]

(ii) Determine the input voltage at which the amplifier just saturates.

.....

.....

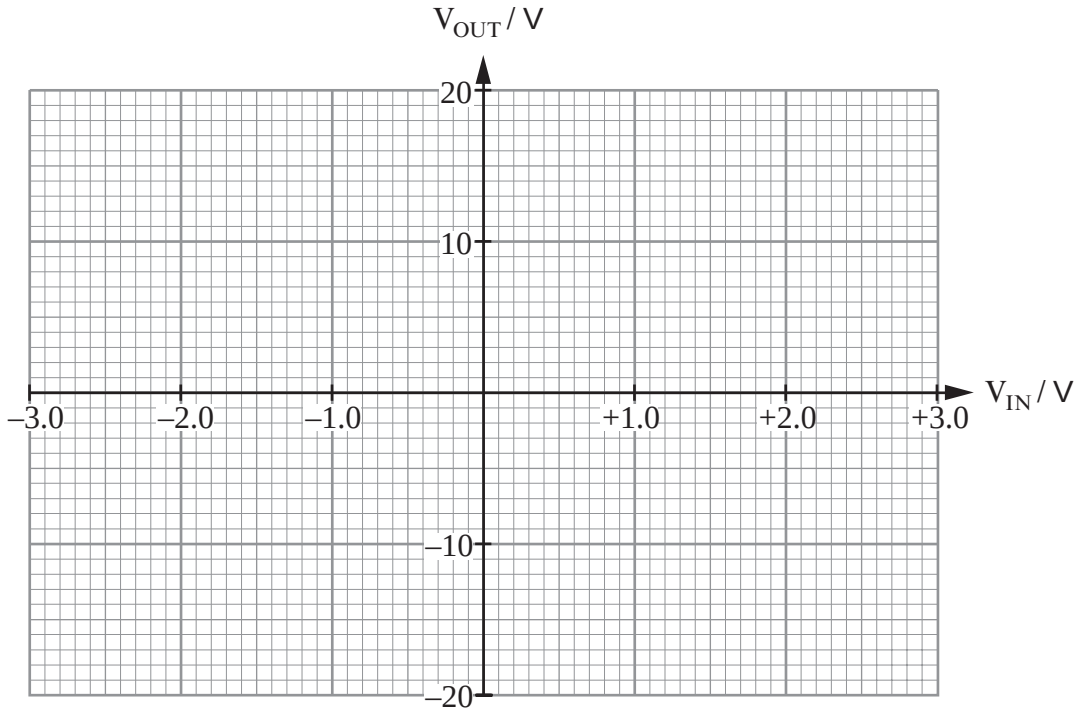
[1]

(b) A student varies the input voltage V_{IN} from – 3.0 V to + 3.0 V.

V_{IN} / V	V_{OUT} / V
–3.0	
–2.0	
–1.0	
1.0	
2.0	
3.0	

(i) Use the information in part *(a)* to complete the V_{OUT} column of the table. [2]

(ii) Draw the graph of V_{OUT} against V_{IN}.



[3]

(c) The student replaces the 2 kΩ resistor with a 3 kΩ resistor. What effect will this have on the input voltage needed to saturate the amplifier?

.....

.....

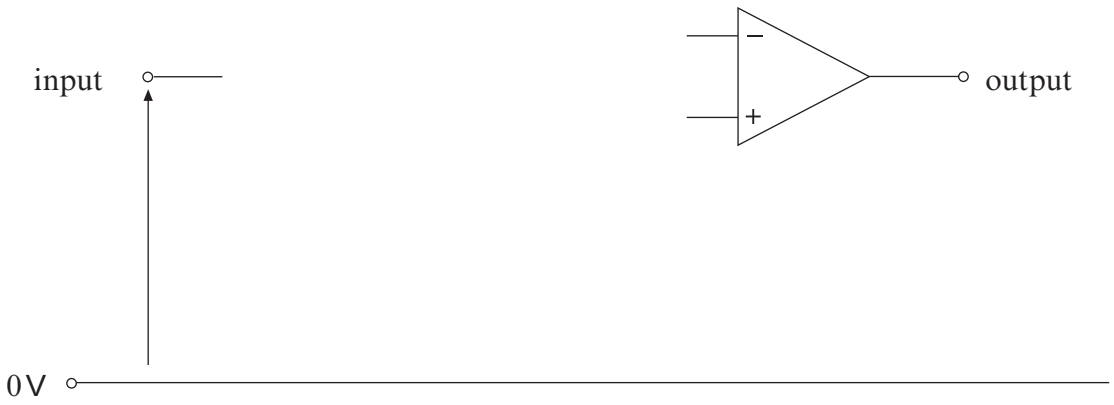
[1]

Examiner only

8. An extract from the data sheet for an op-amp is given below. The op-amp is powered by a ± 15 V supply.

Parameter	Value
Open-loop gain	3.0×10^5
Input Impedance	$2.0 \times 10^{12}\ \Omega$
Saturation voltage	± 14.0 V
Slew Rate	$5.6\ \text{V}\ \mu\text{s}^{-1}$
Gain-bandwidth product	3 MHz

(a) (i) Draw the circuit diagram for an inverting amplifier based on this op-amp.



[3]

(ii) Select suitable resistors to give a gain of –12.

R_F .....

R_{IN} .....

[2]

Examiner only

(b) A test signal V_{IN} is applied to the input.

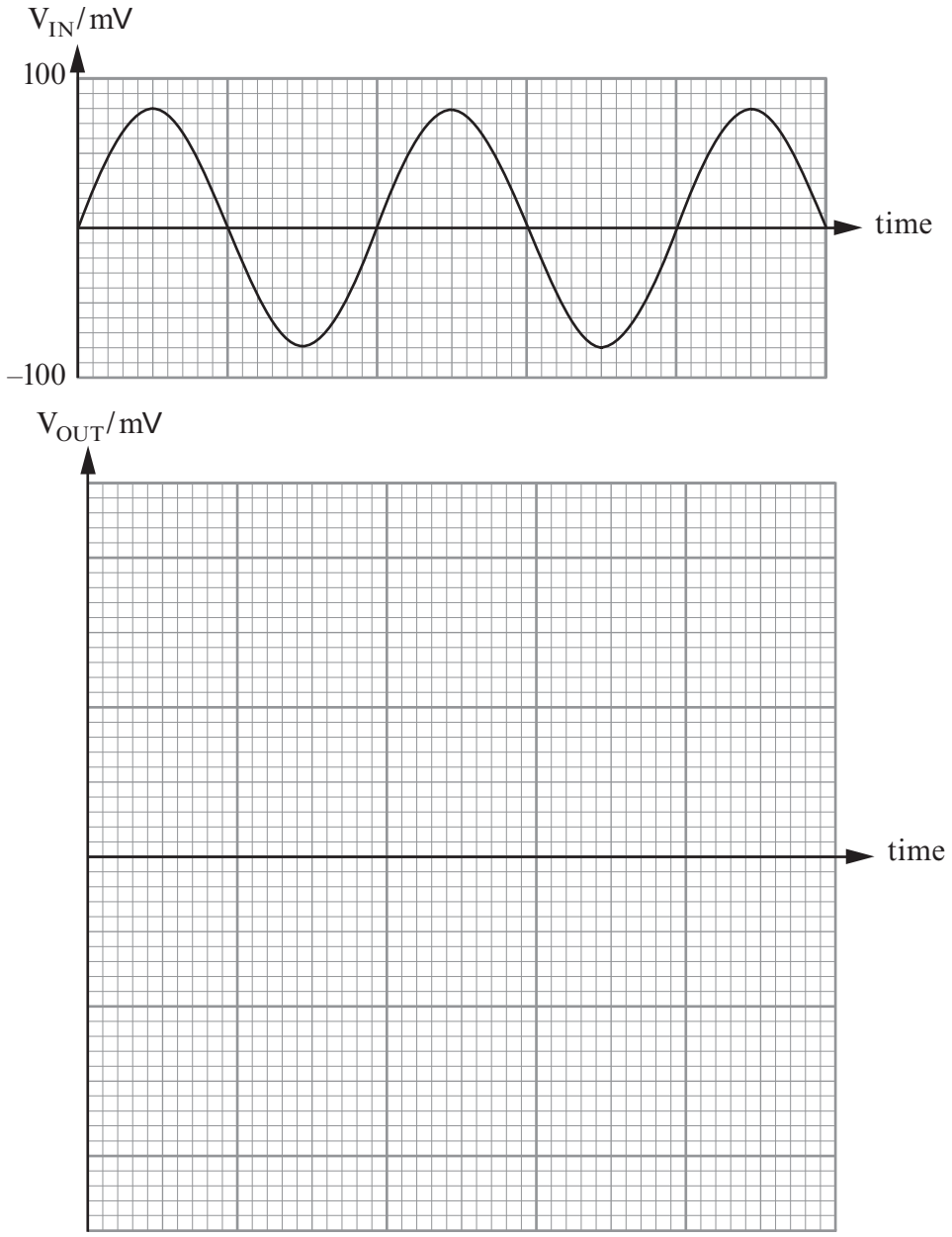
(i) Use the information on the graph below to calculate the amplitude of the output voltage.

.....

.....

[1]

(ii) Complete the graph to show the output voltage V_{OUT}. Label any significant voltages.



[2]

(c) What is the bandwidth of this amplifier?

.....

.....

[1]

THIS QUESTION CONTINUES OVER THE PAGE.

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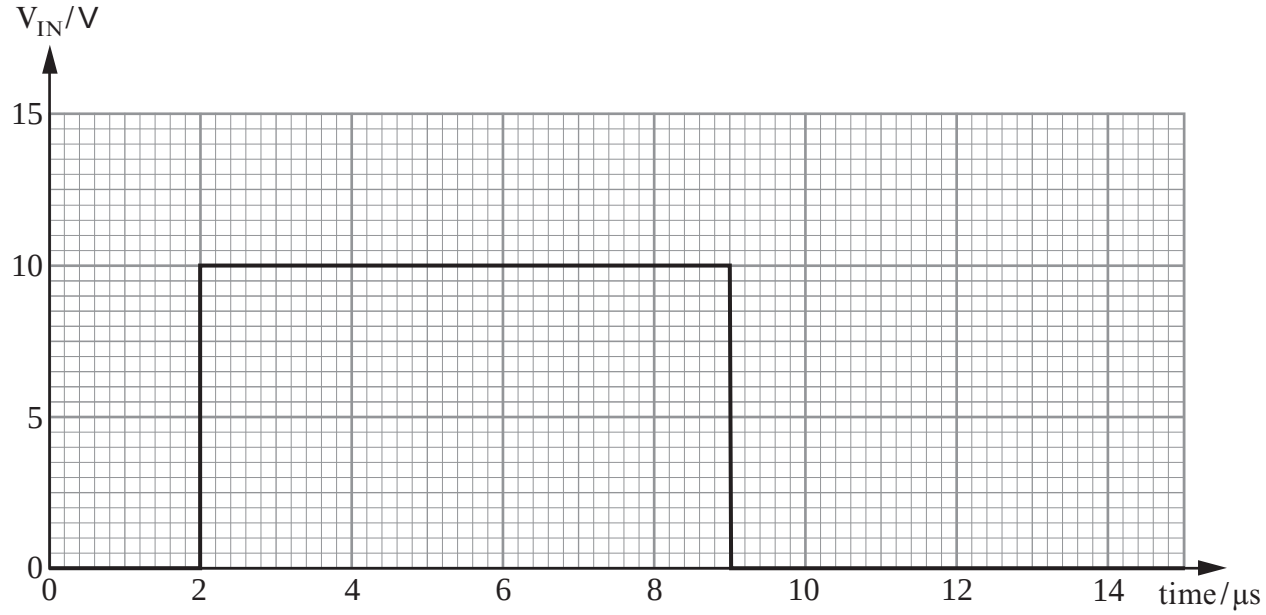
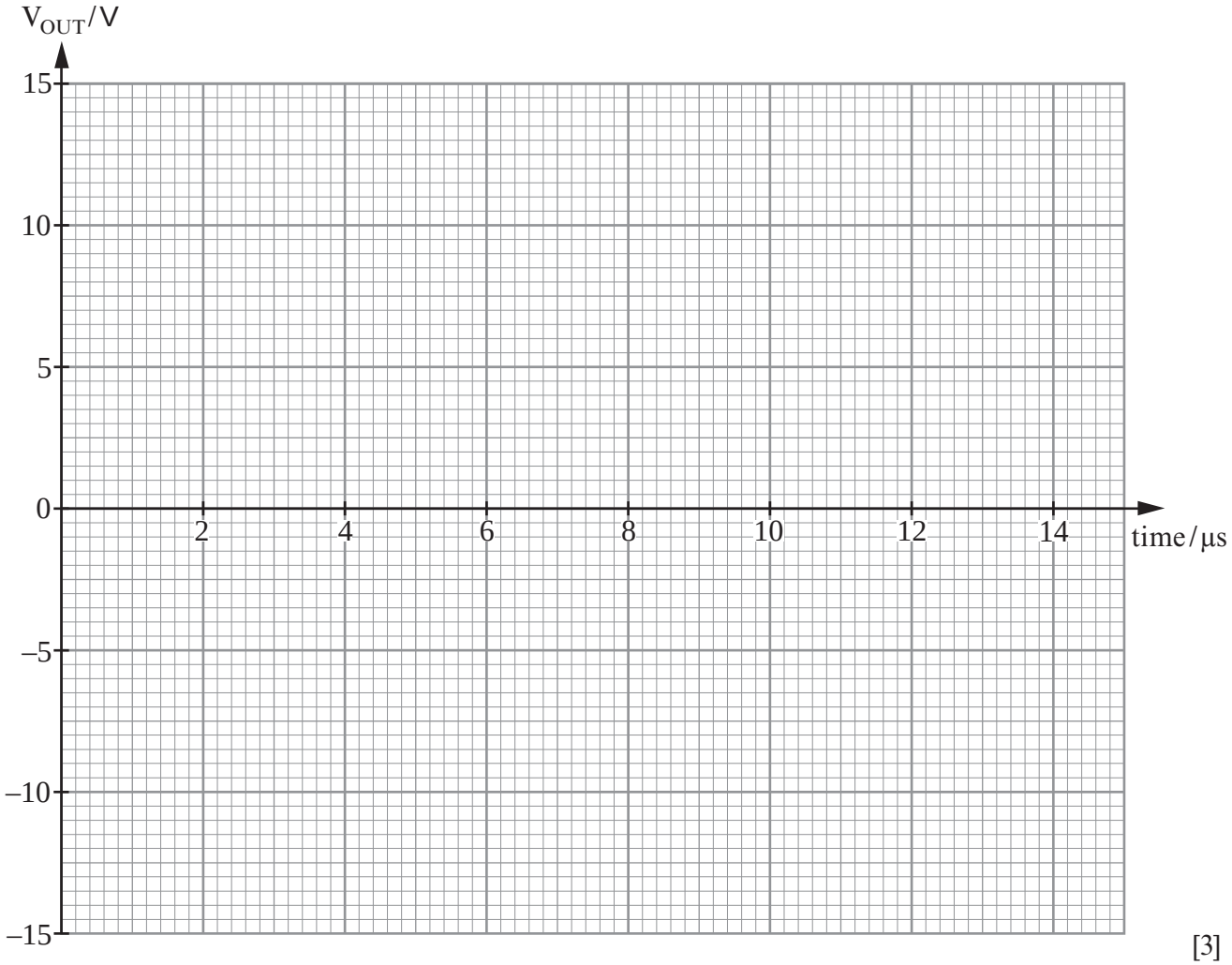
(d) The following signal is applied to the input to illustrate the effect of slew-rate on the output of the voltage amplifier.
Draw the output voltage on the axes below.
V_{OUT} is initially at 0 V.





[3]

THERE ARE NO MORE QUESTIONS IN THE EXAMINATION.