| Candidate Name | Centre Number | Candidate Number |
|---|---|---|
| | | 2 |

WJEC CBAC

# GCE AS/A level

381/01

# ELECTRONICS

## ET1

A.M. FRIDAY, 16 May 2008

1½ hours

**ADDITIONAL MATERIALS**

In addition to this examination paper, you will need a calculator.

**INSTRUCTIONS TO CANDIDATES**

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

**INFORMATION FOR CANDIDATES**

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

| For Examiner's use only. | |
|---|---|
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | |
| Total | |

## INFORMATION FOR THE USE OF CANDIDATES

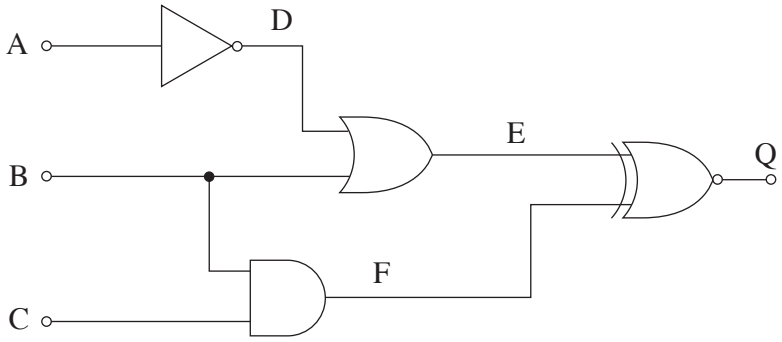
**Preferred Values for resistors**

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

| | | |
|---|---|---|
| **RC networks** | $V_C = V_O\,(1 - e^{-t/RC})$ | for a charging capacitor |
| | $V_C = V_O\,e^{-t/RC}$ | for a discharging capacitor |
| | $t = -RC\ 1n\left(1 - \frac{V_C}{V_O}\right)$ | for a charging capacitor |
| | $t = -RC\ 1n\left(\frac{V_C}{V_O}\right)$ | for a discharging capacitor |
| **Alternating Voltages** | $V_O = V_{rms}\sqrt{2}$ | |
| **Silicon Diode** | $V_F \approx 0{\cdot}7\,V$ | |
| **Bipolar Transistor** | $h_{FE} = \frac{I_C}{I_B}$ | Current gain |
| | $V_{BE} \approx 0{\cdot}7\,V$ | in the on state |
| **MOSFETs** | $I_D = g_M V_{GS}$ | |
| **Operational amplifier** | $G = -\frac{R_F}{R_{IN}}$ | Inverting amplifier |
| | $G = 1 + \frac{R_F}{R_1}$ | Non-inverting amplifier |
| | $V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$ | Summing amplifier |
| | $\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$ | Slew rate |
| **555 Monostable** | $T = 1{\cdot}1\ RC$ | |
| **555 Astable** | $t_H = 0{\cdot}7\,(R_A + R_B)C$ | |
| | $t_L = 0{\cdot}7\,R_B C$ | |
| | $f = \frac{1 \cdot 44}{(R_A + 2R_B)C}$ | |
| **Schmitt Astable** | $f \approx \frac{1}{RC}$ | |

**1.** A system of logic gates is shown below.




*(a)* Give the Boolean expressions for the outputs D, E and F of the gates in the logic system **in terms of A, B and C**. [2]

D = .....

E = .....

F = .....

*(b)* Complete the truth table for the system.

| C | B | A | D | E | F | Q |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | |
| 0 | 0 | 1 | | | | |
| 0 | 1 | 0 | | | | |
| 0 | 1 | 1 | | | | |
| 1 | 0 | 0 | | | | |
| 1 | 0 | 1 | | | | |
| 1 | 1 | 0 | | | | |
| 1 | 1 | 1 | | | | |

[4]

Examiner only

**2.** The output Q of an electronic warning system in a car sounds an alarm if either the driver's door is opened or the ignition key is removed whilst the headlights are on.

- A microswitch, C, on the driver's door outputs a logic 1 if the door is opened.
- A sensor, B, outputs a logic 0 when the ignition key is removed.
- The headlight switch, A, outputs a logic 1 when switched on.

*(a)* Complete the truth table for the logic system.

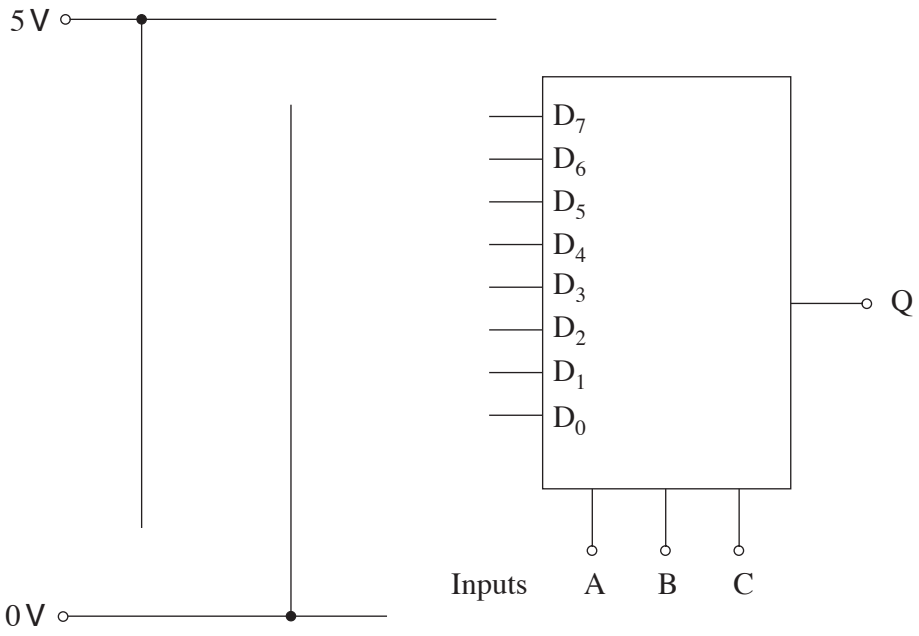
| Door switch C | Key sensor B | Headlight switch A | Q |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

[2]

*(b)* Write down the Boolean expression for Q in terms of C, B and A.
*There is no need to simplify it.*

Q = ..... [2]

*(c)* Show on the following diagram how the same output as Q can be generated using an 8 to 1 multiplexer.

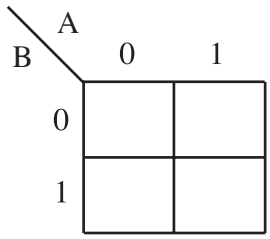



[2]

**3.** *(a)* Simplify the following expressions.

(i) $A + 1 =$ .....

(ii) $A.\overline{B} + B =$ .....




[3]

*(b)* Either using a Karnaugh map or the rules of Boolean algebra simplify the following expression as much as possible.

$$Q = C.B.\overline{A} + \overline{D}.\overline{C}.B.A + D.B.A + C.\overline{B}.\overline{A} + D.\overline{C}.B.\overline{A}$$

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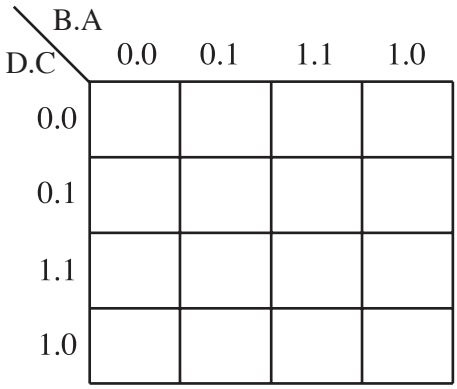


[5]

*(c)* Apply DeMorgan's theorem to the following expression **and** simplify the result.

$$Q = \overline{(\overline{A} + \overline{B}).(\overline{A}.B)}$$

.....

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.....

.....

.....

[3]

Examiner only

**4.** All logic gates have a propagation delay.

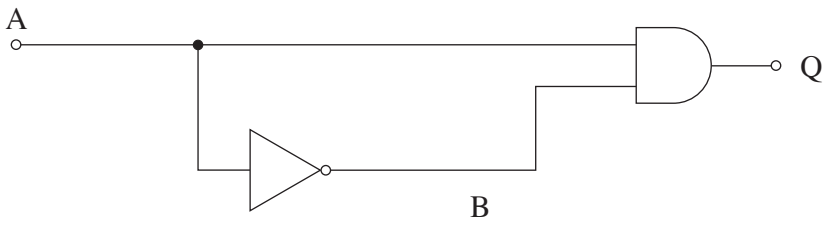
*(a)* Explain what is meant by a *propagation delay*.

.....

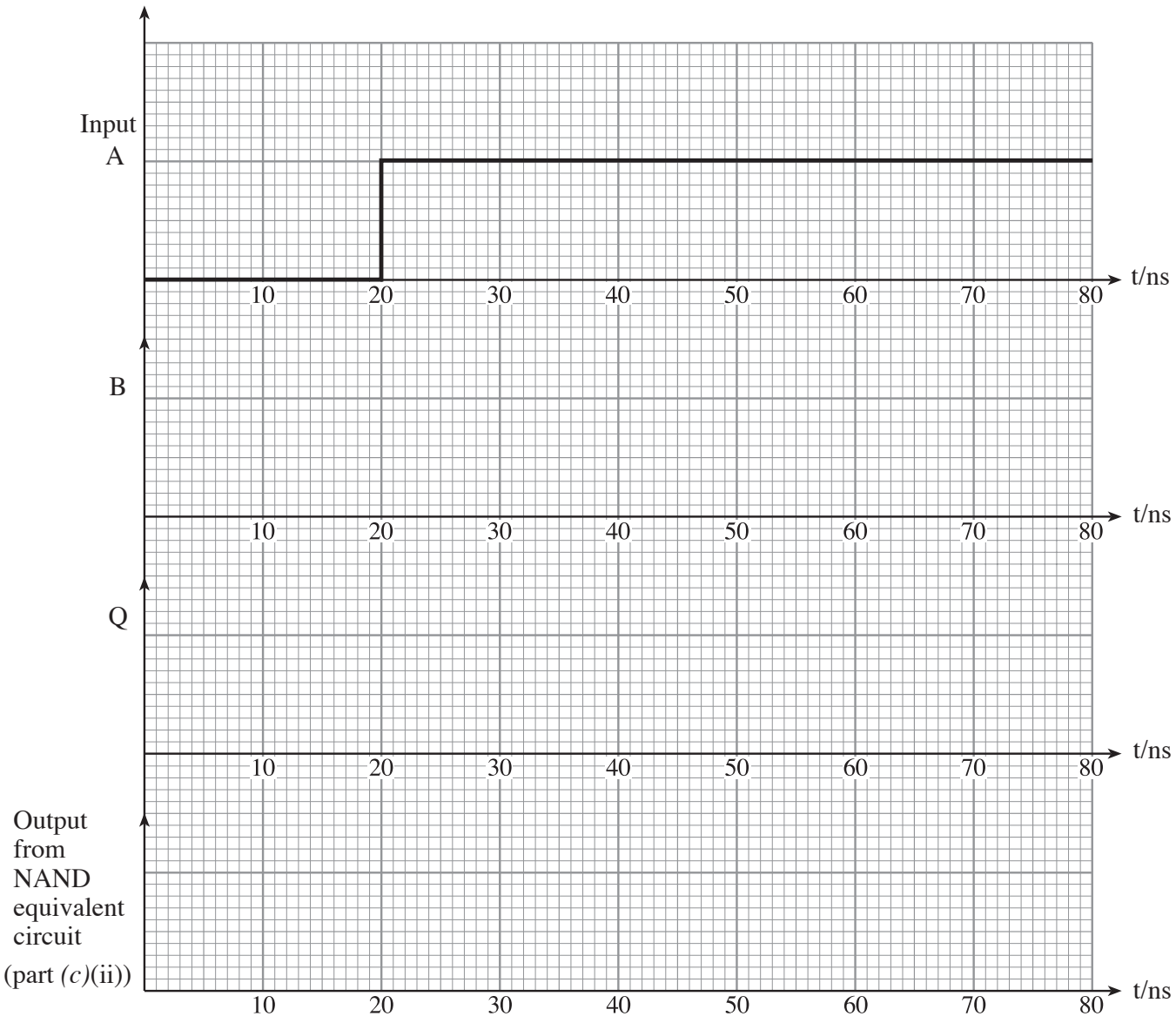
.....

[1]

*(b)* A simple transition gate makes use of this propagation delay.
For each logic gate the propagation delay is 10 ns.




An input signal, shown on the timing diagram below, is applied to input A.
Show on the diagram how the logic levels at B and Q change over the course of 80 ns.



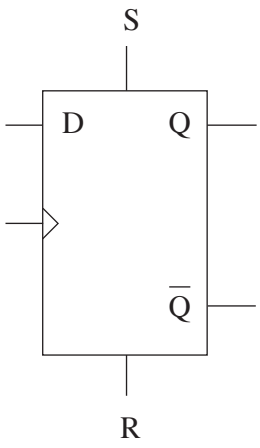

[4]

*(c)* (i) Redraw the transition gate replacing each gate with its NAND-gate equivalent.

[1]

(ii) Draw the output signal from the NAND equivalent circuit on the timing diagram. [2]

**5.** A D-type flip flop is shown below.




The RESET is *active high*.

*(a)* What is the effect of taking input R to logic 1?

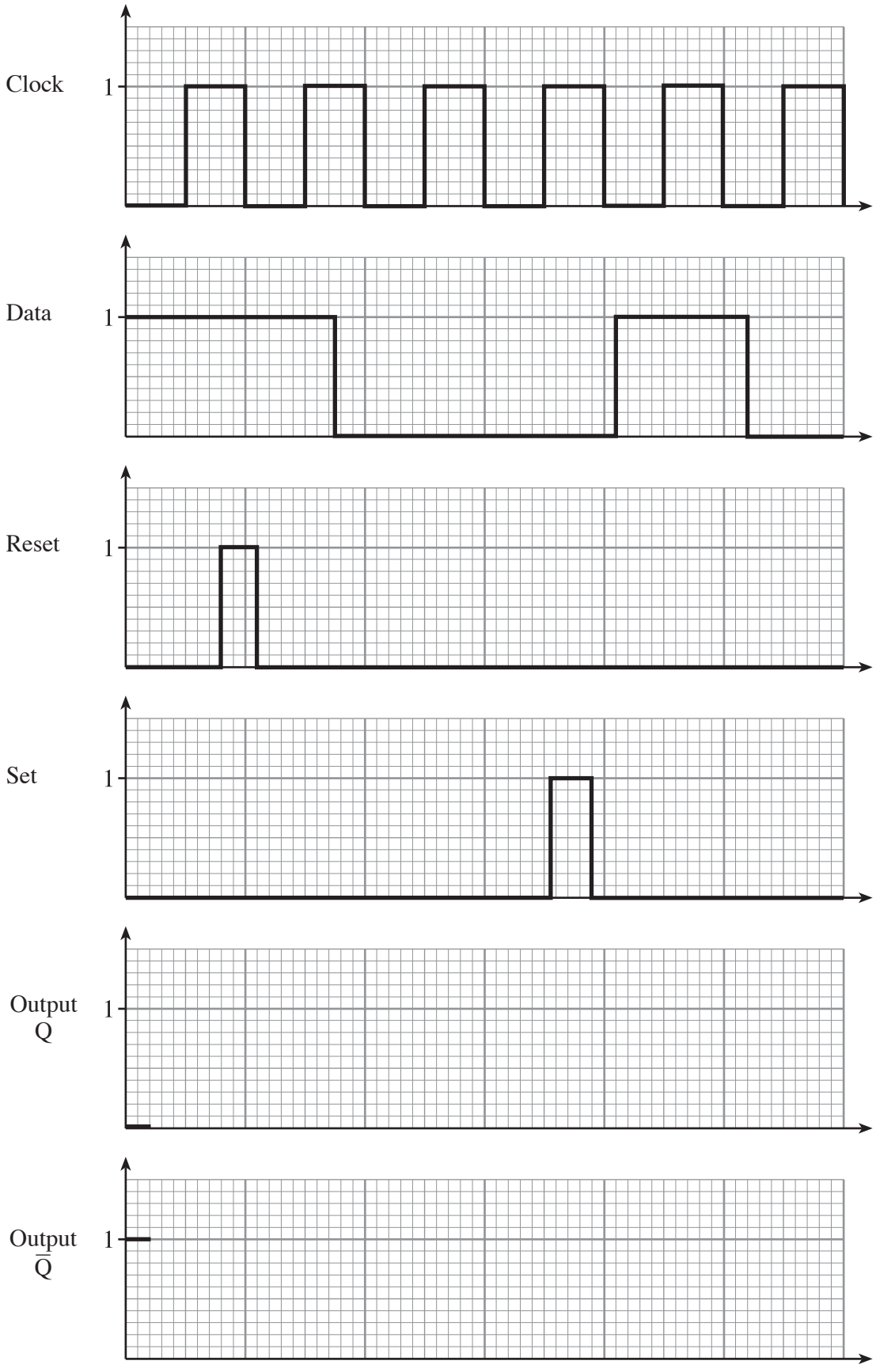
.....

.....

[1]

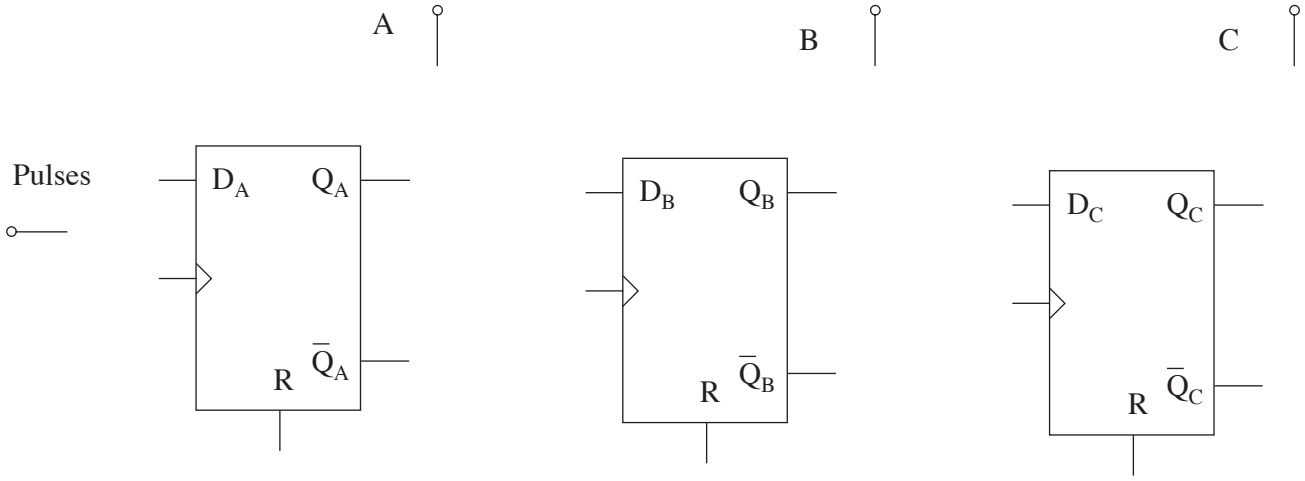
Examiner only

*(b)* The signals shown in the timing diagrams are applied to the D-Type. Complete the timing diagram for both outputs Q and $\overline{Q}$.




[4]

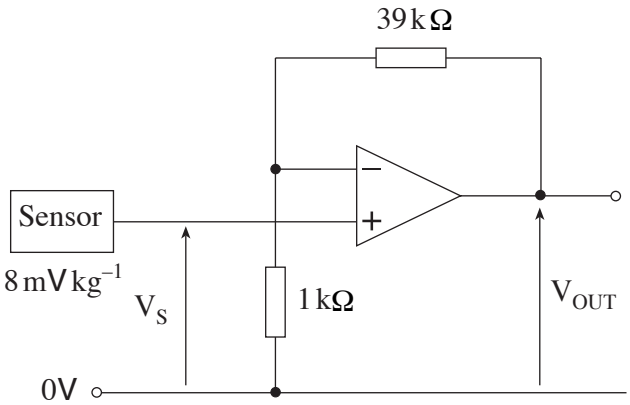
**6.** A system is required to count objects on a conveyor belt. A pulse is produced as each object passes a sensor. The counter is made from 3 D-type flip-flops.




*(a)* Complete the diagram to make a three-bit binary up counter. [3]

*(b)* On the diagram in part *(a)* add a logic gate and the connections necessary to make the counter reset on the fifth clock pulse. [3]

**7.** The circuit diagram shows part of an electronic balance. The output of the sensor changes by 8 mV for each kilogram added to the balance. A non-inverting amplifier, based on an op-amp is then used to process this voltage.




*(a)* What is the voltage gain of the non-inverting amplifier?

.....

.....

[1]

*(b)* The system is adjusted so that the sensor output $V_S = 0$ mV when no load is on the balance. A 12 kg load is then placed on the balance.

(i) Calculate the voltage, $V_S$.

.....

[1]

(ii) Calculate the voltage, $V_{OUT}$.

.....

[1]

*(c)* The output of the op-amp saturates at 16 V.
What is the maximum load that this system can measure?

.....

.....

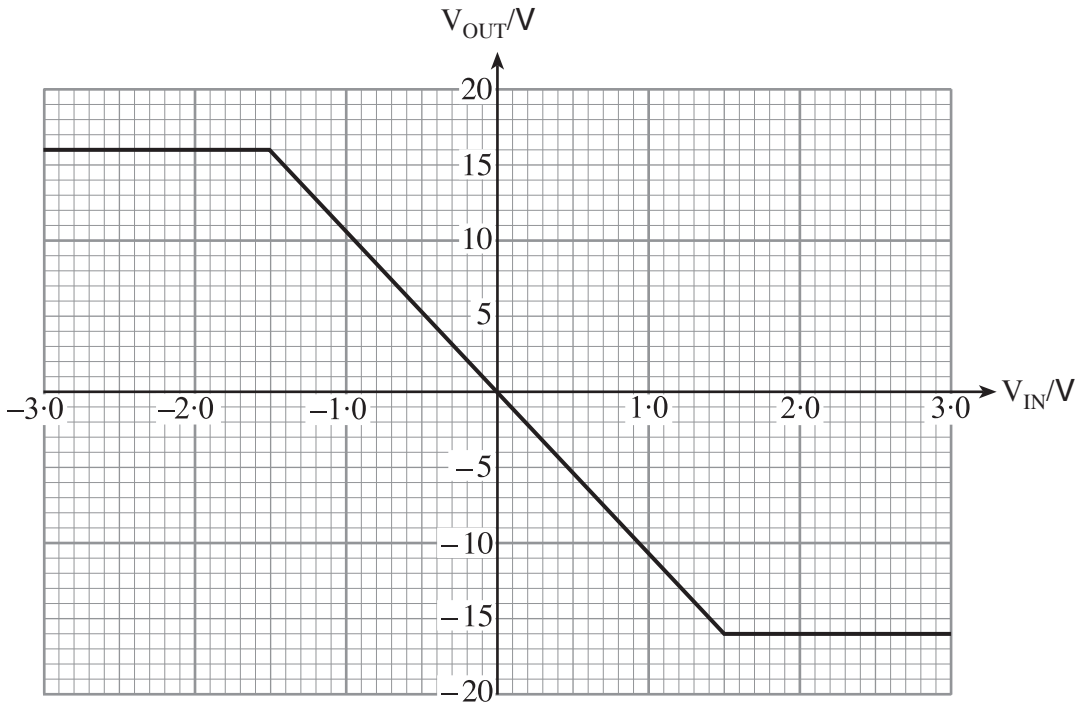
.....

[3]

**8.** The table gives some data about an op-amp.

| Parameter | Value |
|---|---|
| Open-loop gain | $3{\cdot}0 \times 10^5$ |
| Input impedance | $1{\cdot}0 \times 10^7\ \Omega$ |
| Gain-bandwidth product | 5·6 MHz |
| Slew-rate | $3{\cdot}2\ V\mu s^{-1}$ |

The graph shows the voltage transfer characteristic of a voltage amplifier containing this op-amp.




*(a)* Use the graph to determine the voltage gain of this amplifier.

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.....

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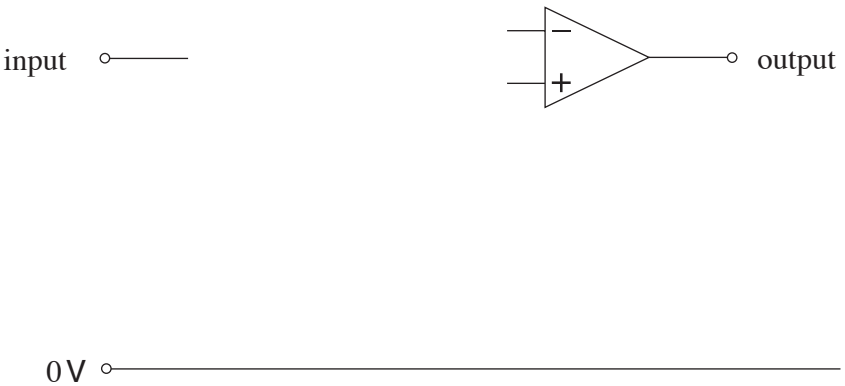
[2]

*(b)* The amplifier is modified to give a voltage gain of –28.

(i) Complete the circuit diagram for a voltage amplifier based on an op-amp which will have a gain of –28.




[3]

(ii) Calculate suitable resistor values to give this gain.

$R_{IN}$ .....

$R_F$ ..... [2]

(iii) State the value of input impedance of this amplifier.

.....

[1]

(iv) Calculate the maximum bandwidth of the amplifier when the voltage gain is –28.

.....

.....

[2]

(v) Calculate the time taken for the output to change from 0 V to 16 V in response to a large step change in input voltage.

.....

.....

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[2]

Examiner only

**FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.**