Candidate Name	Centre Number	Candidate Number

WELSH JOINT EDUCATION COMMITTEE
General Certificate of Education
Advanced Subsidiary/Advanced

CYD-BWYLLGOR ADDYSG CYMRU
Tystysgrif Addysg Gyffredinol
Uwch Gyfrannol/Uwch

381/01

ELECTRONICS

ET1

A.M. TUESDAY, 22 May 2007

(1½ hours)

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

For Examiner's use only.	
1	
2	
3	
4	
5	
6	
7	
8	
Total	

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

RC networks

$V_C = V_O\,(1 - e^{-t/RC})$ for a charging capacitor

$V_C = V_O\,e^{-t/RC}$ for a discharging capacitor

$$t = -RC\ 1n\left(1 - \frac{V_c}{V_o}\right)$$ For a charging capacitor

$$t = -RC\ 1n\left(\frac{V_c}{V_o}\right)$$ For a discharging capacitor

Alternating Voltages $V_o = V_{rms}\sqrt{2}$

Silicon Diode $V_F \approx 0{\cdot}7$ V

Bipolar Transistor

$$h_{FE} = \frac{I_C}{I_B}$$ Current gain

$V_{BE} \approx 0{\cdot}7$ V in the on state

MOSFETs $I_D = g_M V_{GS}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$ Inverting amplifier

$$G = 1 + \frac{R_F}{R_1}$$ Non-inverting amplifier

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$ Summing amplifier

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$ Slew rate

555 Monostable $T = 1{\cdot}1\ RC$

555 Astable

$t_H = 0{\cdot}7\ (R_A + R_B)C$

$t_L = 0{\cdot}7\ R_B C$

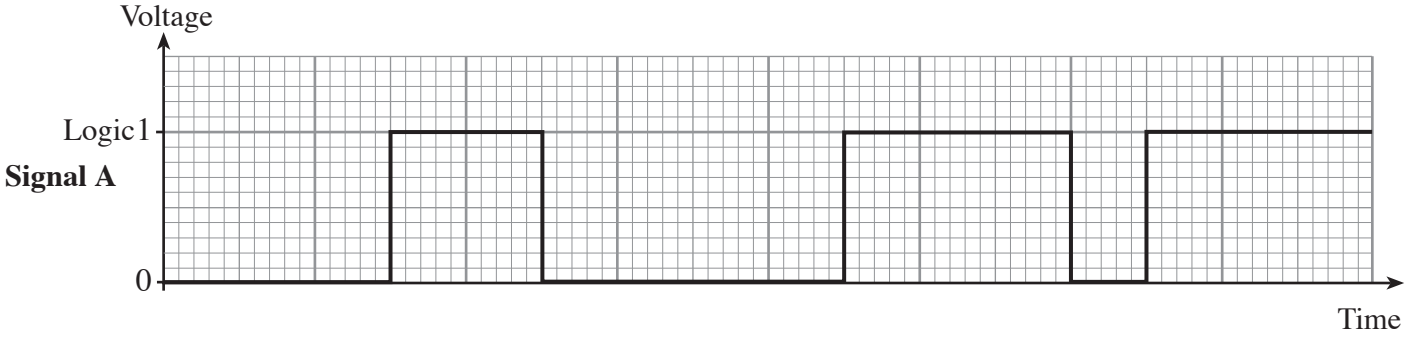
$$f = \frac{1 \cdot 44}{(R_A + 2R_B)C}$$

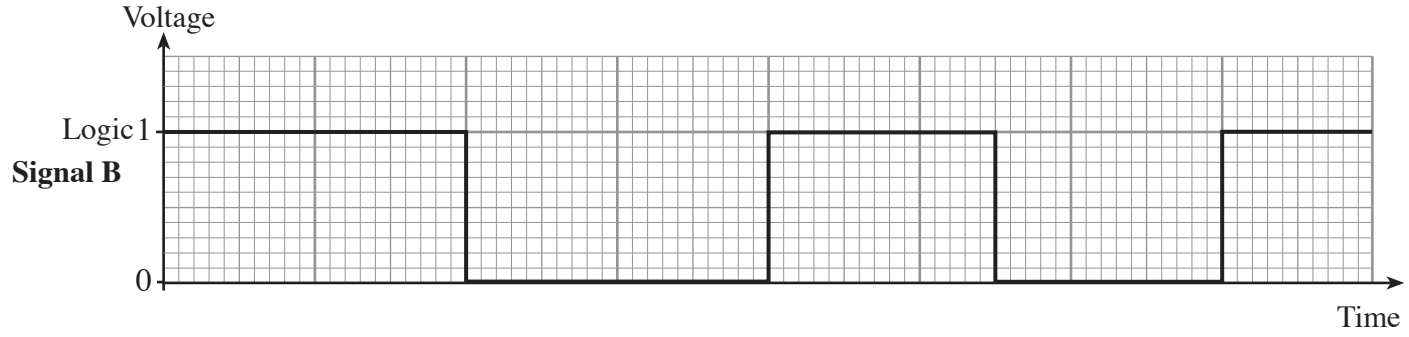
Schmitt Astable

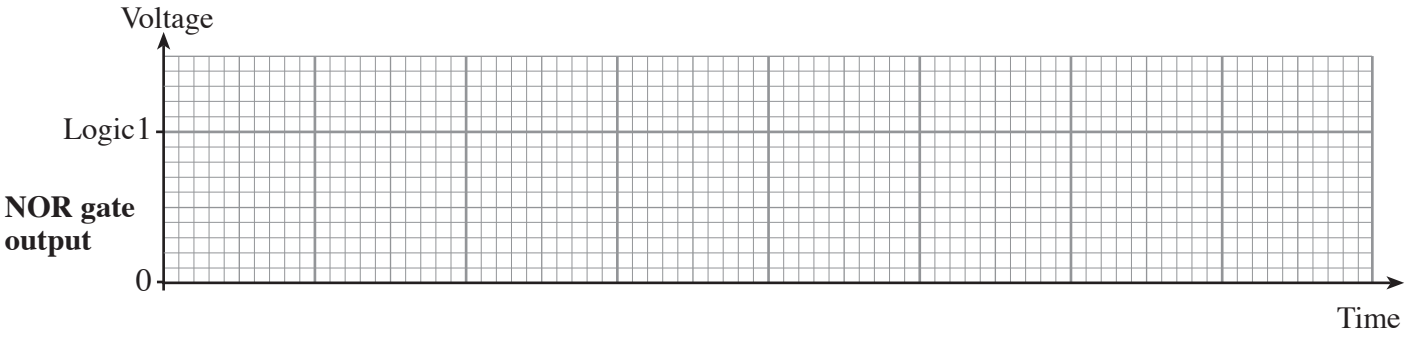
$$f \approx \frac{1}{RC}$$

1. The graphs show two signals **A** and **B**.

(a) Use the axes provided to sketch the output signal when **A** and **B** are applied to the inputs of a 2-input NOR gate. [2]







(b) The following graph shows the output signal from a 2-input logic gate when **A** and **B** are applied to the inputs. What type of gate is it? [1]

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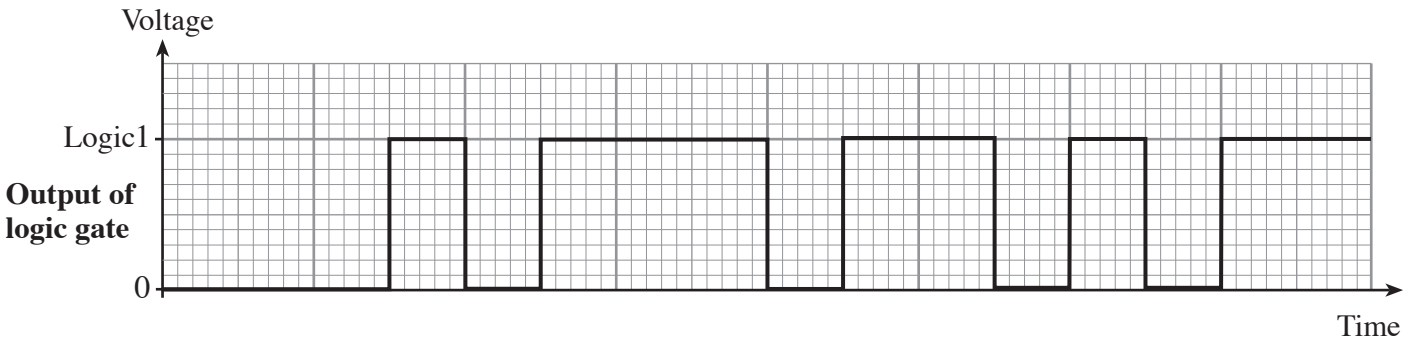
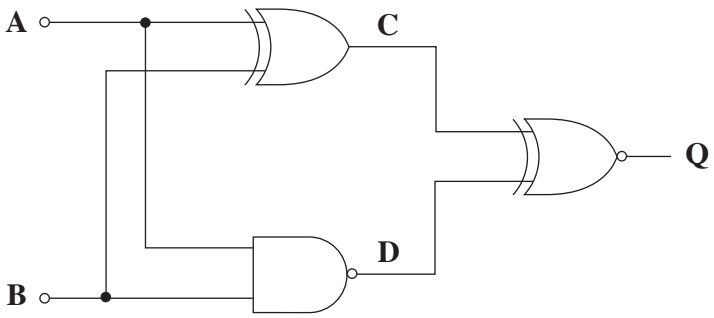


2. A logic system is shown below.



(a) Write down the Boolean expressions for **C**, **D** and **Q** in terms of **A** and **B**. [3]

C = ...

D = ...

Q = ...

(b) Complete the truth table for this system.

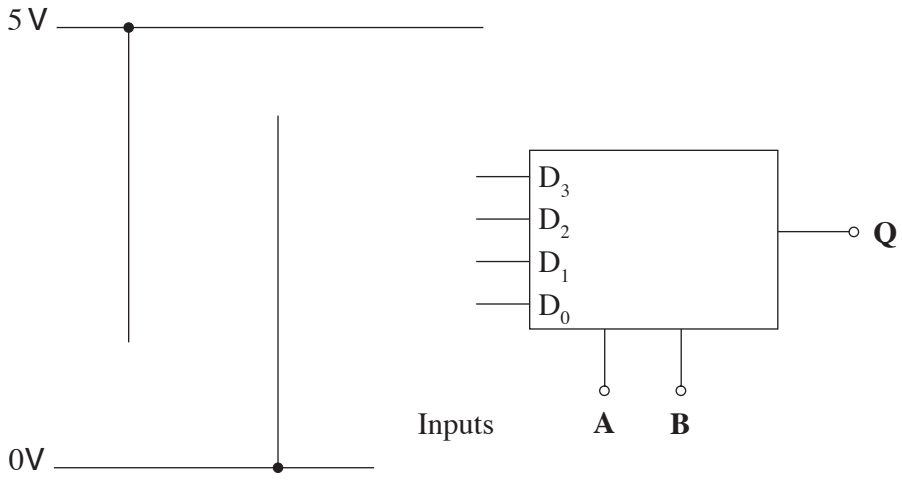
B	A	C	D	Q
0	0			
0	1			
1	0			
1	1			

[3]

(c) Name the single 2-input logic gate that could produce the same function as the **Q** output.

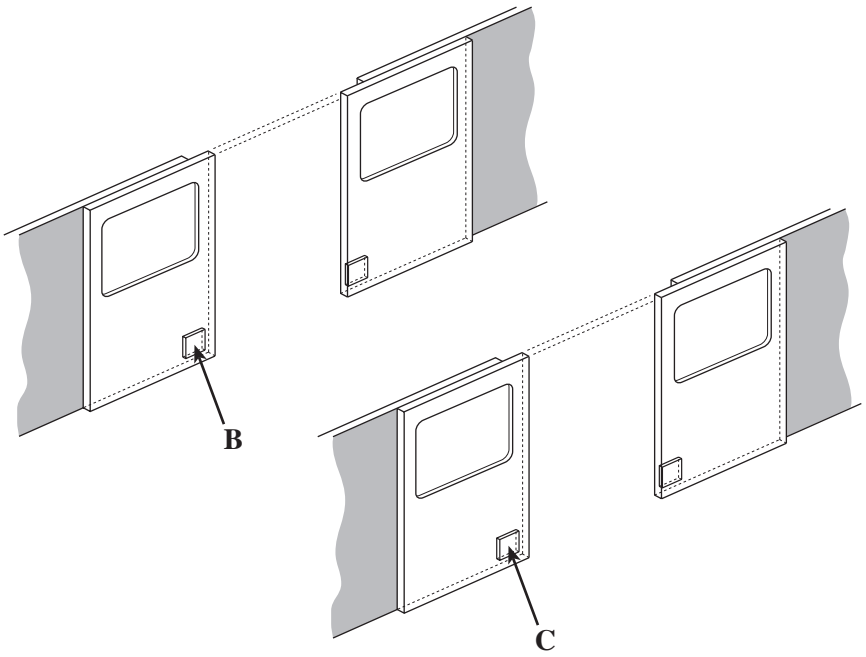
Logic Gate ..... [1]

(d) Show on the following diagram how the same output as **Q** can be generated using a 4 to 1 multiplexer.



[1]

3. An electronic system on a shuttle train sounds an alarm if the doors are still open when the train is about to depart. The diagram shows the doors on either side of the train.



Switch **A** [not shown] is a motion sensor that outputs logic 1 when the train begins to move. When a door is open, its sensor, **B** or **C**, outputs logic 0. The output **Q** of the electronic system becomes logic 1 and triggers the alarm if either or both doors are open as the train begins to move.

(a) Complete the truth table for the electronic system.

C	B	A	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[2]

(b) Write down the Boolean expression for **Q** in terms of **A**, **B** and **C**.
There is no need to simplify it. [2]

.....

4. *(a)* Simplify the following expressions, showing all stages of your working.

(i) $B + 1 =$ ..... [1]

(ii) $A.B + A.\overline{B} =$ .....

..... [2]

(b) Using either a Karnaugh map or the rules of Boolean algebra, simplify the following expression as much as possible.

$$\overline{D}.\overline{C}.\overline{B}.\overline{A} + \overline{D}.C.A + \overline{D}.\overline{B}.\overline{A} + D.C.A + \overline{D}.B.\overline{A}$$

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D.C \ B.A	0.0	0.1	1.1	1.0
0.0				
0.1				
1.1				
1.0				

[4]

(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{A}.B + \overline{B}}$$

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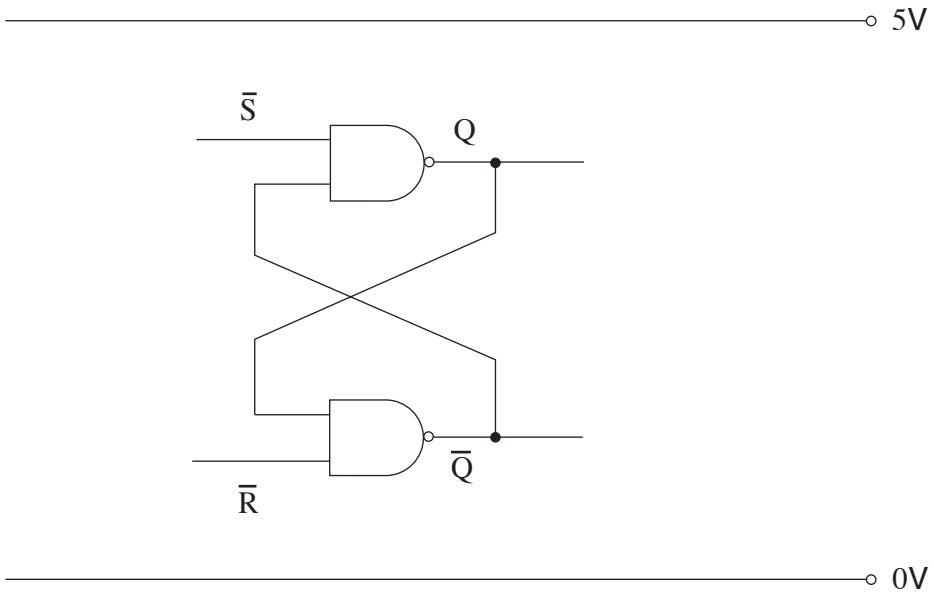
5. The circuit diagram shows one part of an alarm system.



(a) Inputs $\overline{S}$ and $\overline{R}$ are operated in the following sequence. Complete the truth table to show how the outputs Q and $\overline{Q}$ respond.

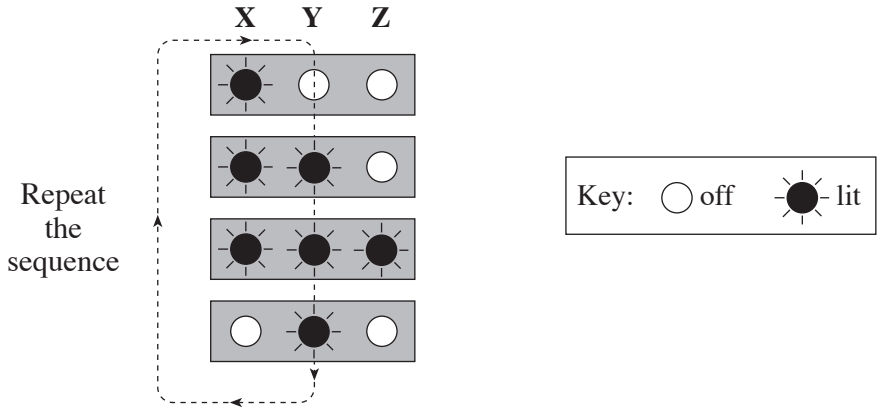
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
1	1	0	
0	1		
1	1		
1	0		
1	1		

[3]

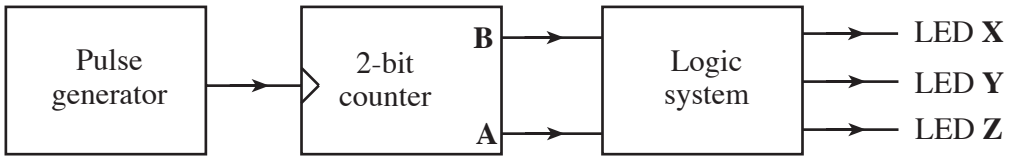
(b) Add a switch and resistor to the $\overline{S}$ input on the diagram, which can be used to **set** Q to logic 1 when the switch is pressed. [2]

(c) Add to the diagram to show how an LED can be used to indicate the logic state of $\overline{Q}$. The LED should be ON when $\overline{Q}$ is **sinking a current**. [2]

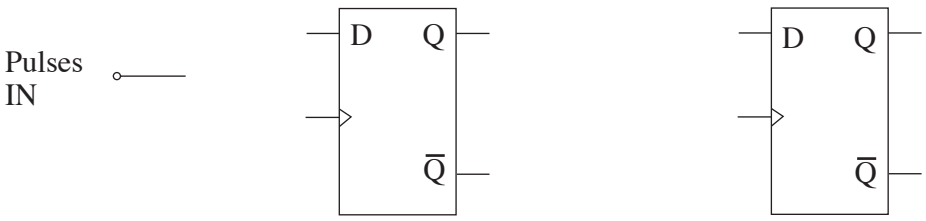
6. A student builds a light sequencer effect, using three LED's, **X**, **Y** and **Z**. The sequence is shown in the following diagram.



The block diagram of the system is shown below.



(a) Complete the diagram to show how two rising-edge-triggered D-type flip-flops can be connected to make a 2-bit binary up-counter.



[2]

(b) Complete the truth table for the logic system. A logic 1 causes an LED to light.

B	A	X	Y	Z
0	0			
0	1			
1	0			
1	1			

[1]

(c) Design a suitable logic system for the light sequencer, using logic gates. Complete the following diagram with your design. Credit will be given for solutions that use the least number of logic gates.

[3]

(d) Redraw the circuit using 2-input NAND gates only.

[2]

(e) Why is it often cheaper to reduce a circuit to NAND gates only?

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[1]

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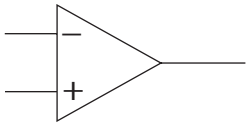
7. *(a)* Complete the circuit diagram for an op-amp inverting amplifier. Label V_{IN} and V_{OUT}.



[3]

(b) Choose suitable resistor values to give the amplifier an input impedance of $2\,k\Omega$ and a voltage gain of -60. **Label the circuit diagram with these values.** [2]

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(c) How could the input impedance of this amplifier be doubled **without changing the gain**? [1]

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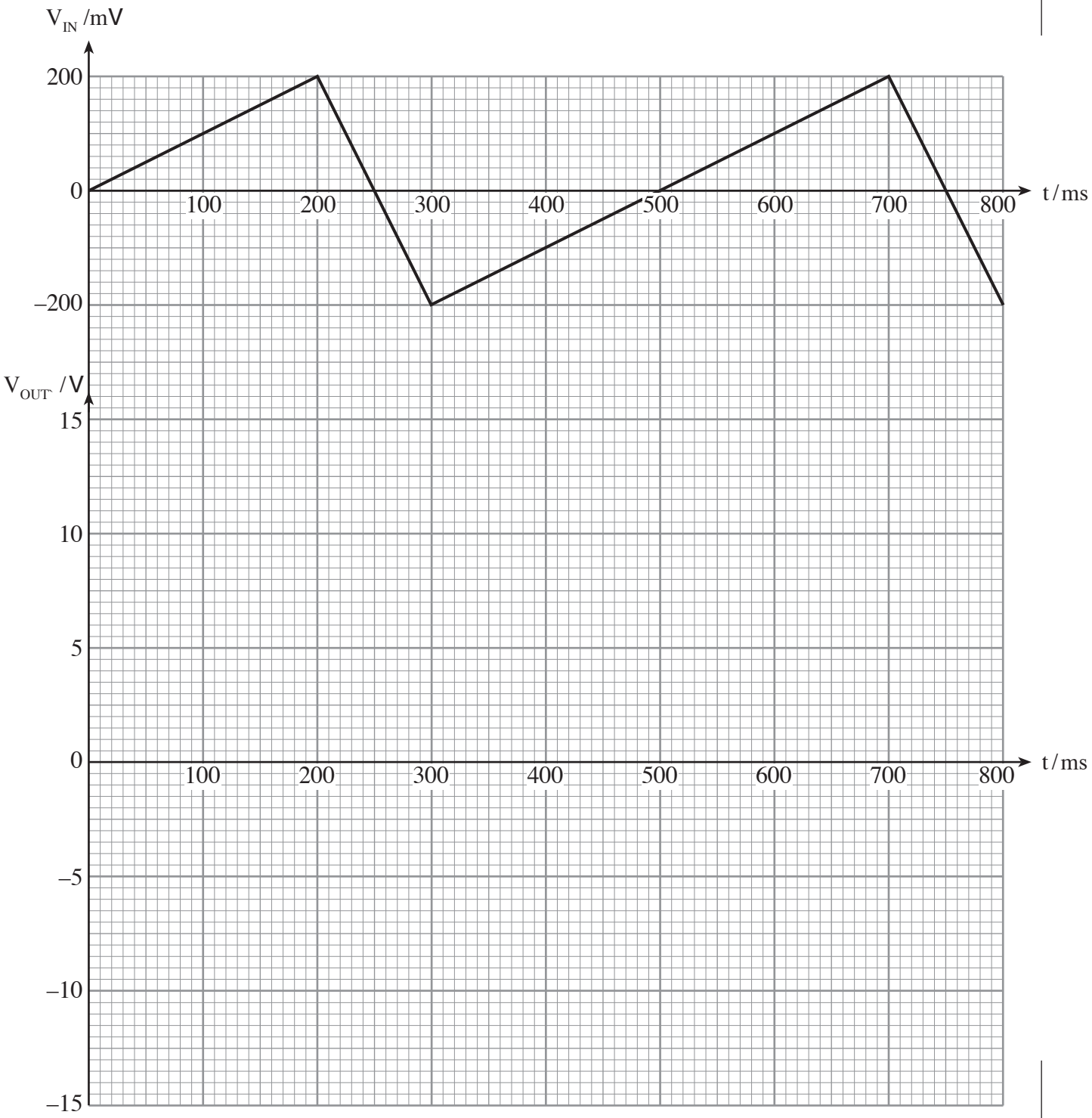
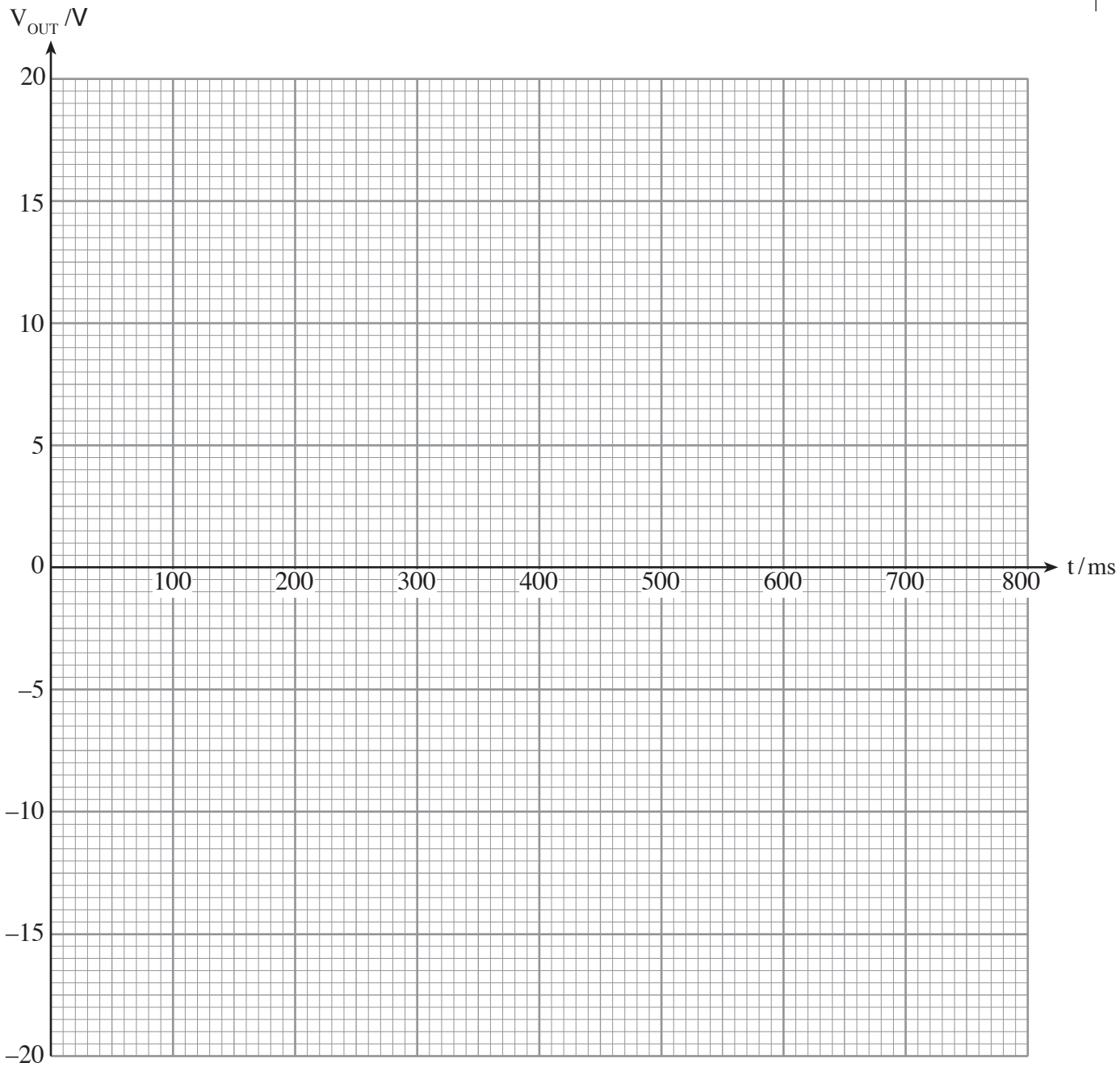
This amplifier (gain – 60) is powered from ± 15 V power supply and saturation occurs at ± 14 V.

(d) The signal V_{IN} is applied to the input. Draw the output voltage V_{OUT} on the axes provided. Label any important voltage values on the axes.



[3]

(e) The input signal is now changed to ± 300 mV. Use the axes provided to sketch the resulting output signal.



[2]

8. When designing op-amp circuits, careful consideration needs to be given to their different parameters. The following table is an extract from the date sheet of a typical op-amp.

Max.supply voltage/V	± 20
Input imdedance/Ω	5×10^6
Open loop gain	2×10^5
Max. output current/mA	24
Gain bandwidth product/MHz	4
Slew Rate/Vμs^{-1}	1·36

(a) Calculate the time for the output to change from +17 V to –17 V for a large step change in input voltage. [2]

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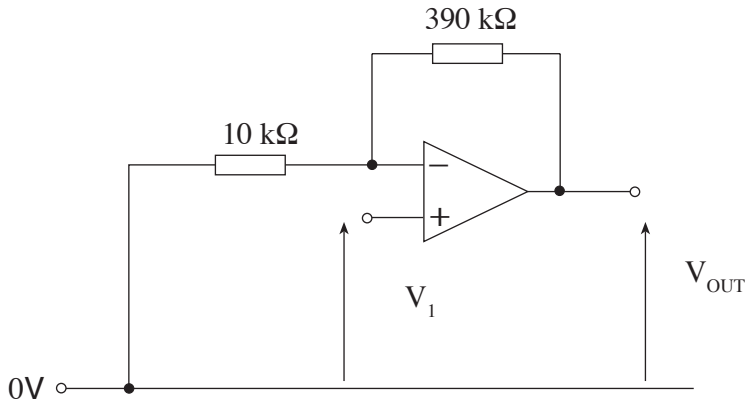
The following diagram shows this op-amp set up as a voltage amplifier.



(b) (i) What is the input impedance of this amplifier? [1]

.....

(ii) Calculate the voltage gain of this amplifier. [1]

.....

.....

(iii) What is the bandwidth of **this** amplifier? [2]

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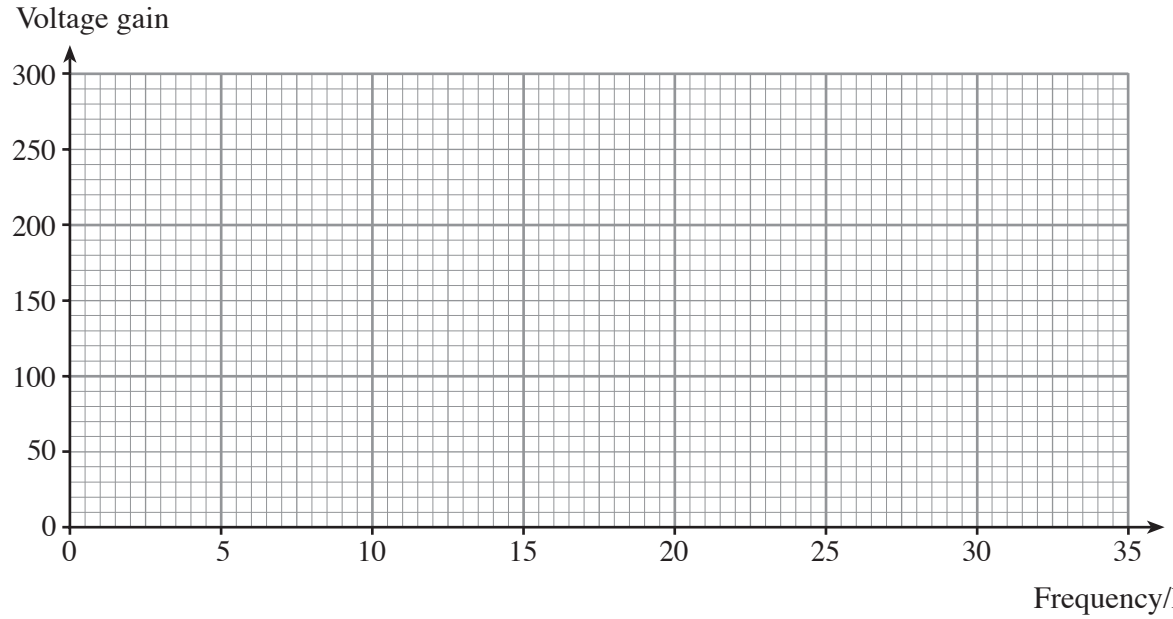
.....

(c) The values of the resistors are **changed** to give the amplifier a voltage gain of 200 with a bandwidth of 20 kHz. Use the axes provided to sketch the frequency response of the amplifier.



[2]

FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.