Candidate Name	Centre Number	Candidate Number

WELSH JOINT EDUCATION COMMITTEE
General Certificate of Education
Advanced Subsidiary/Advanced

CYD-BWYLLGOR ADDYSG CYMRU
Tystysgrif Addysg Gyffredinol
Uwch Gyfrannol/Uwch

381/01

ELECTRONICS

ET1

P.M. TUESDAY, 16 January 2007

(1½ hours)

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

For Examiner's use only.	
1	
2	
3	
4	
5	
6	
7	
8	
9	
Total	

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

RC networks

$V_C = V_O\,(1 - e^{-t/RC})$ for a charging capacitor

$V_C = V_O\,e^{-t/RC}$ for a discharging capacitor

$t = -RC\ 1n\left(1 - \frac{V_c}{V_o}\right)$ For a charging capacitor

$t = -RC\ 1n\left(\frac{V_c}{V_o}\right)$ For a discharging capacitor

Alternating Voltages $V_o = V_{rms}\sqrt{2}$

Silicon Diode $V_F \approx 0{\cdot}7$ V

Bipolar Transistor $h_{FE} = \frac{I_C}{I_B}$ Current gain

$V_{BE} \approx 0{\cdot}7$ V in the on state

MOSFETs $I_D = g_M V_{GS}$

Operational amplifier $G = -\frac{R_F}{R_{IN}}$ Inverting amplifier

$G = 1 + \frac{R_F}{R_1}$ Non-inverting amplifier

$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$ Summing amplifier

$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$ Slew rate

555 Monostable $T = 1{\cdot}1\ RC$

555 Astable $t_H = 0{\cdot}7\ (R_A + R_B)C$

$t_L = 0{\cdot}7\ R_B C$

$f = \frac{1 \cdot 44}{(R_A + 2R_B)C}$

Schmitt Astable $f \approx \frac{1}{RC}$

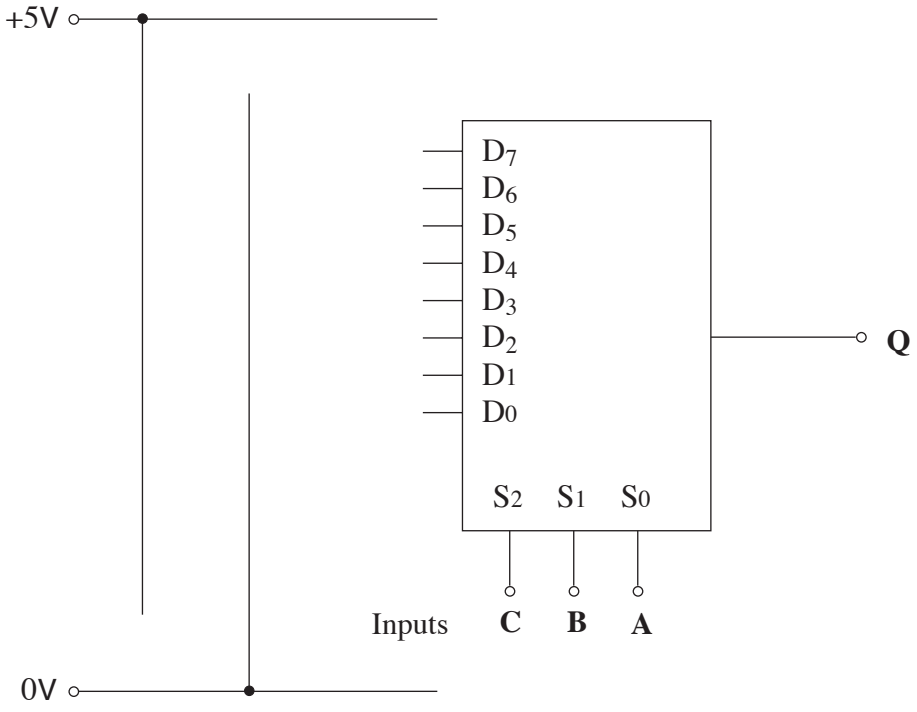
1. A logic system gives the following truth table.

C	B	A	Q
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**0**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**0**

Write down the Boolean expression for **Q** in terms of **A**, **B** and **C**.
Do **not** simplify the Boolean expression.

Q = ... [2]

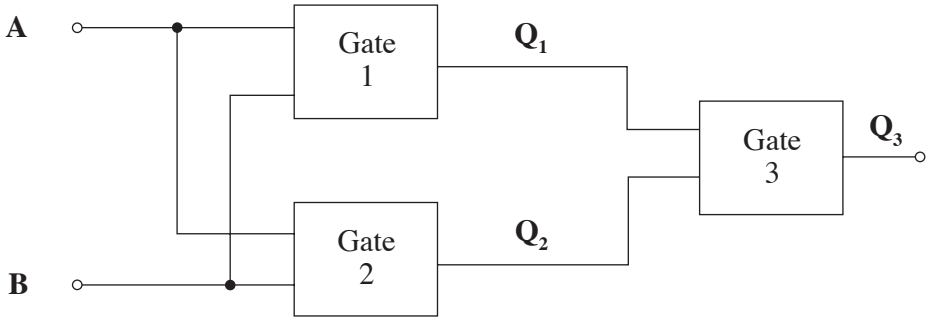
(b) Show on the following diagram how the same **Q** output can be generated using an 8 to 1 multiplexer.



[2]

2. The truth table shows the values of two inputs **A** and **B** and the corresponding outputs $\mathbf{Q_1}$, $\mathbf{Q_2}$ and $\mathbf{Q_3}$ of the three logic gates of the system shown below.

A	**B**	$\mathbf{Q_1}$	$\mathbf{Q_2}$	$\mathbf{Q_3}$
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	0	1	1



(a) Identify the gate used in each case.

Gate 1 .....

Gate 2 .....

Gate 3 .....

[3]

(b) Write down the Boolean expressions for the signals at $\mathbf{Q_1}$, $\mathbf{Q_2}$ and $\mathbf{Q_3}$ **in terms of the inputs A and B.**

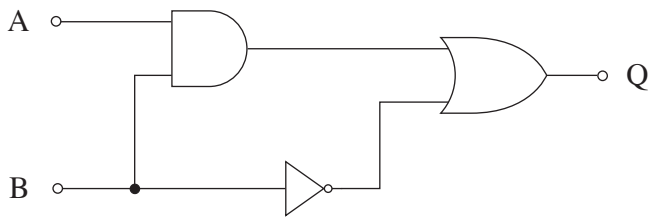
$\mathbf{Q_1}$ = ...

$\mathbf{Q_2}$ = ...

$\mathbf{Q_3}$ = ...

[3]

3. The diagram below shows a logic system.



(a) (i) In the space below, draw the same logic system, but with the logic gates replaced by their NAND gate equivalents.

[3]

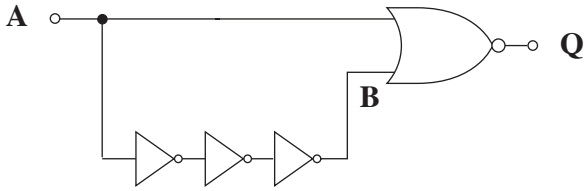
(ii) How many **pairs** of redundant gates are there in this system?

..... pairs [1]

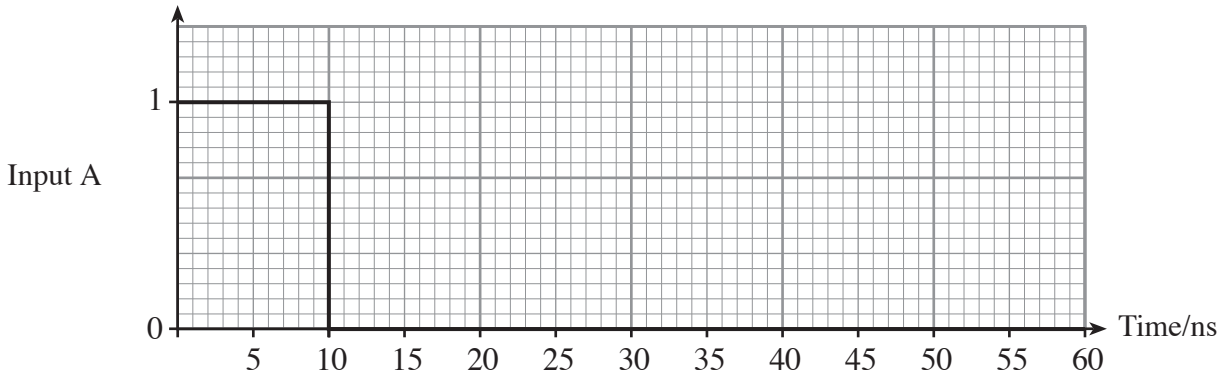
(b) Redraw **the simplified system** in the space below.

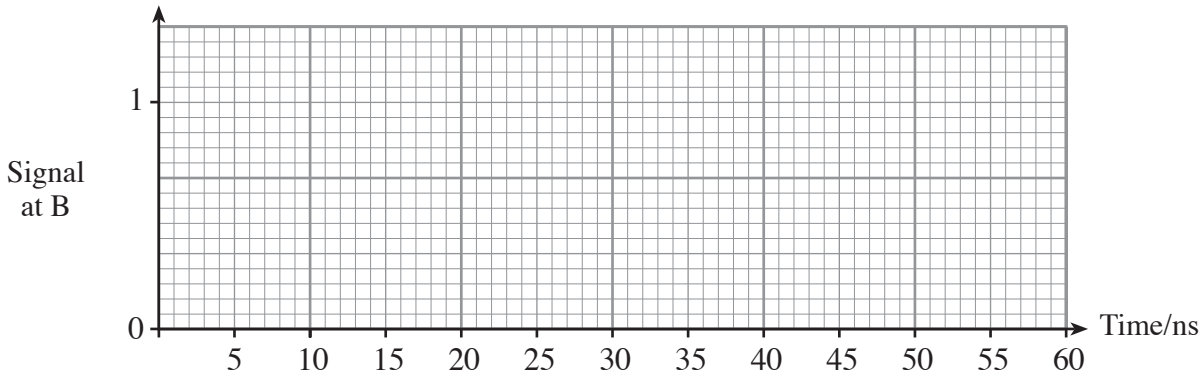
[1]

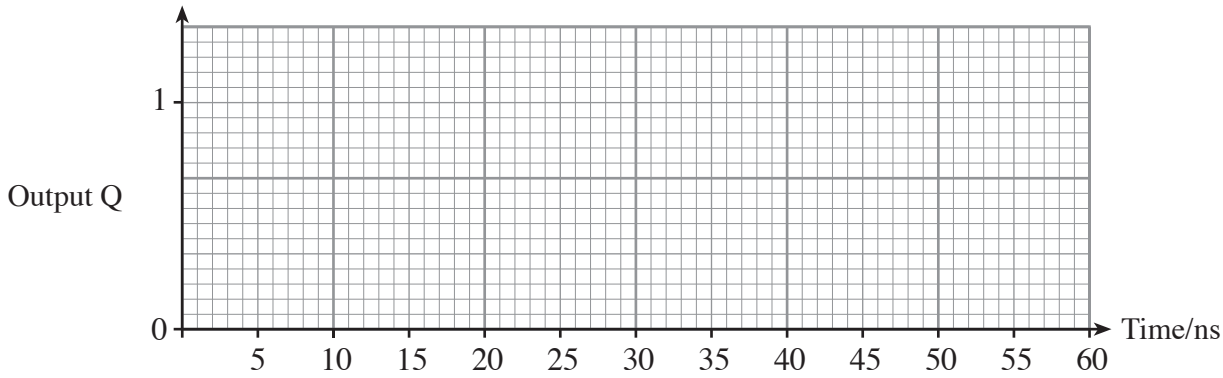
4. The following transition gate is used to provide edge-triggering.
Each gate has a propagation delay of 5ns.



Complete the following diagram to show how the signal at **B** and the output **Q** change when the pulse shown is applied to input **A**.
Initially, output Q is at logic 0.







[4]

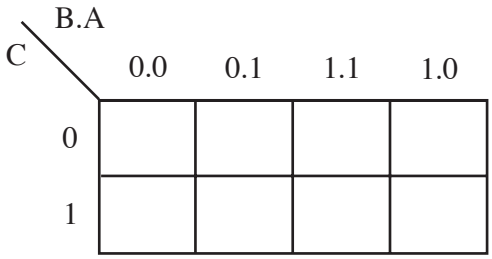
5. *(a)* Simplify each of the Boolean expressions as much as possible.

(i) $\overline{A}.1 =$ .....

(ii) $\overline{B}.\overline{B} =$ ..... [2]

(b) Draw the Karnaugh map that corresponds to the following Boolean expression.

$Q = A.\overline{B} + A.B.C + \overline{C}$



[1]

(c) Apply DeMorgan's theorem to the following expression and simplify the result.

$\overline{\overline{A}.\overline{B.C}} =$ .....

.....

.....

[3]

(d) In designing a logic system, a student has produced the Karnaugh map shown below.

D.C \ B.A	0.0	0.1	1.1	1.0
0.0	1	0	1	0
0.1	1	0	1	0
1.1	1	1	0	0
1.0	1	1	0	0

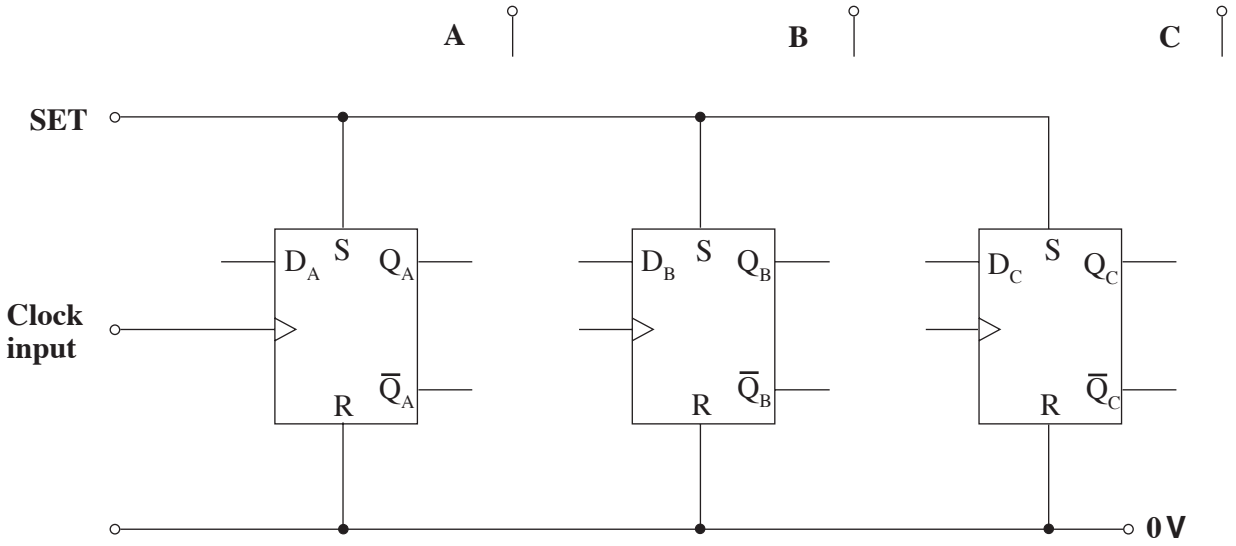
Give the simplest Boolean expression for the output Q of this logic system.
Show, on the Karnaugh map any groups that you create in producing this expression.

.....

.....

[4]

6. The diagram shows 3 D-type flip-flops, which form part of a binary **down-counter**. Output's A, B and C are used to indicate the binary output. A is the **least significant** bit.



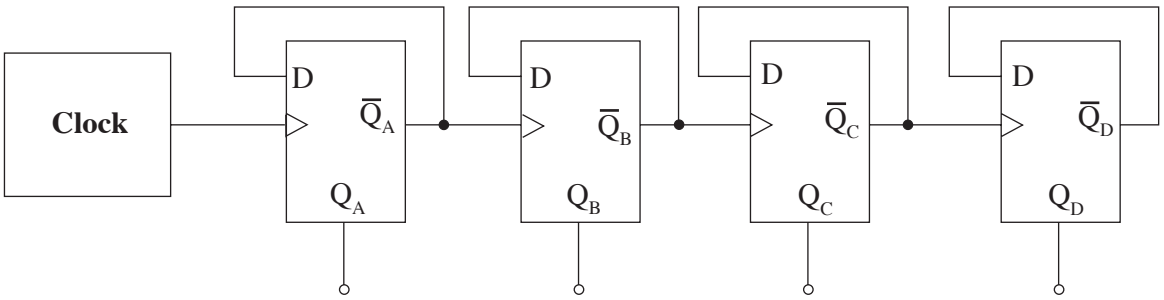
(a) Complete the diagram to make a three bit binary **down-counter**. [3]

(b) The SET input is momentarily taken to logic 1 and back to logic 0 producing the initial state shown in the table. Complete the table, using **0** or **1**, to indicate the logic state of each output after the stated number of clock pulses.

	OUTPUT C	**OUTPUT B**	**OUTPUT A**
Initial State	**1**	**1**	**1**
After **ONE** clock pulse			
After **TWO** clock pulses			
After **FIVE** clock pulses			

[3]

7. The clock in the diagram produces a square wave output of 1 MHz. This is fed into a series of 4 D-type flip-flops, which are rising-edge triggered.



(a) What is the frequency at the output Q_A of the first D type flip-flop? [1]

.....

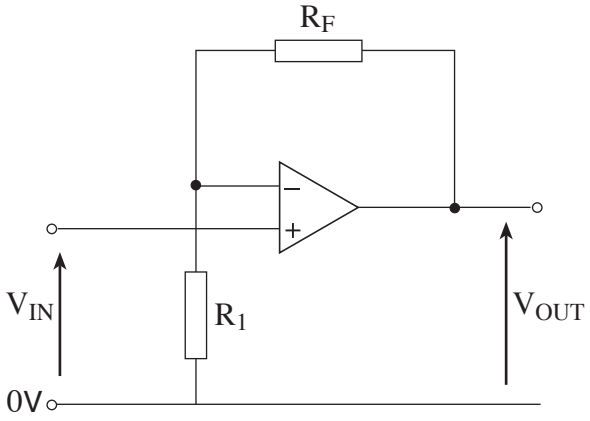
(b) Which output will produce a frequency of 125 kHz? [1]

.....

(c) The timing diagram below shows the output from the clock.
Complete the diagram to show the signal at outputs Q_A, Q_B and Q_C.

[3]

8. The circuit diagram shows an op-amp connected as a voltage amplifier.
The amplifier uses a ±15 V power supply and saturates at ±14 V.

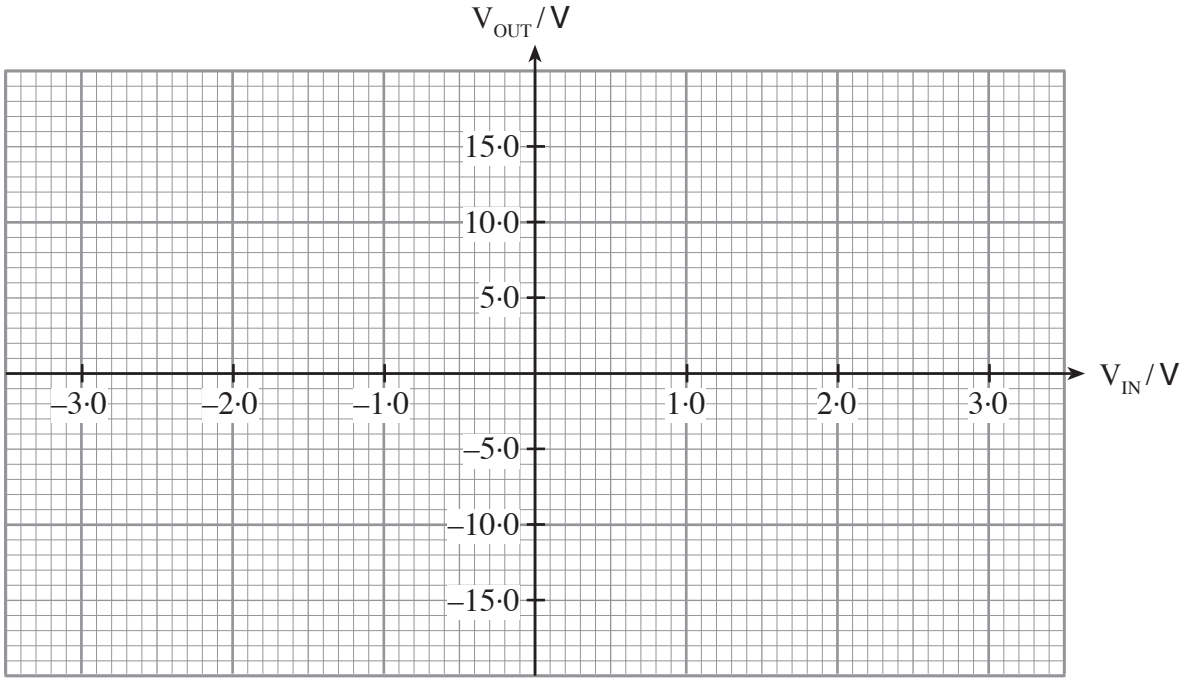


(a) Choose suitable resistor values such that this amplifier has a voltage gain of 6.6.

R_1 = ...

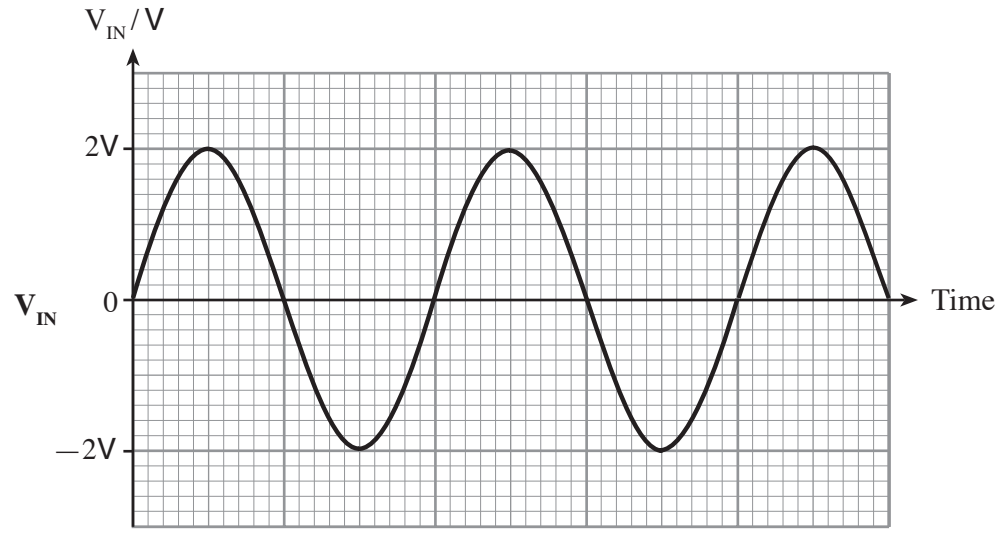
R_F = ... [2]

(b) Use the axes below to sketch the voltage characteristics for this amplifier.



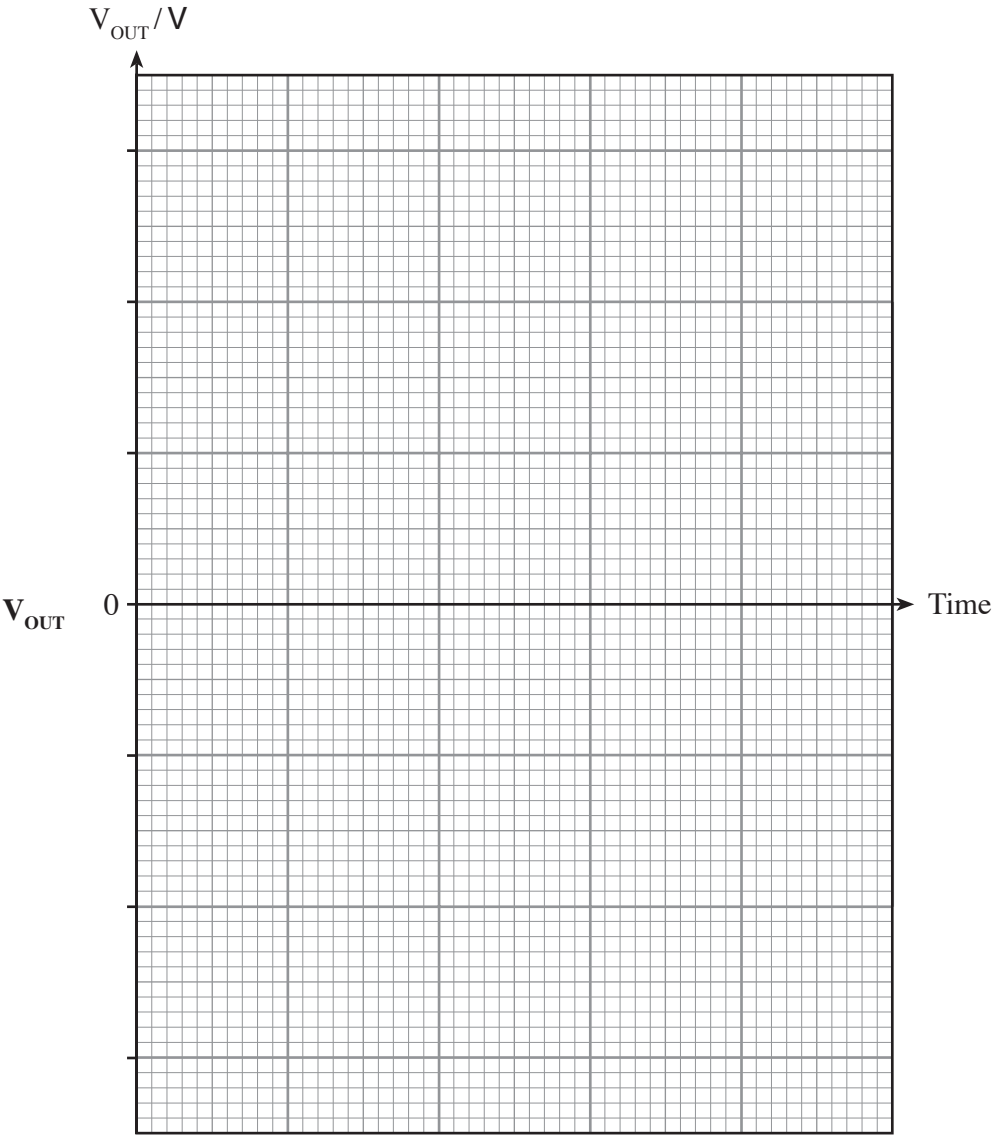
[3]

(c) The signal V_{IN} is applied to the input.



(i) Determine the peak value of V_{OUT}. .....

(ii) Draw the output voltage on the axes provided. Label important voltage values on the axes.

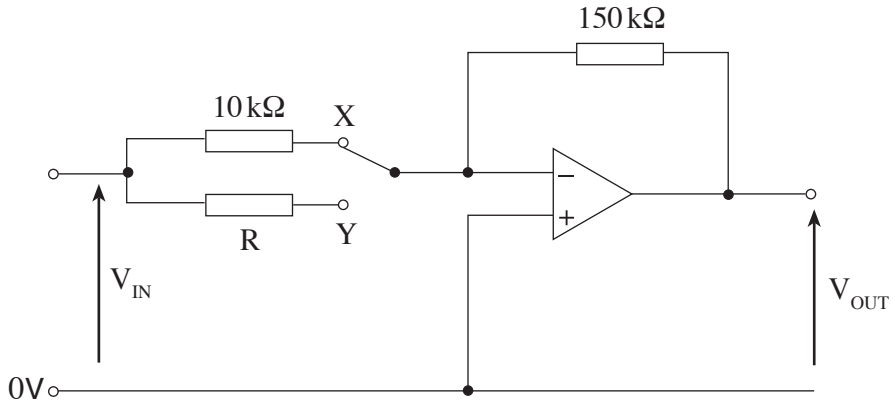


[3]

9. An extract from the data sheet of an op-amp is shown in the following table.

Parameter	Value
Input Impedance	10 MΩ
Output Impedance	100 Ω
Open Loop Gain	10^5
Gain Bandwidth Product	1·2 MHz
Slew Rate	6 Vμs^{-1}

The circuit diagram shows an op-amp set up as a voltage amplifier. The switch allows the user to change the gain of the amplifier.



The op-amp is powered from a ±12 V supply and saturation occurs at ±11 V.

An input voltage of 0·6 V is applied to V_{IN}.

(a) The switch is initially connected to position **X**.

(i) Determine the input impedance of the amplifier.

.....

(ii) Calculate the voltage gain of the amplifier.

.....

.....

(iii) Calculate the output voltage when $V_{IN} = 0{\cdot}6$ V.

.....

(iv) Calculate the bandwidth of the amplifier.

.....

.....

[6]

(b) The switch is moved to position **Y**. This doubles the gain of the amplifier.

(i) Calculate the value of resistor **R**.

.....

.....

(ii) Determine the output voltage for $V_{IN} = 0{\cdot}6\,V$.

.....

.....

[2]

(c) State what change, **if any**, has occurred to the following after the switch is moved from position **X** to **Y**.

(i) The **output** impedance .....

(ii) The bandwidth .....

[2]

(d) Calculate the time for the output voltage to change from +9 V to –9 V in response to a large step-change in input voltage.

.....

.....

.....

.....

[2]

FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.