Candidate Name	Centre Number	Candidate Number

WELSH JOINT EDUCATION COMMITTEE
General Certificate of Education
Advanced

CYD-BWYLLGOR ADDYSG CYMRU
Tystysgrif Addysg Gyffredinol
Uwch

385/01

ELECTRONICS

ET5

P.M. TUESDAY, 13 June 2006

($1\frac{3}{4}$ hours)

ADDITIONAL MATERIALS

In addition to this examination paper you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number, and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

Your attention is drawn to the Information for the Use of Candidates on page 2 and 3 of this paper.

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

For Examiner's use only.	
1	
2	
3	
4	
5	
6	
7	
8	
Total	

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

RC networks	$V_C = V_O\,(1 - e^{-t/RC})$	for a charging capacitor
	$V_C = V_O\,e^{-t/RC}$	for a discharging capacitor
	$t = -RC\ 1n\left(1 - \frac{V_c}{V_o}\right)$	For a charging capacitor
	$t = -RC\ 1n\left(\frac{V_c}{V_o}\right)$	For a discharging capacitor
Alternating Voltages	$V_o = V_{rms}\sqrt{2}$	
	$X_C = \frac{1}{2\pi fC}$	Capacitive reactance
	$X_L = 2\pi fL$	Inductive reactance
	$f_0 = \frac{1}{2\pi\sqrt{LC}}$	Resonant frequency
	$f_{co} = \frac{1}{2\pi RC}$	Cut-off frequency for high pass and low pass filters
	$\phi = \tan^{-1}\frac{R}{X_C}$	Phase shift between V_R and V_c.
Silicon Diode	$V_F \approx 0{\cdot}7V$	
Bipolar Transistor	$h_{FE} = \frac{I_C}{I_B}$	Current gain
	$V_{BE} \approx 0{\cdot}7V$	in the on state
MOSFETs	$I_D = g_M V_{GS}$	

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$ Inverting amplifier

$$G = 1 + \frac{R_F}{R_1}$$ Non-inverting amplifier

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$ Summing amplifier

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$ Slew rate

$$V_{OUT} = V_{DIFF}\left(\frac{R_F}{R_1}\right)$$ Difference amplifier

$$V_L \approx V_Z\left(1 + \frac{R_F}{R_1}\right)$$ Stabilised power supply

Power Amplifier

$$P_{MAX} = \frac{V_S^2}{8R_L}$$ where V_S is rail-to-rail voltage

555 Monostable $T = 1{\cdot}1\ RC$

555 Astable $t_H = 0{\cdot}7\ (R_A + R_B)C$

$t_L = 0{\cdot}7\ R_BC$

$$f = \frac{1\cdot 44}{(R_A + 2R_B)C}$$

Schmitt Astable

$$f \approx \frac{1}{RC}$$

Turn over.

BLANK PAGE

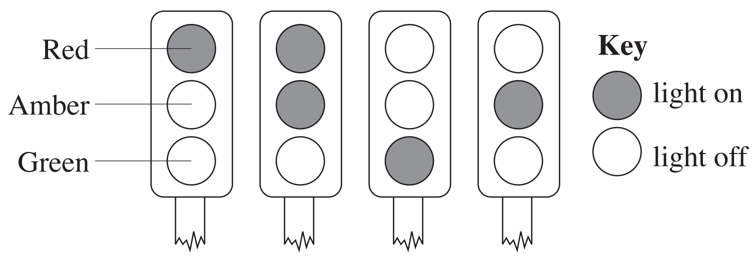
1. *(a)* A synchronous counter is used as a sequence generator to control traffic lights. Unused states can stop a sequence generator from functioning properly. Explain how this can occur. [1]

....

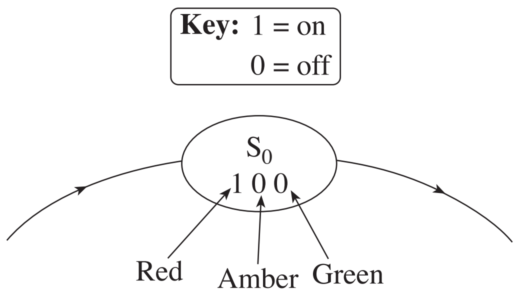
....

....

(b) The diagram illustrates the sequence for this set of traffic lights.



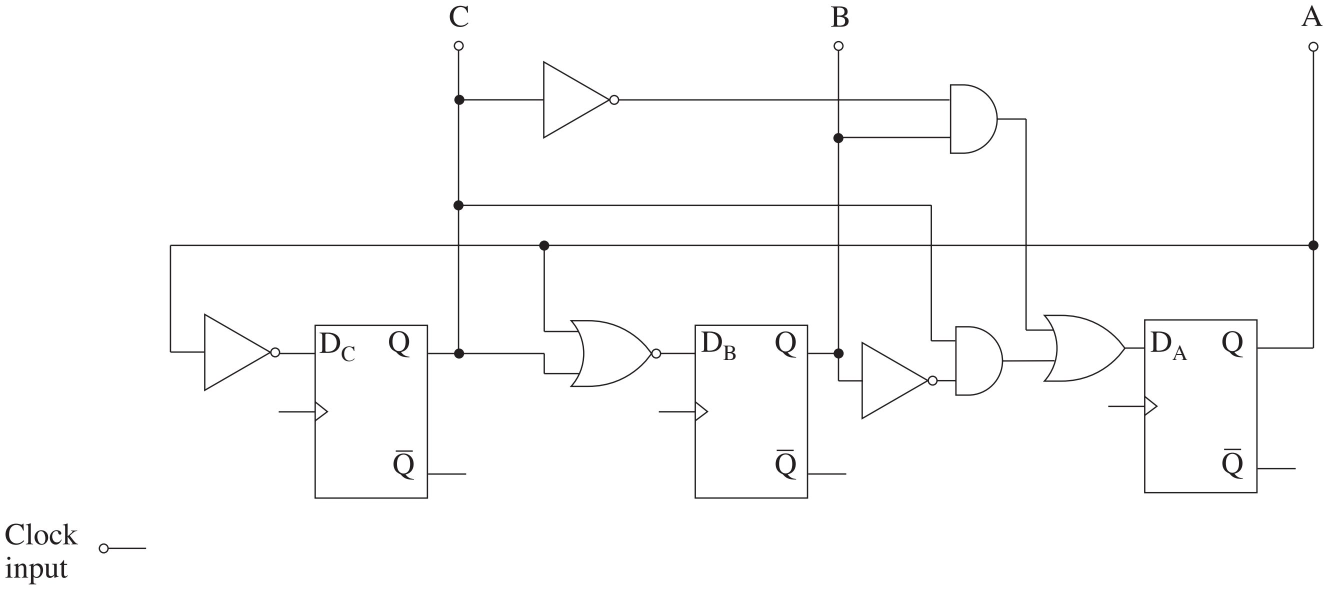
(i) Complete the **main sequence** in the state diagram for this traffic light system. [2]



(ii) Complete the state diagram by adding the **unused states**, so that there are no *stuck states*. [1]

Turn over.

2. Here is part of the circuit diagram for a synchronous counter.



(a) Complete the circuit diagram by adding the correct connections for the clock inputs of the D-type flip-flops. [1]

(b) The Boolean expression for the input D_A is:

$D_A = \overline{C}.B + C.\overline{B}$

Give the Boolean expressions for the inputs D_C and D_B in terms of the outputs C, B and A. [2]

D_C = ...

D_B = ...

....

(c) Complete the table to show the sequence of states produced by this system.
*You should find that there are **five** different states in the main sequence.*

State	C	B	A	D_C	D_B	D_A
0	0	0	0			
1						
2						
3						
4						

[5]

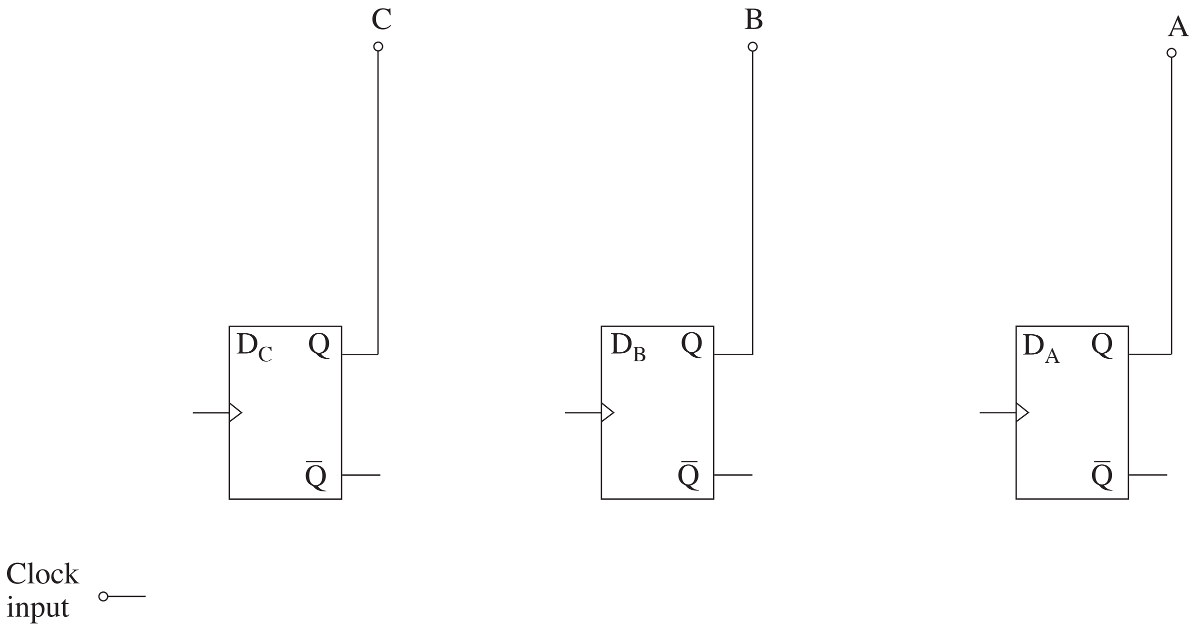
(d) Complete the following table by:

(i) identifying any unused states,

(ii) determining the values of D_C, D_B and D_A which they produce. [4]

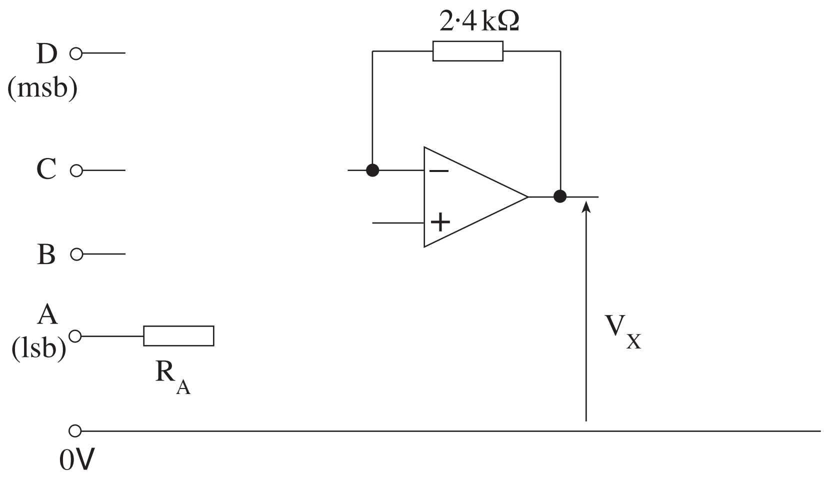
Unused state			Produces		
C	B	A	D_C	D_B	D_A

(e) As shown in the diagram, the circuit requires seven logic gates. It can be built using only two logic gates, without changing the behaviour of the system.
Complete the following circuit diagram to show how this can be done. [3]



Examiner only
Arholwr yn unig

3. *(a)* Complete the circuit diagram for a 4-bit DAC. [2]



(b) Logic 1 in this system is represented by a +10V signal, and logic 0 by a 0V signal. The response of the DAC is linear. The table illustrates the performance of the system.

Input	Output V_X/V
0000	0
0001	-0·8
1111	-12

(i) Calculate voltage V_X when the output is 0011. [1]

....

(ii) Calculate a suitable value for the resistor R_A. [2]

....

....

....

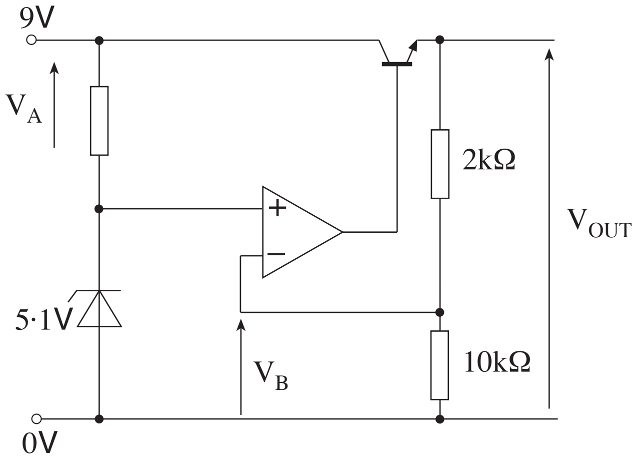
(iii) Hence determine the values of the other resistors used in this circuit. Add labels to the circuit diagram to show these values. [2]

....

(c) The output voltages V_X from the DAC are negative.
Modify the circuit diagram by adding another op-amp, configured as an inverting amplifier, so that the final output voltage range is from 0V to +12V.
Labels all resistors used with appropriate values. [3]

Examiner only
Arholwr yn unig

4. The following subsystem is part of a power supply unit.



(a) Calculate:

(i) the voltage V_A; [1]

....

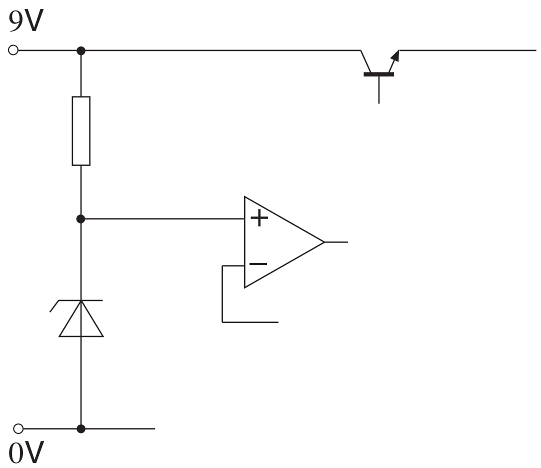
(ii) the output voltage V_{OUT}; [1]

....

(iii) the voltage V_B at the inverting input of the op-amp. [1]

....

(b) (i) Modify the circuit by adding a second transistor and any other components needed to provide short-circuit protection. Complete the following diagram to show your modification. [2]



(ii) This modification must prevent currents greater than 1A. Calculate suitable values for any resistors used. [1]

....

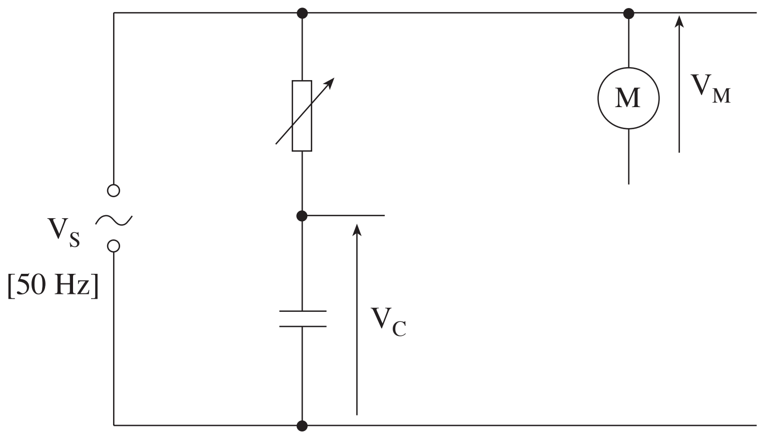
....

....

Turn over.

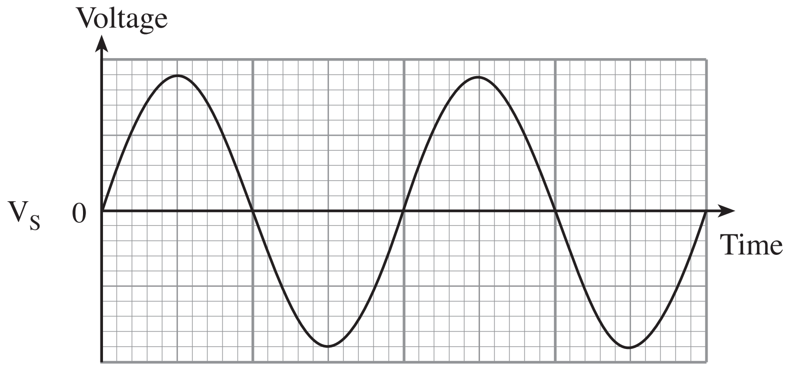
Examiner only
Arholwr yn unig

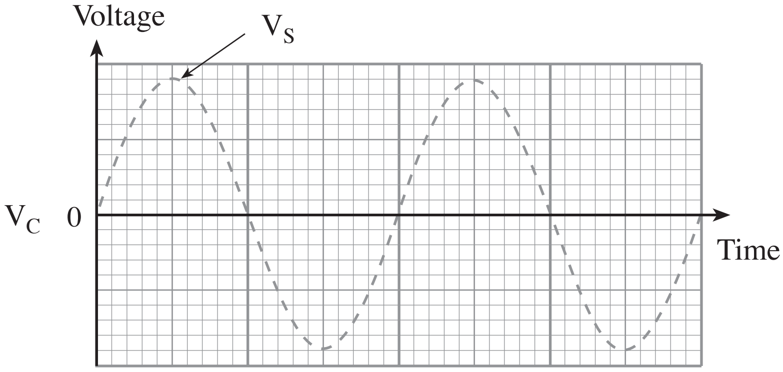
5. The circuit diagram shows part of a speed control system for a motor.



(a) Complete the circuit diagram for the control system by adding a thyristor and a diac, using the correct circuit symbols. [3]

(b) (i) The variable resistor is set to give a phase shift of 45° between V_S, the 50 Hz AC supply voltage, and V_C, the voltage across the capacitor.
Use the axes provided below to sketch the waveform for V_C, with the 45° phase shift.
The upper graph shows V_S, the AC supply waveform. [2]





(iii) The capacitor has a capacitance of 1μF.

Use the equation $R = X_C \tan \phi$ to calculate the setting of the variable resistor needed to give a phase shift of 45°. [2]

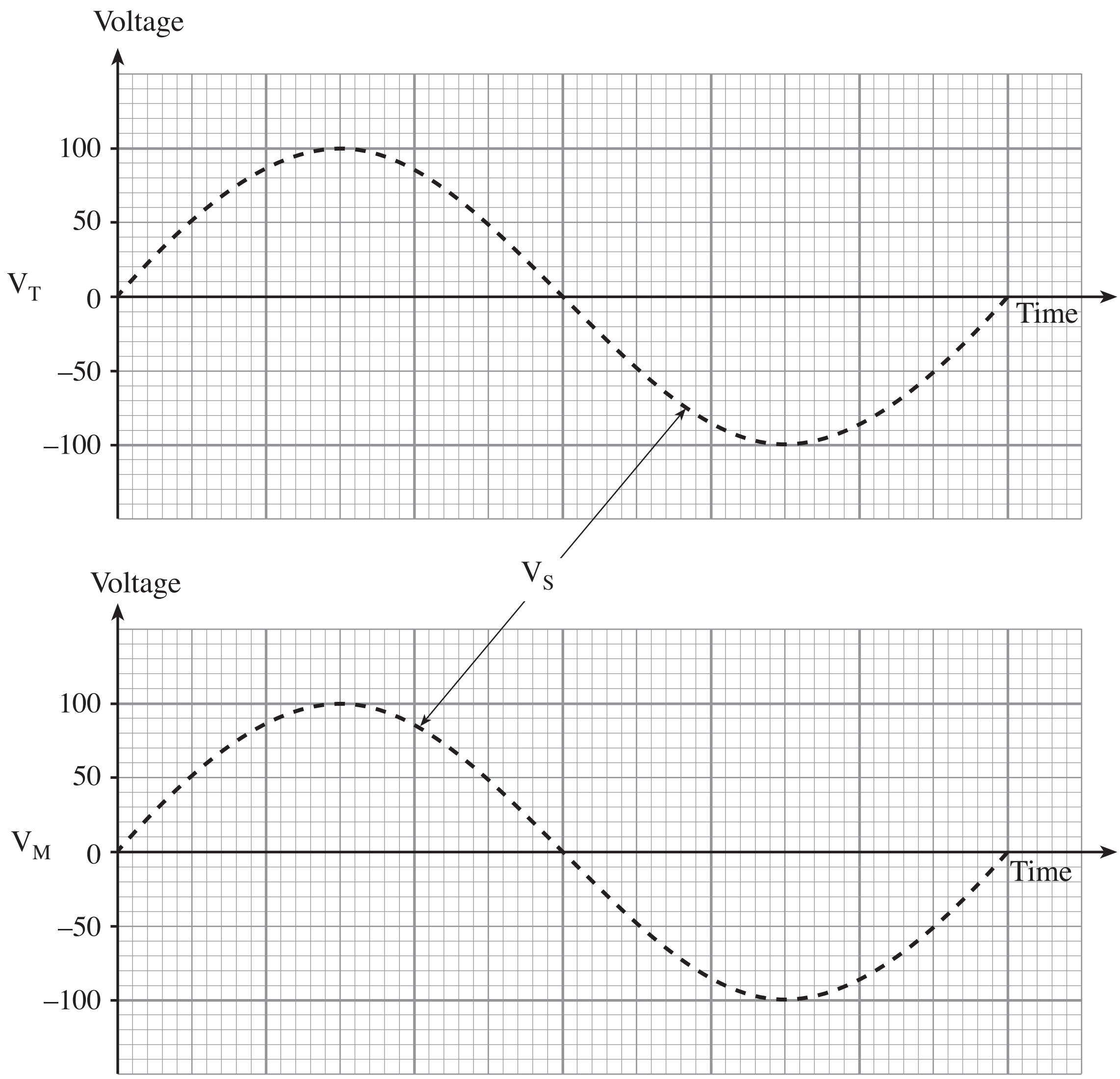
....

....

....

Examiner only *Arholwr yn unig*

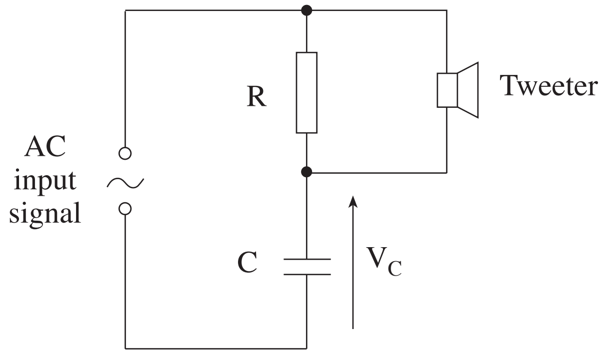
(c) The variable resistor is now set to give a phase shift of 0°. The thyristor conducts when V_C reaches 25V.
Uses the axes provided to sketch the waveforms for the voltage V_T across the thyristor, and V_M across the motor. The waveform of the supply voltage V_S is shown as a dotted line. [3]



Turn over.

Examiner only
Arholwr yn unig

6. *(a)* The circuit diagram shows a passive filter connected to a tweeter. A tweeter is a loudspeaker designed to reproduce only high frequency sounds.



As the signal frequency increases, what happens to:

(i) the reactance of the capacitor; [1]

....

(ii) the resistance of the resistor; [1]

....

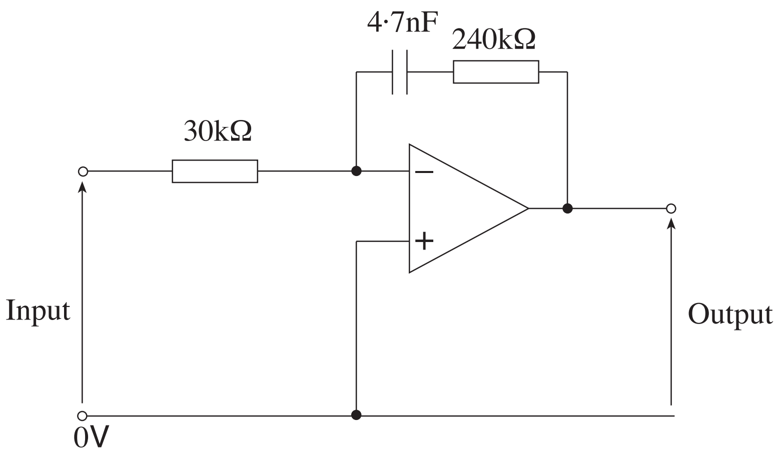
(iii) the voltage V_C across the capacitor; [1]

....

(iv) the voltage across the tweeter? [1]

....

(b) Another audio system uses the following active filter.



(i) What type of active filter is this? [1]

....

(ii) What will be the reactance of the capacitor at the break frequency? [1]

....

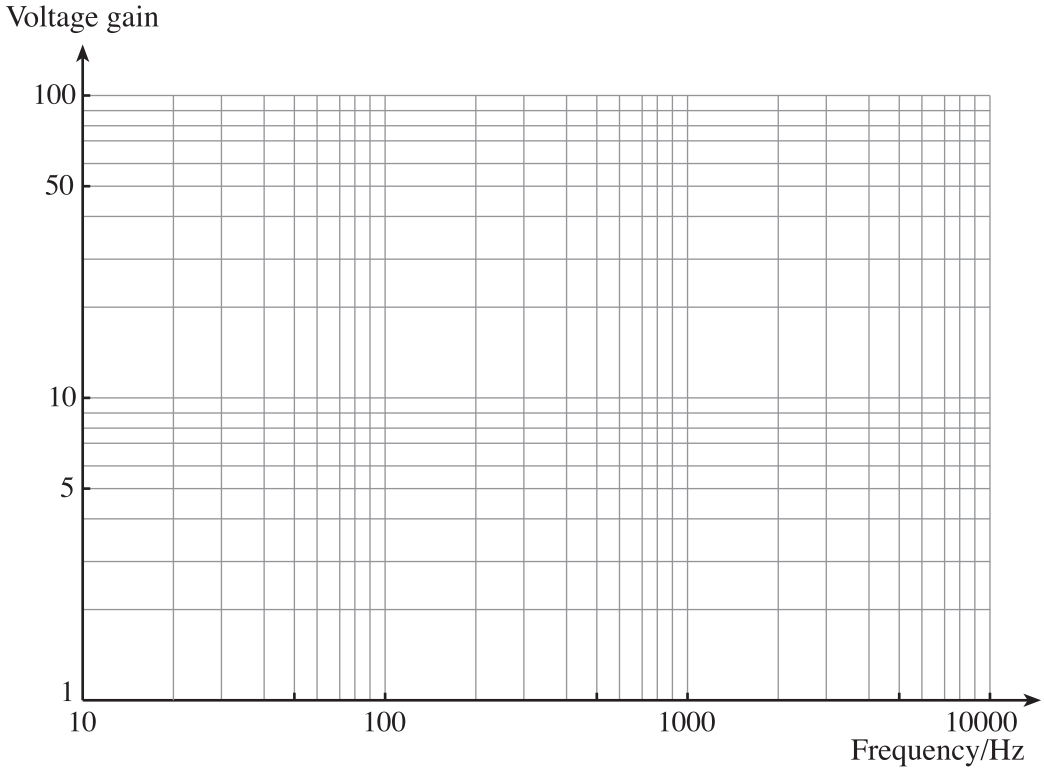
(iii) Calculate the break frequency for this filter. [2]

....

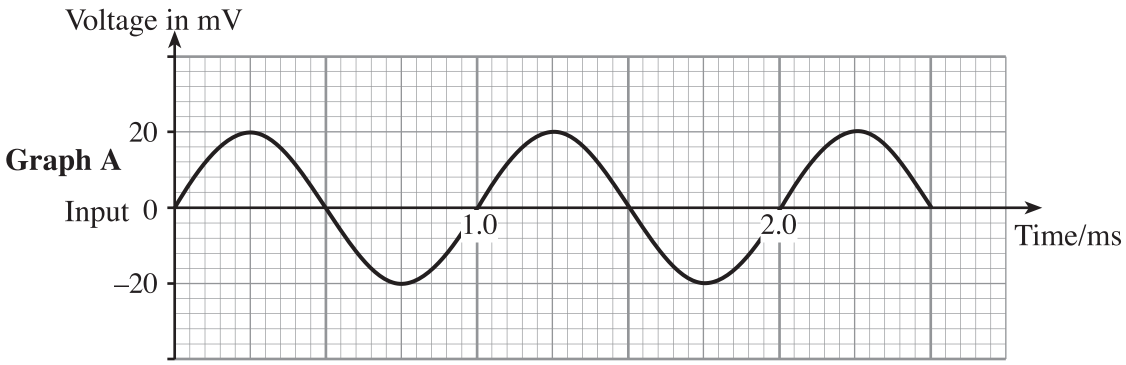
....

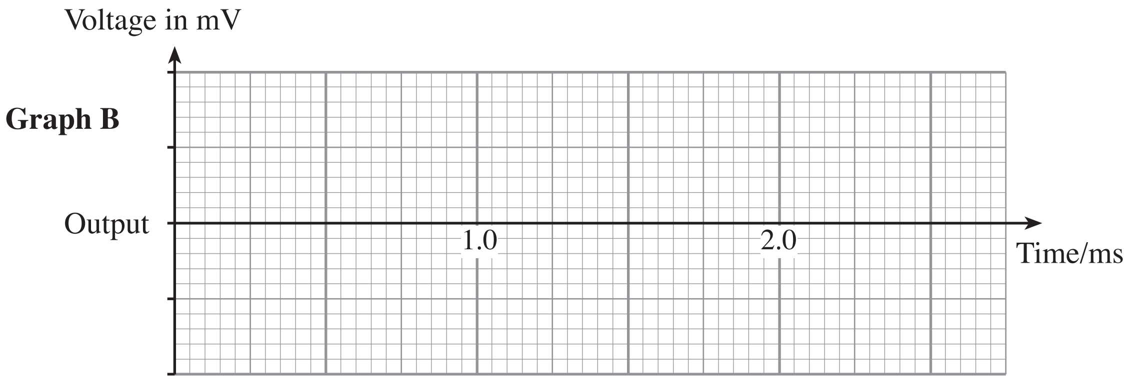
....

(iv) Sketch the frequency response for this filter, using the axes provided. [3]



(v) The test signal shown in **Graph A** is applied to the input of this filter.
Sketch the output signal produced, using the axes provided in **Graph B**.
Label the voltage axis with a suitable scale. [2]

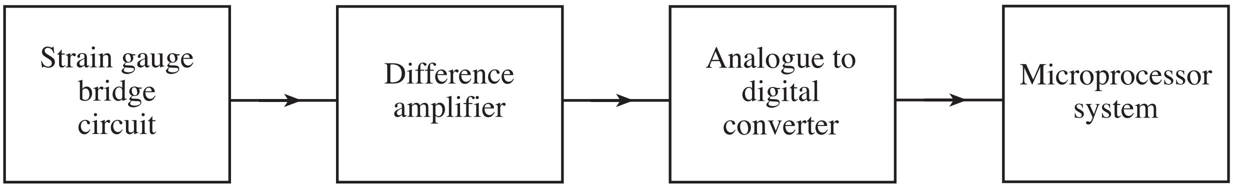




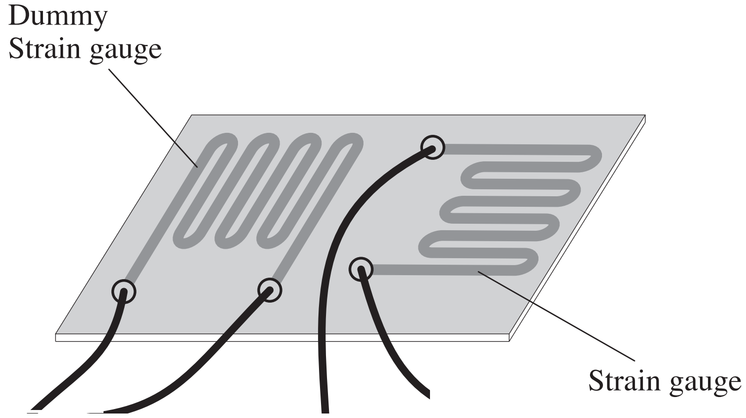
Turn over.

Examiner only
Arholwr yn unig

7. A civil engineering company wants to monitor a concrete column supporting part of a building.
The measurements of strain are stored in a microprocessor system.
Here is the block diagram for the system.



The bridge circuit uses the following strain gauge unit:



(a) (i) Draw the circuit diagram for the bridge circuit. Include a variable resistor to adjust the output to zero.
Label all components. [2]

(ii) What is the purpose of using the dummy strain gauge in this bridge circuit? [1]

....

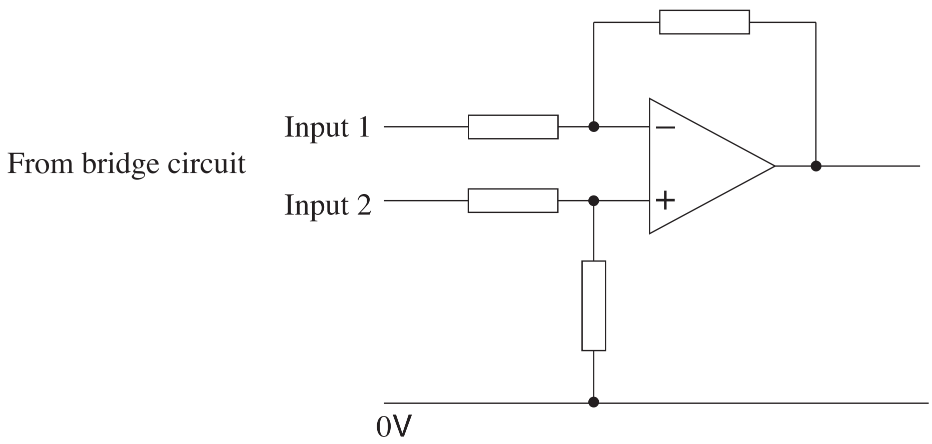
....

....

....

Examiner only
Arholwr yn unig

(b) Here is the circuit diagram for the difference amplifier. It has a voltage gain of 200.



The bridge circuit provides signals of 6·005V at Input 1, and 6·015V at Input 2. Calculate the resulting voltage at the output of the difference amplifier. [2]

....

....

....

....

(c) Measurements of strain are taken at 10 seconds intervals and are processed by the analogue to digital converter (ADC) before being stored by the microprocessor system.

(i) A successive approximation ADC is chosen for this system. One reason for this is because it is much cheaper than the equivalent flash converter. Give another reason why it is unnecessary to use a flash converter in this system. [1]

....

....

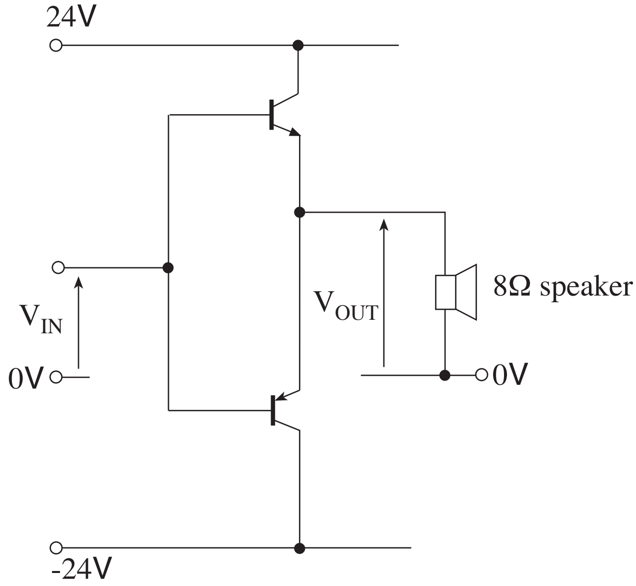
(ii) The response of the ADC is linear. It outputs a 4-bit signal and has a resolution of 0.5V.
Complete the following table to show the response of the ADC. [2]

Input/V	Output
0	0000
0·5	0001
2·2	
	0111

Turn over.

Examiner only
Arholwr yn unig

8. The power amplifier shown in the following circuit diagram is used to drive a loudspeaker.



(a) Complete the table to show the values of the output voltage V_{OUT}. [3]

Input voltage V_{IN}V	Output voltage V_{OUT}V
+2.0	
+0.5	
-0.2	
-2.5	

(b) Estimate the maximum power that can be dissipated in the 8Ω loudspeaker in this circuit. [1]

....

....

....

Examiner only
Arholwr yn unig

FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.

Examiner only
Arholwr yn unig