Candidate Name	Centre Number	Candidate Number

WELSH JOINT EDUCATION COMMITTEE
General Certificate of Education
Advanced Subsidiary/Advanced

WJEC CBAC

CYD-BWYLLGOR ADDYSG CYMRU
Tystysgrif Addysg Gyffredinol
Uwch Gyfrannol/Uwch

381/01

ELECTRONICS

ET1

P.M. TUESDAY, 23 May 2006

(1½ hours)

ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

For Examiner's use only.	
1	
2	
3	
4	
5	
6	
7	
Total	

No certificate will be awarded to a candidate detected in any unfair practice during the examination.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors
The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

RC networks

$V_C = V_O (1 - e^{-t/RC})$ for a charging capacitor

$V_C = V_O e^{-t/RC}$ for a discharging capacitor

$$t = -RC \ln\left(1 - \frac{V_c}{V_o}\right)$$ For a charging capacitor

$$t = -RC \ln\left(\frac{V_c}{V_o}\right)$$ For a discharging capacitor

Alternating Voltages $V_o = V_{rms}\sqrt{2}$

Silicon Diode $V_F \approx 0{\cdot}7V$

Bipolar Transistor

$$h_{FE} = \frac{I_C}{I_B}$$ Current gain

$V_{BE} \approx 0{\cdot}7V$ in the on state

MOSFETs $I_D = g_M V_{GS}$

Operational amplifier

$$G = -\frac{R_F}{R_{IN}}$$ Inverting amplifier

$$G = 1 + \frac{R_F}{R_1}$$ Non-inverting amplifier

$$V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$$ Summing amplifier

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$ Slew rate

555 Monostable $T = 1{\cdot}1\ RC$

555 Astable

$t_H = 0{\cdot}7\ (R_A + R_B)C$

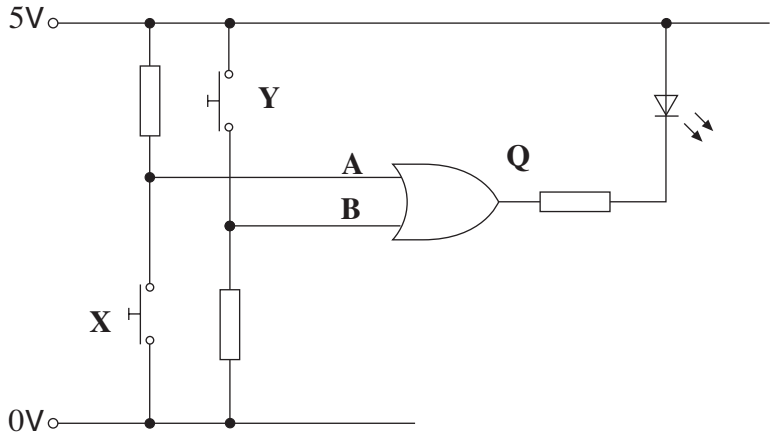
$t_L = 0{\cdot}7\ R_B C$

$$f = \frac{1{\cdot}44}{(R_A + 2R_B)C}$$

Schmitt Astable

$$f \approx \frac{1}{RC}$$

1. A circuit below contains both a pull-up and pull-down resistor.

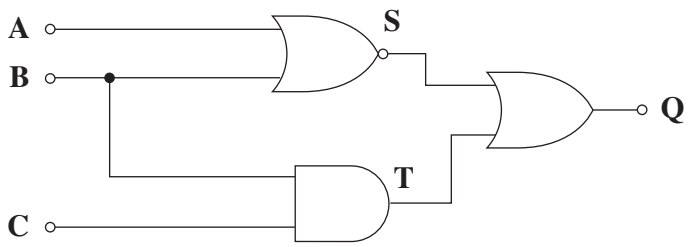


The table below shows the four possible states of the switches **X** and **Y**. Complete the table by adding:

- The correct logic levels at points **A**, **B** and **Q**
- The word **'OFF'** or **'ON'** to indicate the state of the LED **in each case**. [4]

Switch **X**	Switch **Y**	Input **A**	Input **B**	Output **Q**	State of LED
Open	Open				
Open	Closed				
Closed	Open				
Closed	Closed				

2. A logic system is shown below.



(a) Write down the Boolean expressions for **S**, **T** and **Q** in terms of the inputs **A**, **B** and **C**. [3]

S = ...

T = ...

Q = ...

(b) Complete the truth table for this system. [3]

C	B	A	S	T	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

(c) In the space below, draw the same logic system, but with the logic gates replaced by their NAND gate equivalents. [3]

(d) Draw a line through all redundant gates. [2]

3. Simplify the following expressions, showing all stages of your working.

(a) $A + \overline{A} =$ ..... [1]

(b) $\overline{A}.(\overline{B} + A) =$ .....

..... [2]

(c) $\overline{(\overline{A} + B).A}$ [3]
(hint: use DeMorgan's theorem)

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(d) Use Boolean algebra or the Karnaugh map to find the **simplest** expression for the output Q. If you use the map, show and label any groups you create in producing this expression. [3]

$$Q = C.\overline{A} + \overline{C}.\overline{B} + C.\overline{B}.A + C.B.A$$

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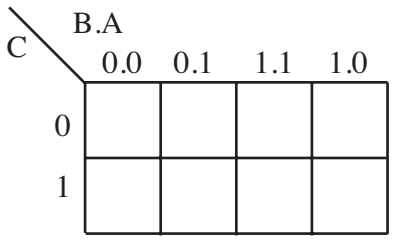
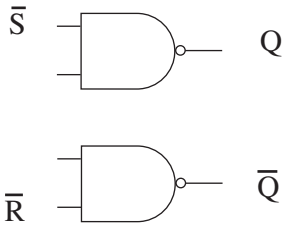
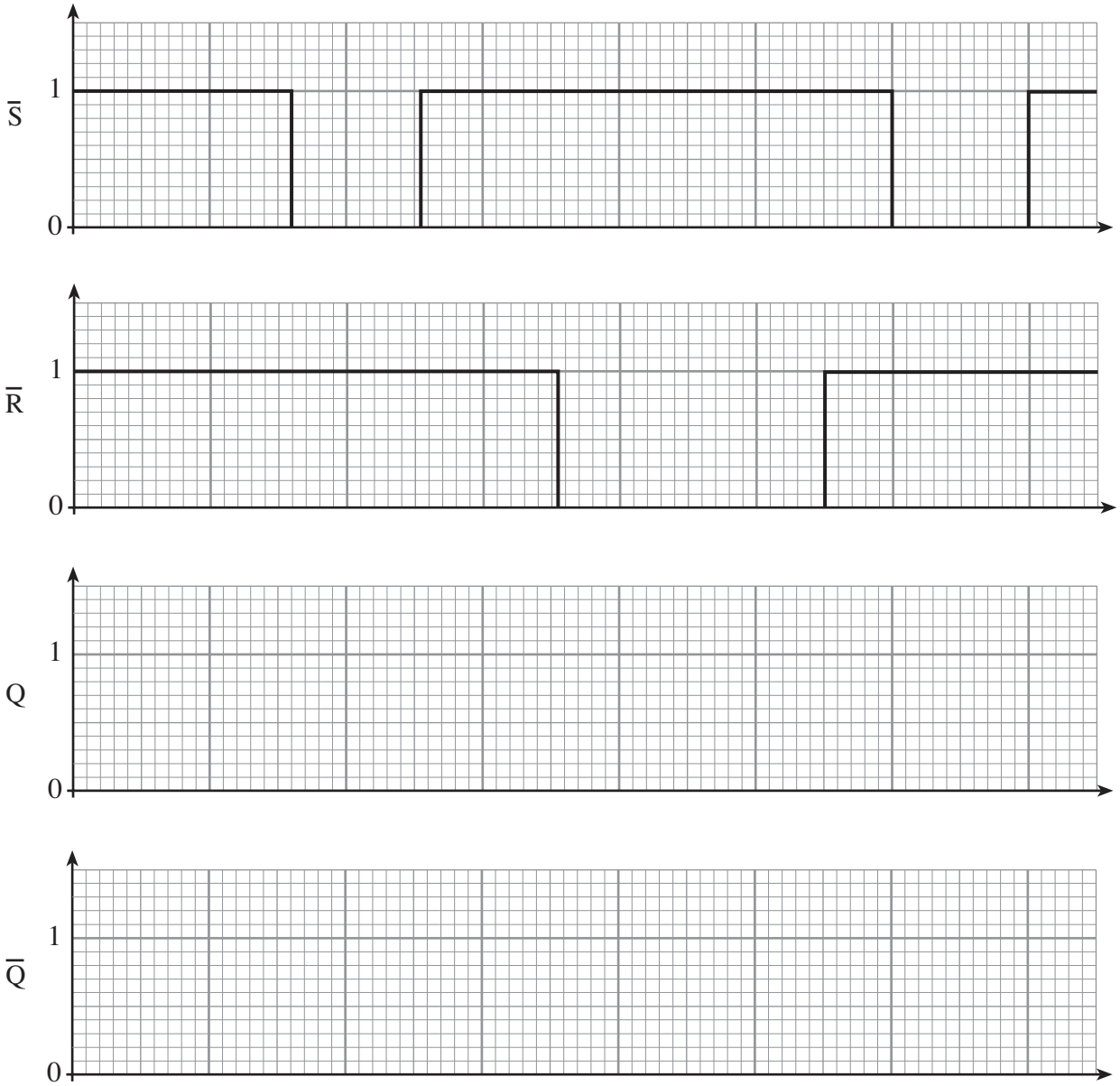


4. *(a)* Complete the diagram to show how two NAND gates can be connected to make an $\overline{S}.\overline{R}$ bistable (latch). [2]



(b) Pulses are applied to the two inputs as shown below. Draw the corresponding output pulses at Q and $\overline{Q}$ on the axes provided. **Q is initially at logic 0.** [4]



(c) Why is it desirable that $\overline{S}$ and $\overline{R}$ are prevented from being logic 0 at the same time? [1]

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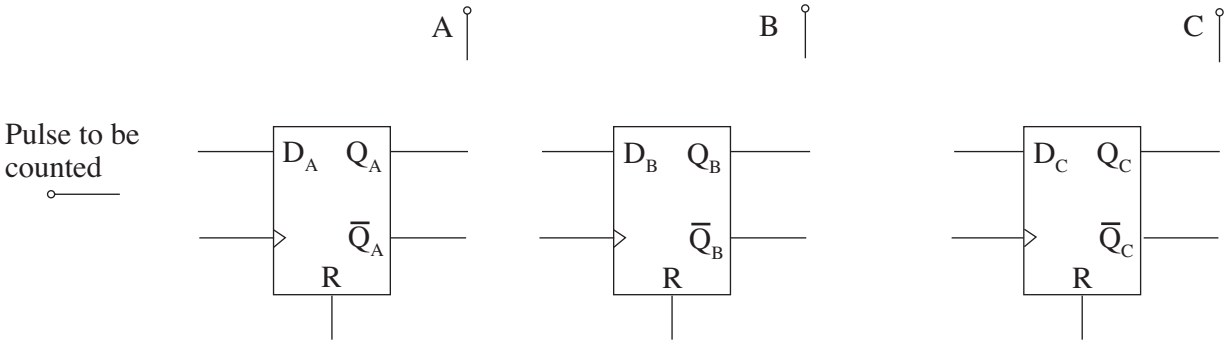
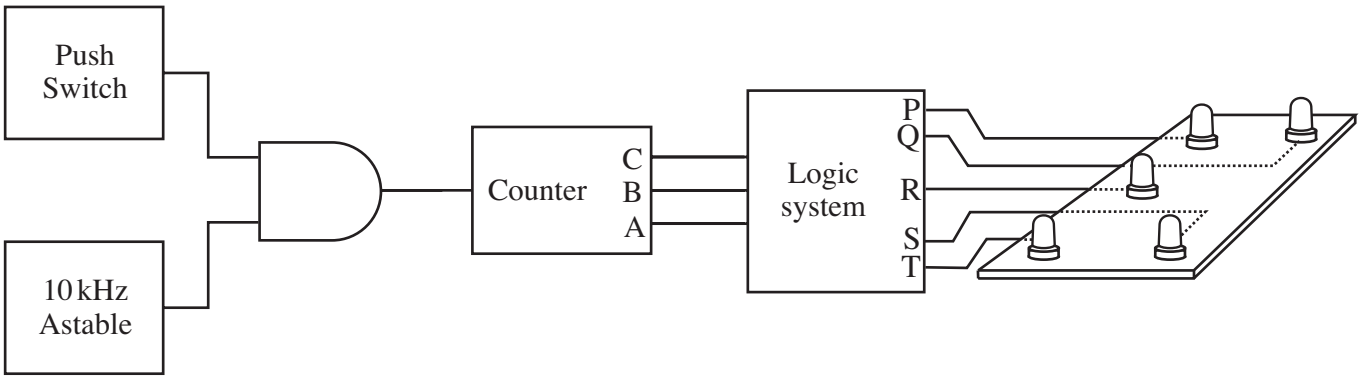
5. The diagram shows 3 D-type flip-flops, which form part of a binary up-counter. Outputs A, B and C are used to indicate the binary output. **C is the most significant bit.**

(a) (i) Complete the diagram to make a three bit binary up-counter. [3]



(ii) On the circuit diagram above add a logic gate and the connections necessary to make the counter reset on the fifth clock pulse. [3]

(b) The three bit up-counter is used as part of the simple electronic dice game shown below.



An LED is on when the corresponding output is high.

When the button is pressed and held the LED's flash in sequence. When the switch is released the sequence stops with one to five LED's on.

The sequence is specified by the following Boolean expressions.

$P = T = A + B + C$

$Q = S = C + B.A$

$R = \overline{A}$

Complete the truth table to show the sequence of outputs produced. [3]

Clock Pulse	C	B	A	P	Q	R	S	T
0	0	0	0					
1	0	0	1					
2	0	1	0					
3	0	1	1					
4	1	0	0					
5	Counter resets here							

6. *(a)* Operational amplifiers have a number of parameters. Some of these should have a very high value and some should be as small as possible. In the space after each parameter, write **either** high **or** low to indicate the desired size of **each**. [2]

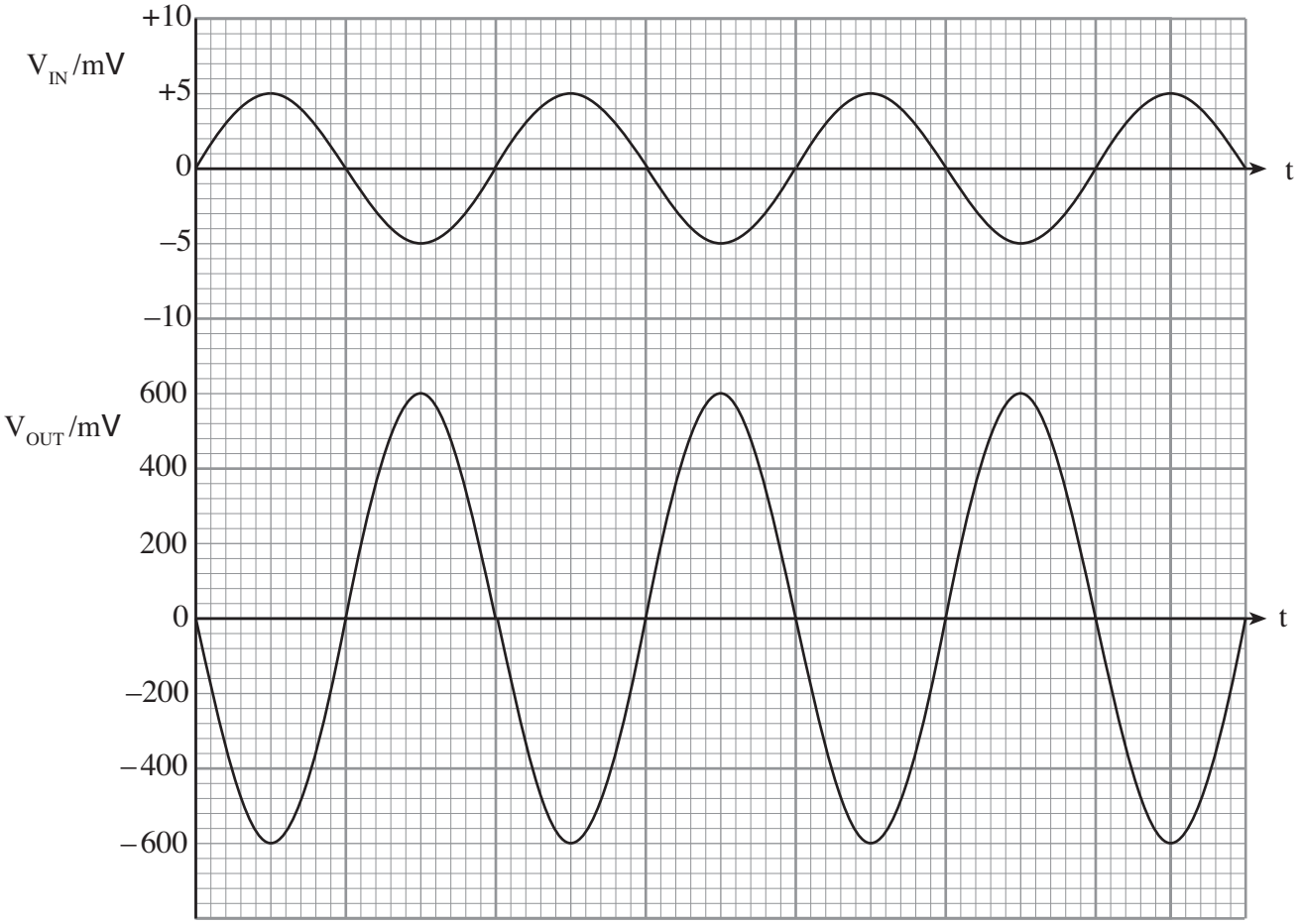
(i) Input impedance .....

(ii) Ouptut impedance .....

(iii) Slew rate .....

(iv) Open loop gain .....

(b) An amplifier has the following input and output signals.



(i) What is the voltage gain of the system? [2]

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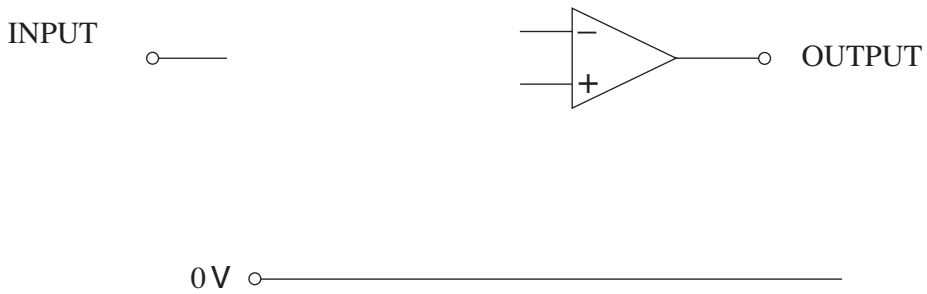
(ii) Draw the circuit diagram, based on a single op-amp, for a suitable voltage amplifier, which could be used for this system. Label any resistors used. [3]



(iii) Calculate suitable resistor values to give the voltage gain in *(b)* part (i). [2]

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(c) The ouput of the op-amp changes from –14 V to +14 V in a time of 3.5 µs.
Calculate the slew rate, giving the appropriate unit. [3]

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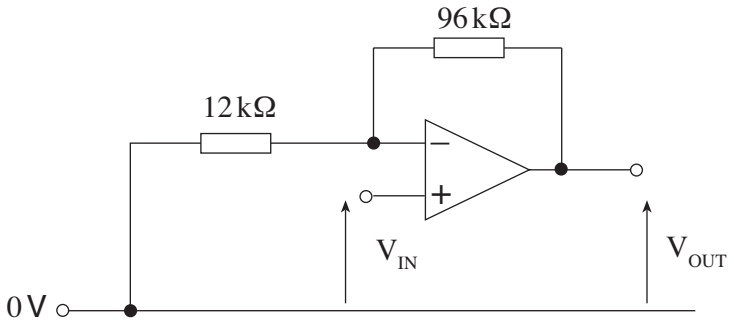
7. The following diagram shows an op-amp set up as a voltage amplifier. The op-amp is powered from a ±15 V supply and saturation occurs at ±14 V.



(a) Calculate the voltage gain of the amplifier. [1]

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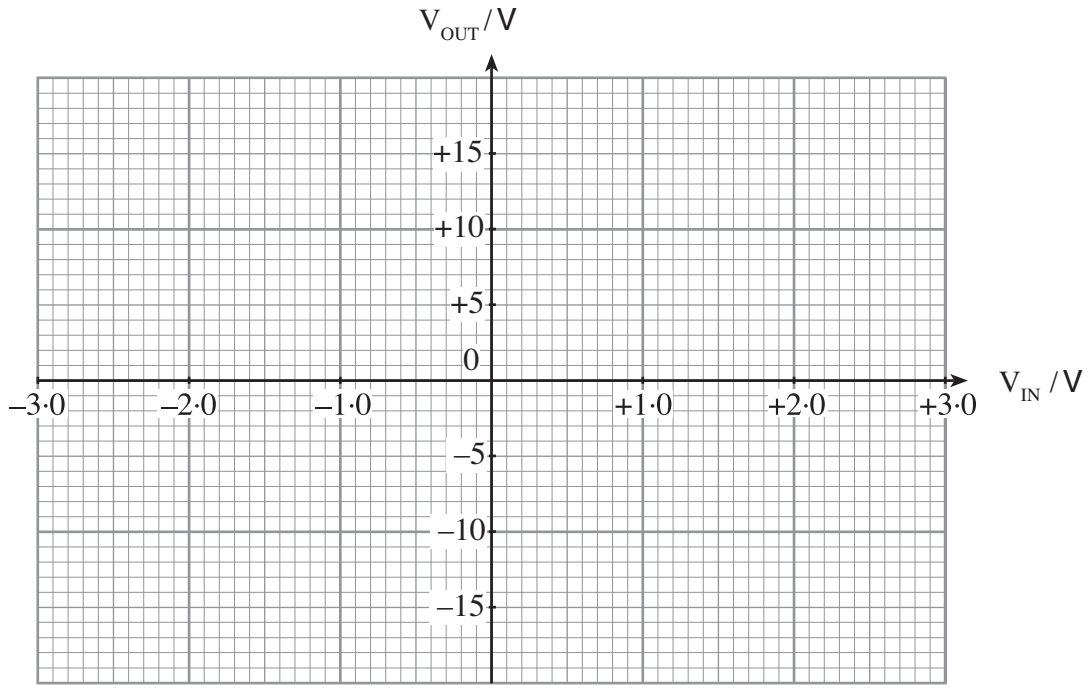
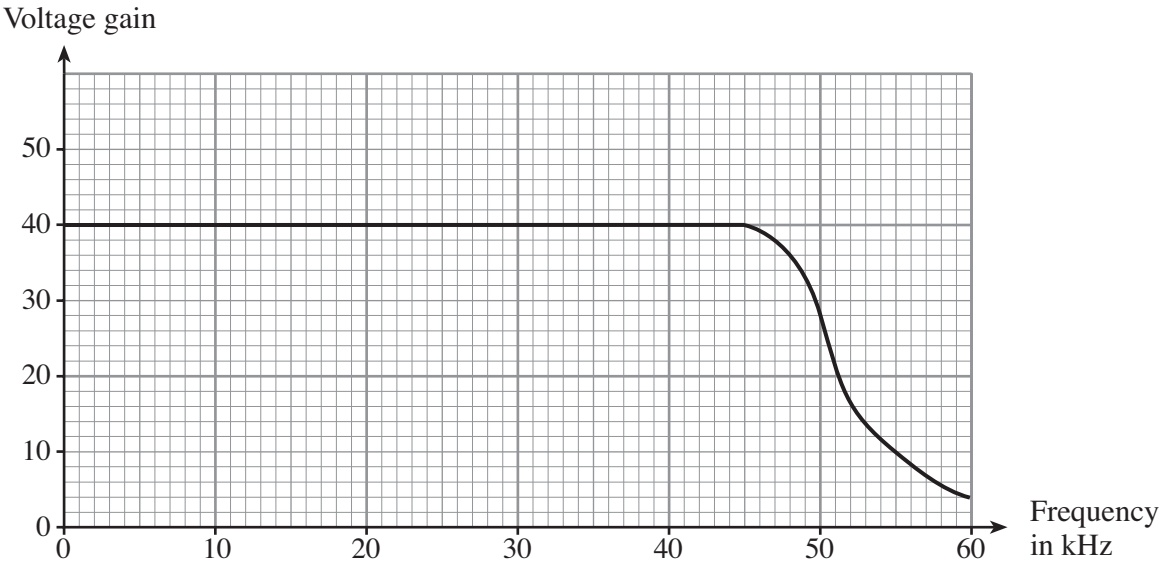
(b) Complete the graph to show how the output voltage V_{OUT} varies as the input voltage V_{IN} is increased from –3·0 V to +3·0 V. [3]



(c) The following graph shows the frequency response of a second amplifier.



Use the graph to estimate the bandwidth of the amplifier. [2]
Show **on the graph** how you obtain your answer.

Bandwidth = ...

(d) A third op-amp has a gain-bandwidth product of 4MHz. Calculate the maximum voltage gain possible if the amplifier is to provide a bandwidth of 20kHz. [2]

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FOR USE ONLY IF YOU HAVE MADE SUBSTANTIAL DELETIONS IN PARTS OF YOUR ANSWERS OR NEED MORE SPACE TO COMPLETE THEM. BE SURE TO INDICATE THE QUESTIONS CONCERNED.