# GCE MARKING SCHEME

## SUMMER 2016

## ELECTRONICS ET5
## 1145/01

## INTRODUCTION

This marking scheme was used by WJEC for the 2016 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

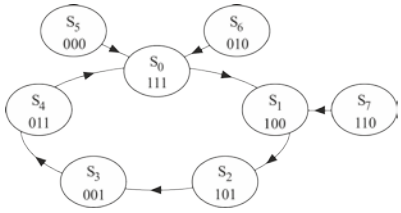
WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

**1.** *(a)*

| | Current Outputs | | | Next Outputs | | |
|---|---|---|---|---|---|---|
| **State** | **C** | **B** | **A** | **$D_C$** | **$D_B$** | **$D_A$** |
| 0 | **1** | **1** | **1** | **1** | **0** | **0** |
| 1 | **1** | **0** | **0** | **1** | **0** | **1** |
| 2 | **1** | **0** | **1** | **0** | **0** | **1** |
| 3 | **0** | **0** | **1** | **0** | **1** | **1** |
| 4 | **0** | **1** | **1** | **1** | **1** | **1** |
| 5 | 0 | 0 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 0 | 1 | 1 | 1 |
| 7 | 1 | 1 | 0 | 1 | 0 | 0 |

Five correct 'current' states identified 1 mark
Correct progression into 'Next Output' 1 mark
States in correct order in table 1 mark
('Next Outputs = 0 0 0' for state 4 = 1 mark total.)

*(b)*




Completely correct 1 mark

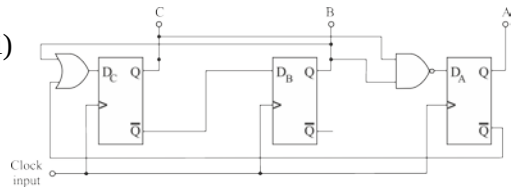
*(c)* "**An unused state is not part of the main sequence.**" or equivalent. 1 mark

*(d)* **A stuck state does not allow progression to the main sequence**, or equivalent. 1 mark

*(e)* (i) $D_B = \overline{C}$ 1 mark

$D_C = B + \overline{A}$ or $\overline{A \cdot \overline{B}}$ one mark per term 2 marks
(Must be simplest for 2 marks. Any other correct = 1 mark.)

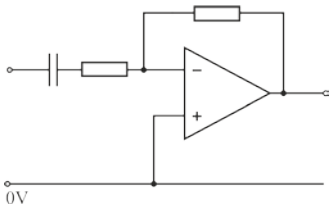
(ii)




**Allow ecf from *(e)* for $D_B$ and $D_C$**
Clock connections correct 1 mark
$D_C$ correct 1 mark
$D_B$ correct 1 mark
$D_A$ correct 1 mark
Use of $\overline{Q}$ 1 mark
(Allow ecf from *(e)* for $D_B$ and $D_C$)

**Total for Q1** **14**

**2.** *(a)*




| | | |
|---|---|---|
| Capacitor in series with resistor | | 1 mark |
| RC network in input circuit | | 1 mark |
| Remainder of circuit correct | | 1 mark |
| *(b)* (i) | Correct multipliers in break frequency formula | 1 mark |
| | Break frequency = 995 Hz (accept 994.7 Hz). | 1 mark |
| (ii) | Low frequency voltage gain = 12 (or -12) | 1 mark |
| *(c)* (i) | Filter = treble boost | 1 mark |
| (ii) | Break frequency = 3 kHz | 1 mark |
| | **Total for Q2** | **8** |

**3.** *(a)* (i) Voltage at X = 0.1 V — 1 mark

(ii) Binary output = 10 — 1 mark

(iii) Smallest $V_{IN}$ = 0.4 V (accept ">0.4 V") — 1 mark

*(b)* (i) Resolution = 0.0625 V (=1/16 V) (accept 0.063 V) — 1 mark

(ii) $V_{REF}$ = 1.0 V — 1 mark

(iii) No. of resistors = 16 — 1 mark

**Total for Q3** **6**

**4.** *(a)* Answer = D (00011) — 1 mark

*(b)* movlw b'10010XXX' (X = don't care)

Enable GIE (set bit 7) — 1 mark

Enable INTE and disable all others (set bit 4, reset bits 6, 5, 3) — 1 mark

(Answer must be 8 bits)

*(c)*

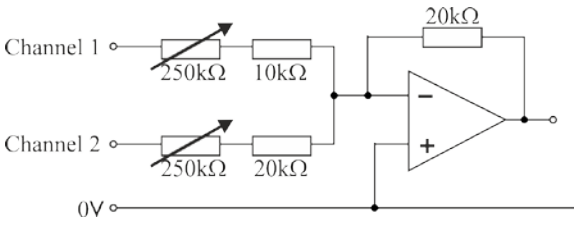
```
220  alarm  movwf   protect    ; store contents of W in register called 'protect';
221         bsf     PORTA, 2   ; output logic 1 to switch on buzzer;
222         call    tensec     ; call ten second delay subroutine;
223         btfss   PORTA,0    ; test reset switch - ignore next instruction if pressed;
224         goto    alarm      ; jump back to line 220;
```

One mark per correct line — 5 marks

( Lower case used in 'PORTA' or upper case in 'alarm' loses 1 mark)

**Total for Q4** **8**

**5.** *(a)*




Correct input impedance on both channels (>10kΩ) 1 mark
Correct max voltage gain on **both** channels 1 mark
Rest of circuit correct 1 mark
(Resistor values may differ from specimen answer.)

*(b)* Output = -[(10 x 2) + (-4 x 1)] = -16 mV
Correct value (16 mV) 1 mark
Correct sign (-) 1 mark
(Allow ecf from *(a)*)

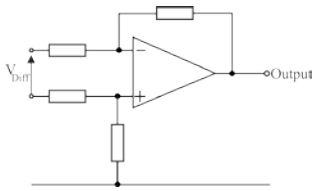
**Total for Q5** **5**

**6.** *(a)* (i) $V_{OUT}$ = 7.2 V 1 mark
(ii) New $V_{OUT}$ = **6.96 V** (accept 7.0 V) 1 mark

*(b)* (i) $V_{DIFF}$ = (6 - 7.2) = -1.2 V - allow ecf from *(a)*
Correct value 1 mark
Correct sign 1 mark
(Allow ecf from *(a)*)
(ii) $V_{DIFF}$ = (5.8 - 7.0) = -1.2 V - allow ecf from (i) 1 mark

*(c)* Advantage such as **immunity to electrical noise** 1 mark

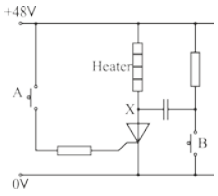
*(d)*




Inverting input at mid-point of voltage divider as shown 1 mark
Non-inverting input at mid-point of voltage divider as shown 1 mark
Correct ratio to give voltage gain of 100 1 mark

**Total for Q6** **9**

**7.** *(a)*




| | | | |
|---|---|---|---|
| (i) | Correct connection for switch, labelled A and resistor | | 1 mark |
| (ii) | Correct connection for switch, labelled B | | 1 mark |
| | Resistor in series with switch | | 1 mark |
| | Correct connection for capacitor | | 1 mark |
| *(b)* (i) | Voltage at X = 0 V | | 1 mark |
| (ii) | Voltage above switch B drops from 48 V to 0 V when switch is pressed | | 1 mark |
| | so voltage at X drops by 48 V to -48 V | | 1 mark |
| | thyristor is momentarily reverse biased and switches off, or equivalent | | 1 mark |
| *(c)* | Advantage such as no moving parts so no wear from friction | | 1 mark |
| | | **Total for Q7** | **9** |

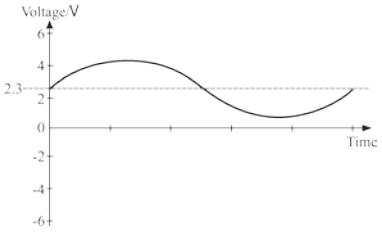
**8.** *(a)* Link **S** 1 mark
(Other links included - zero marks)

*(b)* $R_1 = R_2$ 1 mark

*(c)* (i) $V_{OUT} = 2.3\,V$

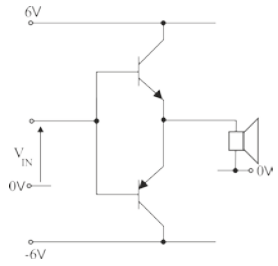
(ii) Power dissipation = 0.66 W (accept 0.7 W) 1 mark

(iii)




Signal centred on +2.3 V 1 mark
Sinusoidal signal of amplitude 2 V 1 mark

*(d)* (i)




| | | | |
|---|---|---|---|
| | Use of complementary pair | | 1 mark |
| | Common emitter connection to output | | 1 mark |
| | Common base connection to input | | 1 mark |
| (ii) | Max. power dissipation = 18 W | | 1 mark |
| (iii) | Advantage such as zero quiescent power dissipation | | 1 mark |
| | | **Total for Q8** | **11** |