GCE MARKING SCHEME

SUMMER 2016

ELECTRONICS ET1
1141/01

INTRODUCTION

This marking scheme was used by WJEC for the 2016 examination. It was finalised after detailed discussion at examiners' conferences by all the examiners involved in the assessment. The conference was held shortly after the paper was taken so that reference could be made to the full range of candidates' responses, with photocopied scripts forming the basis of discussion. The aim of the conference was to ensure that the marking scheme was interpreted and applied in the same way by all examiners.

It is hoped that this information will be of assistance to centres but it is recognised at the same time that, without the benefit of participation in the examiners' conference, teachers may have different views on certain matters of detail or interpretation.

WJEC regrets that it cannot enter into any discussion or correspondence about this marking scheme.

GCE ELECTRONICS - ET1

MARK SCHEME - SUMMER 2016

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>1.</td><td>(a)</td><td>(i)</td><td>OR gate</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>NAND gate</td><td>1</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td>EXNOR gate (XNOR)</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Correct symbol for EXNOR gate (allow ecf (b)(i))</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>4</td></tr>
<tr><td>2.</td><td>(a)</td><td></td><td>$X = \overline{(A + B)}$ or $\overline{A}.\overline{B}$
$Y = \overline{B}.C$
$Q = \overline{(A + B)} + \overline{B}.C$ or $\overline{A}.\overline{B} + \overline{B}.C$ or $\overline{B}.(\overline{A} + C)$</td><td>1
1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>
<table>
<tr><th>C</th><th>B</th><th>A</th><th>X</th><th>Y</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
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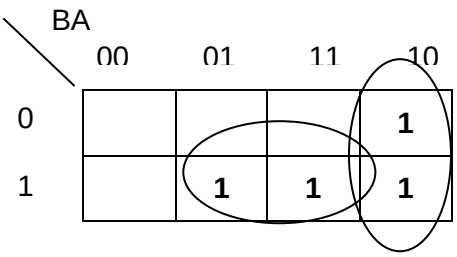
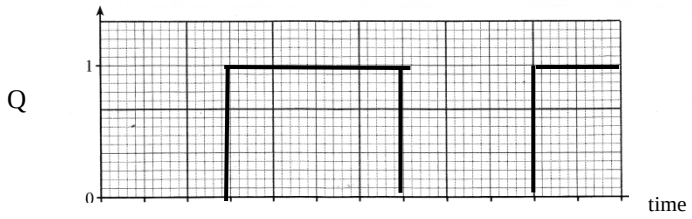
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
One mark each correct column X, Y and Q
(Q ecf on X and Y)</td><td>3</td></tr>
<tr><td></td><td>(c)</td><td>(i)</td><td>Accept correct NAND gate solutions for any of the answers to Q
e.g. First answer:
Correct replacement of NOR with NAND
Correct replacement of both NOT and AND with NAND
Correct replacement of OR with NAND
(allow extra NOT gate on B solution)
2nd answer: Invertors / 2 AND / OR
3rd answer: Invertors / AND / OR</td><td>

1
1
1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>Minimum number of gates to match solution shown with appropriate explanation. 1st and 3rd = 5; 2nd =6
{no ecf mark if extra NOT gate on B used in (i)}</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>10</td></tr>
</table>

Question			Marking detail	Marks available
3.	(a)		 $Q = C.A + B.\overline{A}$ Correct transfer of data to Karnaugh map Each term correct (ecf from map drawn; max. 2 marks)	 1 2
	(b)		D_0, D_1, D_3 and D_4 to 0V D_2, D_5, D_6 and D_7 to 5V Completely correct 1 mark (allow **ecf** from (a))	1
				4
4.	(a)	(i)	(logic) **1**	1
		(ii)	$\overline{A} + B$ alternative $\overline{\overline{B}.A}$	1
		(iii)	$Q = \overline{D}.C$ {interim step ($\overline{D}.C + \overline{D}.D$)}	1
	(b)		$= \overline{\overline{\overline{A} + B}.\overline{A}}$ (line 1) $= (\overline{A} + B).\overline{A}$ (line 2) $= \overline{A}.\overline{A} + B.\overline{A}$ $= \overline{A}.(1+B)$ $= \overline{A}$ Correct application of DeMorgan's theorem (line 1) Correct simplifications (2 marks) Alternative solution for lines 1 and 2 $= \overline{A.\overline{B} + A}$ $= \overline{A.\overline{B}}.\overline{A}$ $= (\overline{A} + B).\overline{A}$	1 2
				6

Question			Marking detail	Marks available
5.	(a)		$\overline{S}$ and $\overline{R}$ correctly connected to NAND gate inputs Correct cross connection of NAND gate outputs and inputs	1 1
	(b)		<table><tr><th>A</th><th>B</th><th>$\overline{S}$</th><th>$\overline{R}$</th><th>Q</th></tr><tr><td>OPEN</td><td>OPEN</td><td>1</td><td>1</td><td>0</td></tr><tr><td>CLOSED</td><td>OPEN</td><td>0</td><td>1</td><td>1</td></tr><tr><td>OPEN</td><td>OPEN</td><td>1</td><td>1</td><td>1</td></tr><tr><td>OPEN</td><td>CLOSED</td><td>1</td><td>0</td><td>0</td></tr><tr><td>OPEN</td><td>OPEN</td><td>1</td><td>1</td><td>0</td></tr></table> $\overline{S}$ and $\overline{R}$ columns BOTH correct Q correct (accept HIGH/LOW)	 1 1
	(c)		Timing diagram completely correct  	1
	(d)		Q is indeterminate / Q and $\overline{Q}$ both logic 1 (high together)	1
				6
6.	(a)		B starts at logic 0 B goes from 0 to 1 at 30 n s Q has 15 Pulse Pulse lies between 20 and 35 s	1 1 1 1
	(b)		To provide edge-triggering/ Transition gate (Produces a **very short** pulse) (Not monostable or time delay or used in a D-type)	1
				5

<table>
<tr><th colspan="3">Question</th><th>Marking detail</th><th>Marks available</th></tr>
<tr><td>7.</td><td>(a)</td><td></td><td>Switch and resistor across power rails and connected to R
Correct orientation of components</td><td>1
1</td></tr>
<tr><td></td><td>(b)</td><td></td><td>When the D-type is reset the output $\overline{Q}$ will be at logic 1 and the LED will be off (both correct for mark)</td><td>1</td></tr>
<tr><td></td><td>(c)</td><td></td><td>Q goes from 0 to 1 on 1st and 3rd clock pulse
Q goes from 1 to 0 on rising edge of RESET only
$\overline{Q}$ is inverse of Q</td><td>1
1
1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>6</td></tr>
<tr><td>8.</td><td>(a)</td><td>(i)</td><td>R_F = 40 kΩ</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>V_{IN} = 1.67 V allow $\frac{15}{9}$</td><td>1</td></tr>
<tr><td></td><td>(b)</td><td>(i)</td><td><table><tr><th>V_{IN} / V</th><th>V_{OUT} / V</th></tr><tr><td>–3</td><td>-15</td></tr><tr><td>–2</td><td>-15</td></tr><tr><td>–1</td><td>-9</td></tr><tr><td>1</td><td>9</td></tr><tr><td>2</td><td>15</td></tr><tr><td>3</td><td>15</td></tr></table>V_{OUT} column correct</td><td>1</td></tr>
<tr><td></td><td></td><td>(ii)</td><td>▪ Positive gradient slope through the origin
▪ Correct plotting of points
{check line passes through (1.0, 9.0) }
▪ Saturation at 15 V (penalise curve)</td><td>1
1
1</td></tr>
<tr><td></td><td>(c)</td><td></td><td>(i) LOWER {V_{IN} (SAT)}
Accept value 1.36 V</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td>(ii) No change</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td>8</td></tr>
</table>

Question			Marking detail	Marks available
9.	(a)	(i)	$12\,k\Omega$	1
		(ii)	voltage gain -15	1
		(iii)	V_{OUT} = -13.5 V {**ecf** gain in a (ii)} (both minus signs = 1 mark)	1 1
		(iv)	$\frac{3x10^6}{15}$ {**ecf** gain in a (ii)} 200 k[Hz] 0.2 M[Hz] 200 000	1 1
	(b)	(i)	6 kΩ	1
		(ii)	-14 V saturated (sign is neutral)	1
	(c)		bw is **Reduced** (owtte) / Halved / value 100 kHz If value given allow **ecf** (a)(iv)	1
	(d)		$\Delta t = \frac{28}{5}$ = 5.6 (1 mark) μs (1 mark) (unit consistent with number)	2
				11