Surname	Centre Number	Candidate Number
Other Names		2

GCE AS/A level

1141/01

S16-1141-01

ELECTRONICS – ET1

P.M. TUESDAY, 17 May 2016

1 hour 15 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	**4**	
2.	**10**	
3.	**4**	
4.	**6**	
5.	**6**	
6.	**5**	
7.	**6**	
8.	**8**	
9.	**11**	
Total	**60**	

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ADDITIONAL MATERIALS

In addition to this examination paper, you will need a calculator.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.

Write your name, centre number and candidate number in the spaces at the top of this page.

Answer **all** questions.

Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The total number of marks available for this paper is 60.

The number of marks is given in brackets at the end of each question or part-question.

You are reminded of the necessity for good English and orderly presentation in your answers.

You are reminded to show all working. Credit is given for correct working even when the final answer given is incorrect.

INFORMATION FOR THE USE OF CANDIDATES

Preferred Values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard Multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Operational amplifier $G = -\frac{R_F}{R_{IN}}$

$$G = 1 + \frac{R_F}{R_1}$$

$$\text{Slew Rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

Boolean identities $A + \overline{A}.B = A + B$

$$A.B + A = A.(B + 1) = A$$

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Answer **all** *questions.*

1. *(a)* Which type of 2-input logic gate outputs a logic 1:

(i) when either input is at logic 1? ..... [1]

(ii) when either input is at logic 0? ..... [1]

(b) The truth table for a logic gate is shown below.

B	A	Q
0	0	1
0	1	0
1	0	0
1	1	1

(i) What logic gate produces this truth table? [1]

.....

(ii) Draw the circuit symbol for this logic gate. [1]

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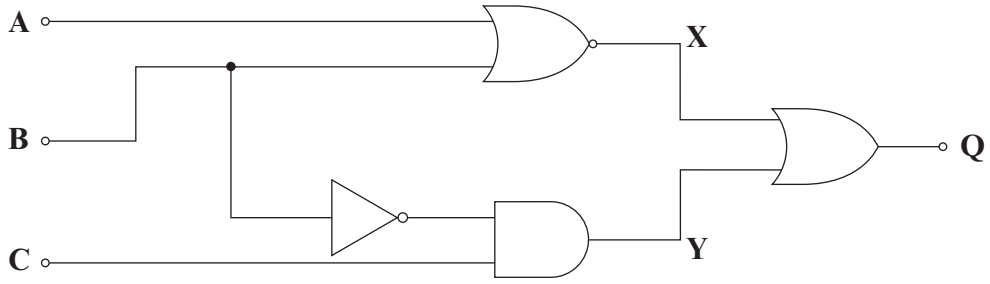
2. A system of logic gates is shown below.



(a) Give the Boolean expression for each of the outputs **X**, **Y** and **Q** in terms of the inputs **A**, **B** and **C**. [3]

X = ...

Y = ...

Q = ...

(b) Complete the truth table for this system. [3]

C	B	A	X	Y	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

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(c) (i) Redraw this logic system using NAND gates only. [3]

(ii) Deduce the **minimum** number of NAND gates needed to construct the equivalent circuit **and** explain how this number was achieved. [1]

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Turn over.

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3. The truth table for a logic system is given below.

C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(a) Transfer this information to a Karnaugh map and obtain the simplest Boolean expression for the output **Q**. [3]

.....

.....

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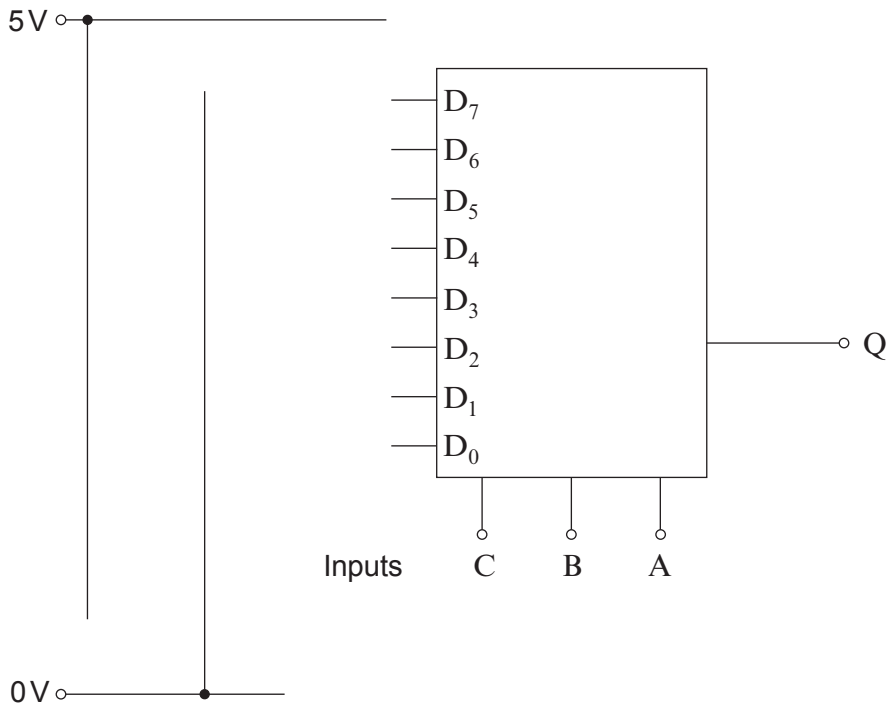
.....

Q = ...

C \ BA	00	01	11	10
0				
1				

(b) Show how the output **Q** could be generated using a multiplexer. [1]



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4. *(a)* Simplify the following expressions.

(i) $\overline{D} + 1$ ..... [1]

(ii) $\overline{B}.\overline{A} + B$ ..... [1]

(iii) $\overline{D}\ (C + D)$ ..... [1]

(b) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{(\overline{A} + B)} + A}$$

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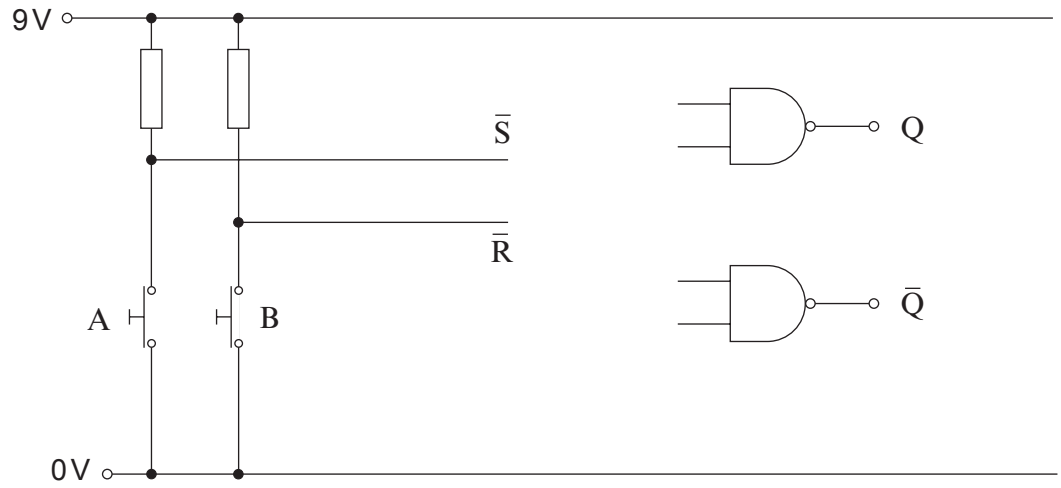
5. *(a)* Complete the diagram to show how two NAND gates can be connected to make a bistable latch and how the two switches A and B can be used to set and reset the system. [2]



(b) Complete the table with the correct logic levels.
Output Q is initially low. [2]

Switch position		Logic levels		
A	**B**	$\overline{\mathbf{S}}$	$\overline{\mathbf{R}}$	**Q**
OPEN	OPEN			
CLOSED	OPEN			
OPEN	OPEN			
OPEN	CLOSED			
OPEN	OPEN			

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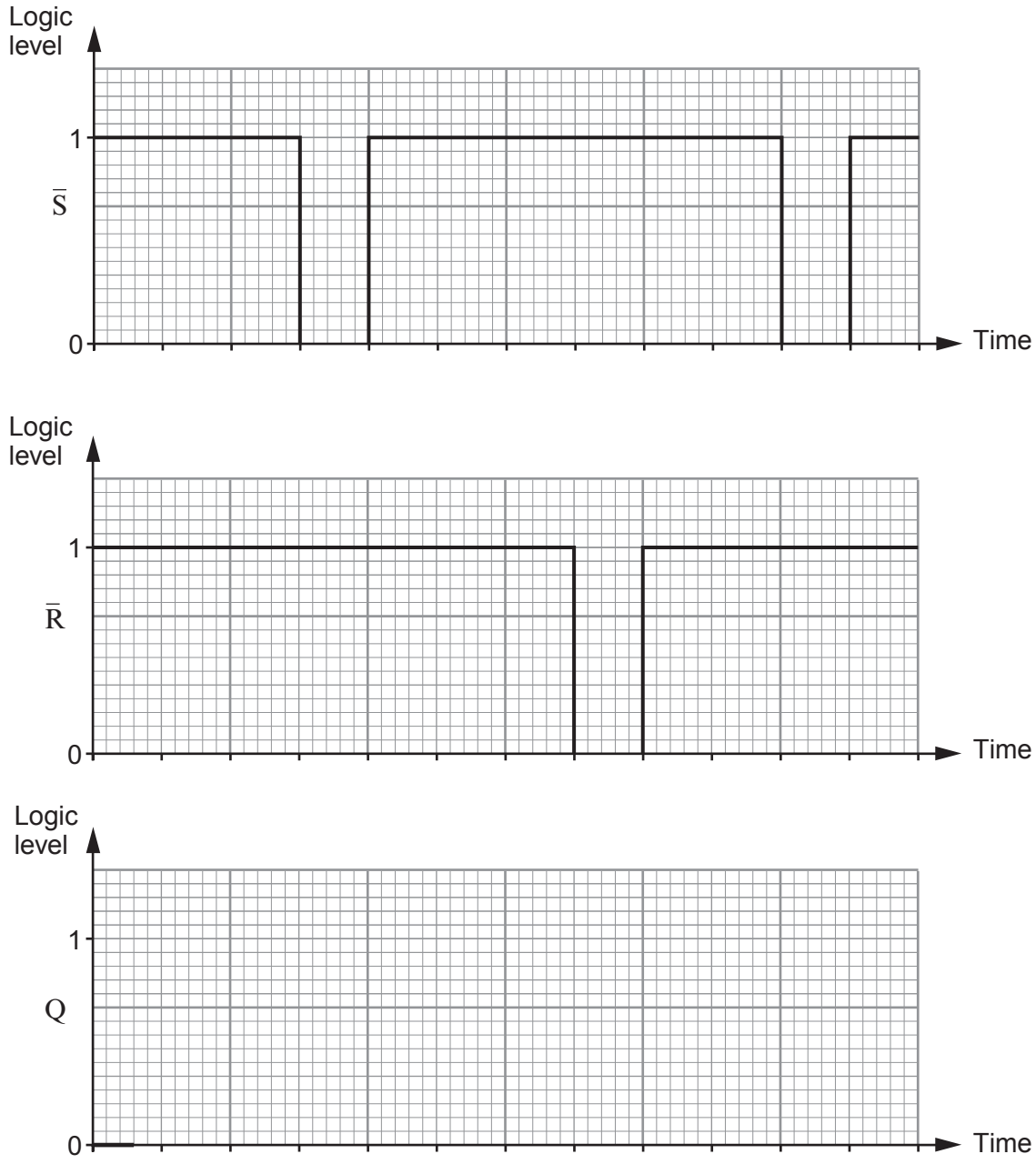
(c) The input logic states of the bistable is shown below. Draw the output signal Q on the axes provided. [1]



(d) Why is it desirable that $\overline{S}$ and $\overline{R}$ are prevented from being logic 0 at the same time? [1]

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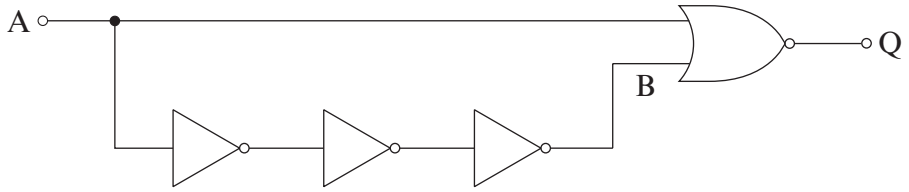
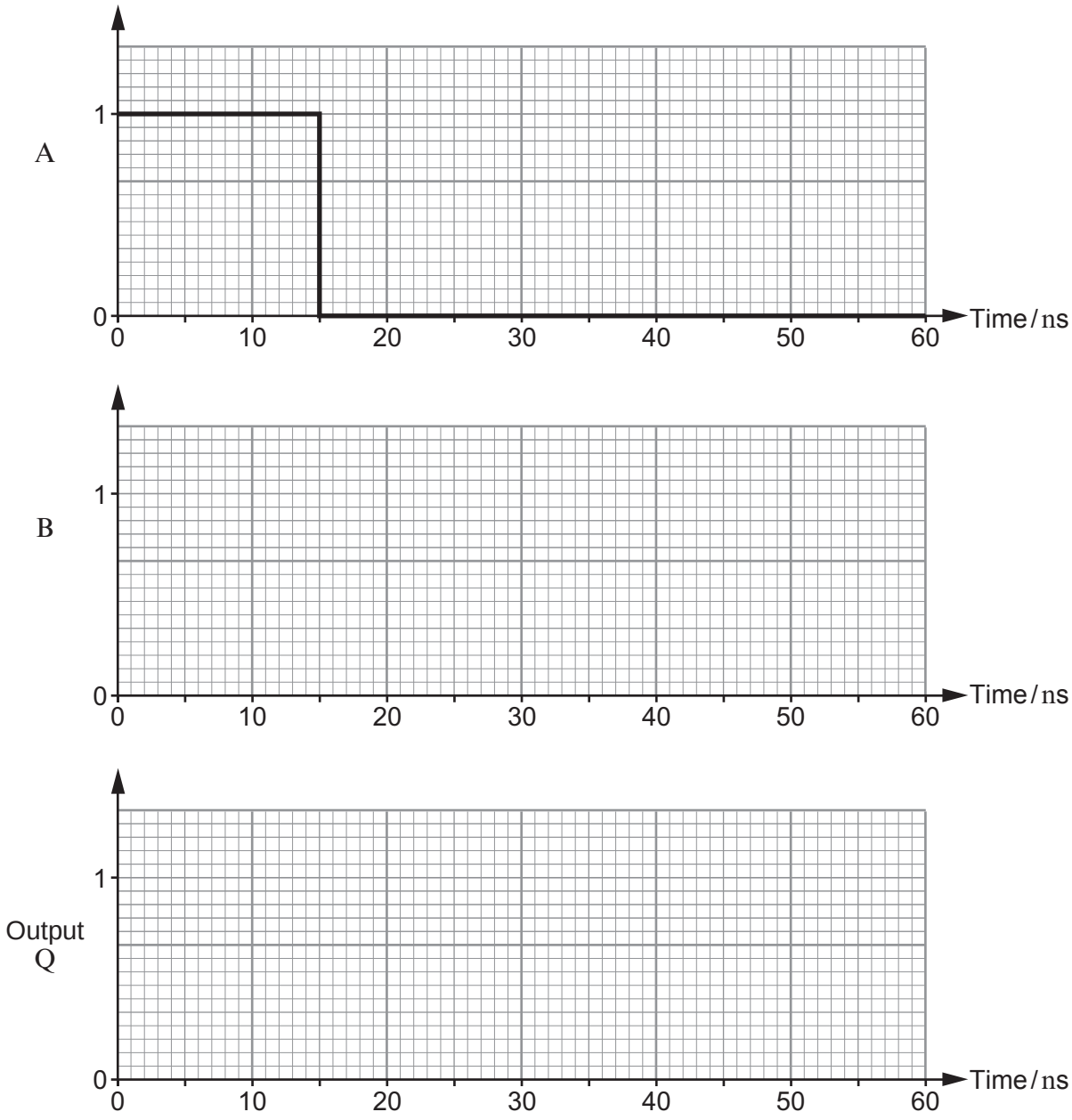
6. Consider the following arrangement of logic gates.



Each gate has a propagation delay of 5 ns.

(a) Complete the following diagram to show how the signal at B and the output Q change when the pulse shown is applied to input A. **Initially, output Q is at logic 0** and input A has been high for a long time. [4]



(b) Give an application for this arrangement of logic gates. [1]

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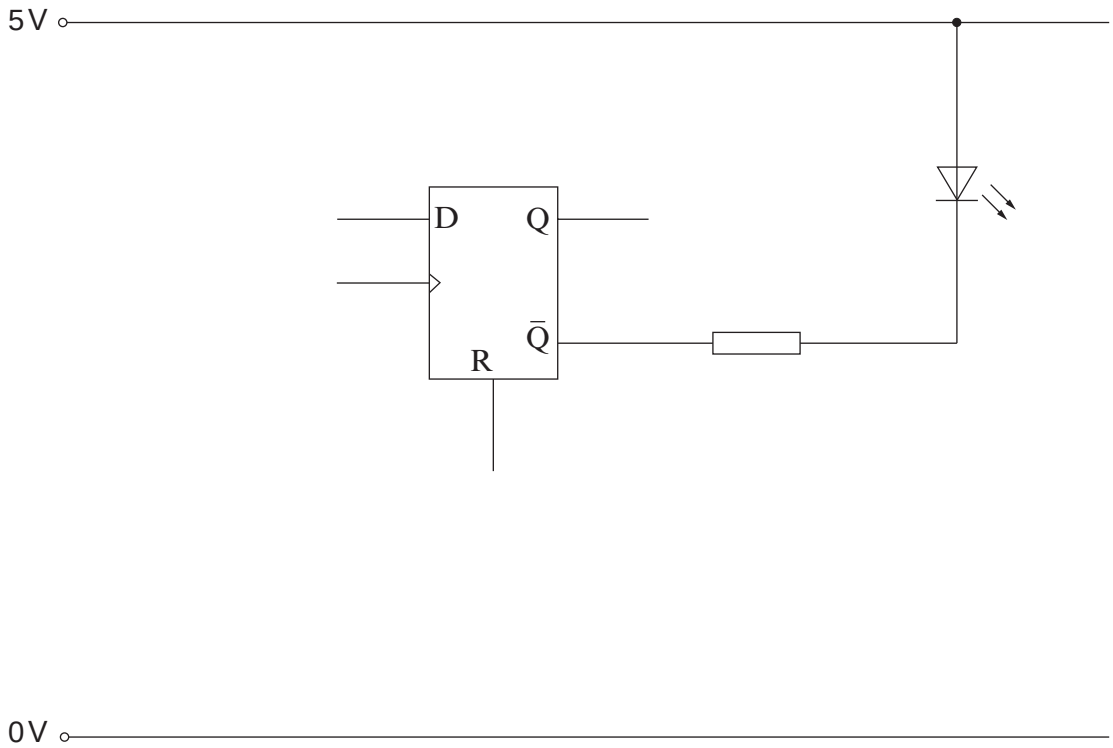
7. The diagram shows a *rising-edge triggered* D-type flip-flop. R is *active high*.



(a) Add the necessary components to the diagram such that the D-type can be **reset** with the momentary press of a switch. [2]

(b) Complete the following sentence.

When the D-type is reset the output $\overline{Q}$ will be at logic ..... and the LED will be ..... . [1]

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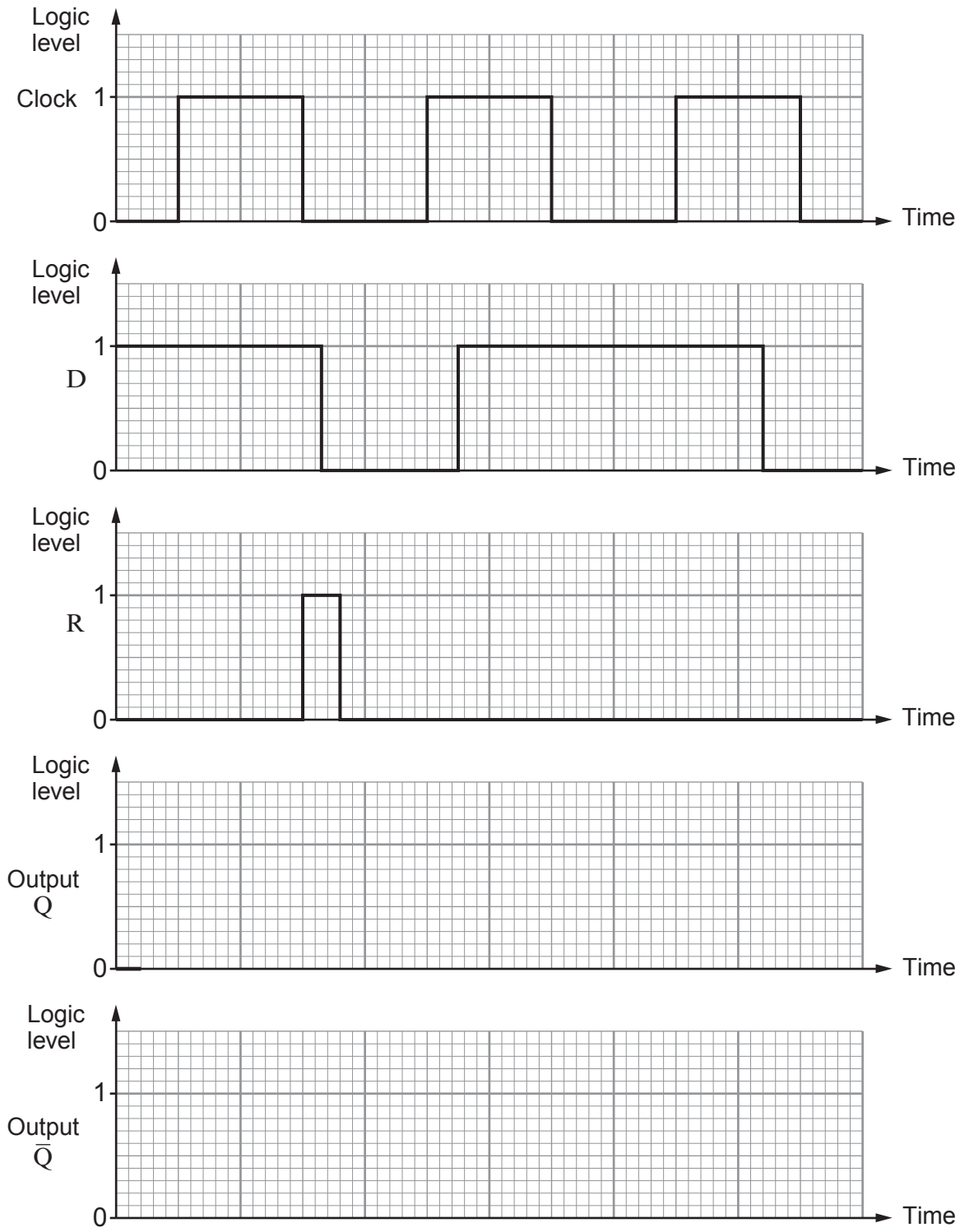
(c) The signals shown in the timing diagrams below are applied to the circuit. Complete the timing diagram for the outputs Q and $\overline{Q}$. [3]



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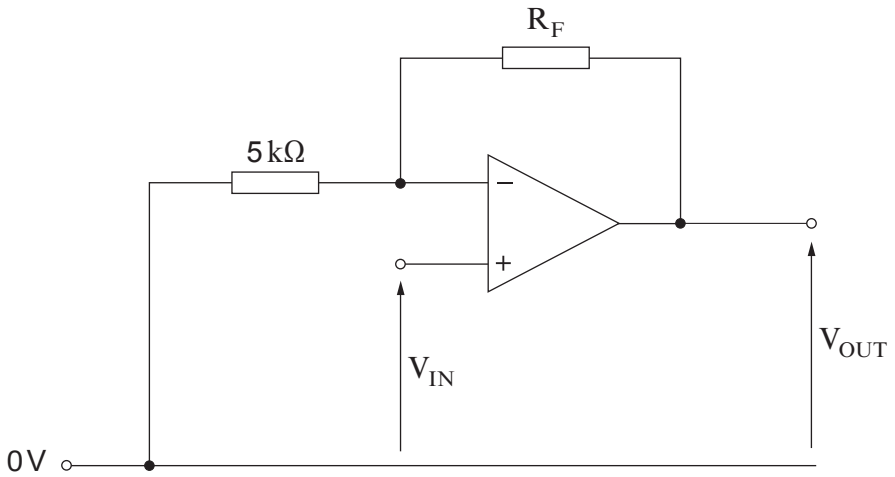
8. The following diagram shows an op-amp set up as a voltage amplifier. The op-amp is powered from a ± 16 V supply. It saturates at ± 15 V.



(a) (i) Calculate the value for resistor R_F such that the voltage gain of the amplifier is 9. [1]

.....

.....

(ii) Determine the input voltage at which the amplifier just saturates. [1]

.....

.....

(b) A student varies the values of the input voltage V_{IN} from –3 V to +3 V.

V_{IN}/V	V_{OUT}/V
–3	
–2	
–1	
+1	
+2	
+3	

(i) Use the information in part (a) to complete the V_{OUT} column of the table. [1]

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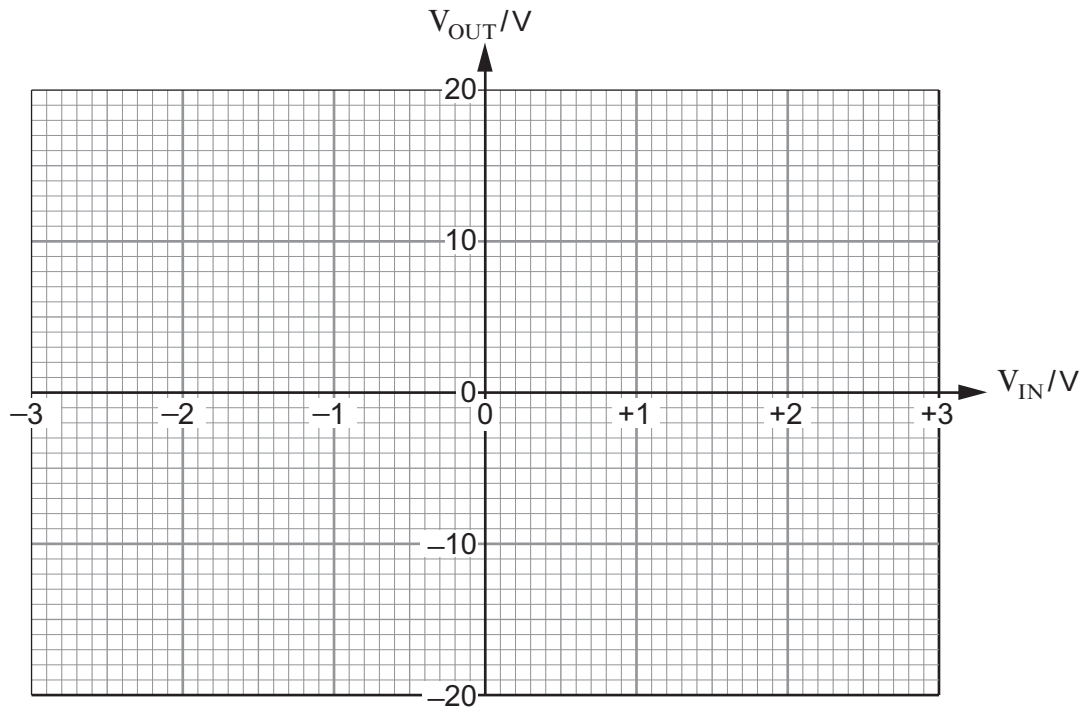
(ii) Draw the graph of V_{OUT} (y-axis) against V_{IN} (x-axis). [3]



(c) The student replaced the 5 kΩ resistor by a 4 kΩ resistor.
What effect does this have on:

(i) the input voltage at which the amplifier just saturates? [1]

.....

.....

(ii) the gain-bandwidth product of the amplifier? [1]

.....

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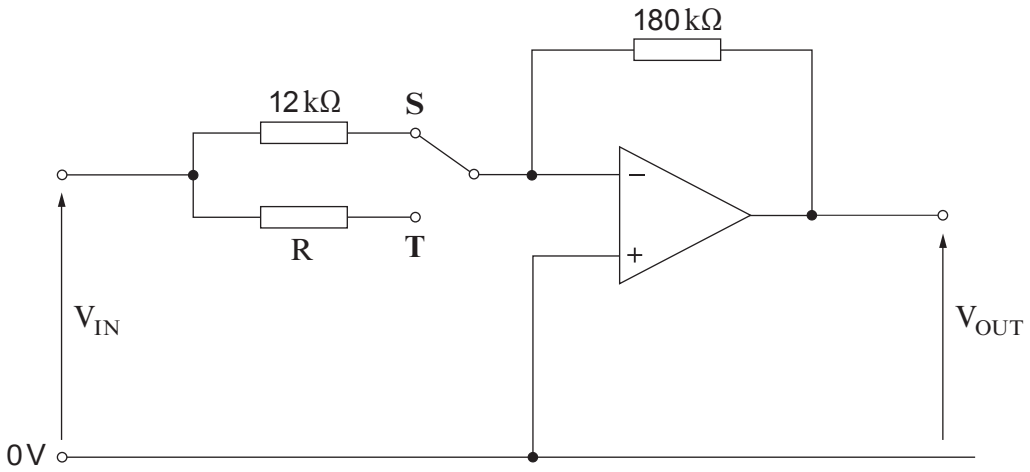
9. An extract from the data sheet of an op-amp is shown in the following table.

Parameter	Value
Input impedance	10 MΩ
Output impedance	100 Ω
Open loop gain	10^5
Gain bandwidth product	3 MHz
Slew rate	5 V μs^{-1}

The circuit diagram below shows an op-amp set up as a voltage amplifier. The switch allows the user to change the gain of the amplifier.



The op-amp is powered from a ± 15 V supply and saturation occurs at ± 14 V.
An input voltage of 0.9 V is applied to V_{IN}.

(a) The switch is initially connected to position S.

(i) Determine the input impedance of the amplifier. [1]

.....

(ii) Calculate the voltage gain of the amplifier. [1]

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(iii) Calculate the output voltage when V_{IN} = 0.9 V. [2]

.....

(iv) Calculate the bandwidth of the amplifier. [2]

.....

.....

(b) The switch is moved to position **T**. This doubles the gain of the amplifier. Calculate:

(i) the value of resistor R; [1]

.....

.....

(ii) the output voltage for V_{IN} = 0.9 V. [1]

.....

.....

(c) State what change, **if any**, has occurred to the bandwidth after the switch is moved from position **S** to **T**. [1]

.....

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(d) In response to a large step input, the output of the op-amp changes from – 14 V to + 14 V. Calculate the time taken for this change in output voltage to occur. [2]

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