OCR
RECOGNISING ACHIEVEMENT

Wednesday 12 June 2013 – Morning

A2 GCE ELECTRONICS

F615 Communication Systems

Candidates answer on the Question Paper.

OCR supplied materials:
None

Other materials required:
- Scientific calculator

Duration: 1 hour 40 minutes

Candidate forename		Candidate surname	

Centre number						Candidate number				

INSTRUCTIONS TO CANDIDATES

- Write your name, centre number and candidate number in the boxes above. Please write clearly and in capital letters.
- Use black ink. HB pencil may be used for graphs and diagrams only.
- Answer **all** the questions.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).
- Do **not** write in the bar codes.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **110**.
- You will be awarded marks for your Quality of Written Communication.
- You are advised to show all the steps in any calculations.
- This document consists of **20** pages. Any blank pages are indicated.

A calculator may be used for this paper

Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15 V and –15 V
- logic circuits are run off supply rails at +5 V and 0 V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7\,RC$
relaxation oscillator period	$T = 0.5\,RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$

Data Sheet

Boolean Algebra	$A.\overline{A} = 0$
	$A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$
	$\overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$
	$A.B + \overline{A}.C = A.B + \overline{A}.C + B.C$
amplifier gain	$G = -g_{\mathrm{m}}R_{\mathrm{d}}$
ramp generator	$\Delta V_{\mathrm{out}} = -V_{in}\dfrac{\Delta t}{RC}$
inductor reactance	$X_L = 2\pi fL$
capacitor reactance	$X_C = \dfrac{1}{2\pi fC}$
resonant frequency	$f_0 = \dfrac{1}{2\pi\sqrt{LC}}$

Answer **all** questions.

1 A student uses three cables to connect their computer to a monochrome monitor, as shown in Fig. 1.1.

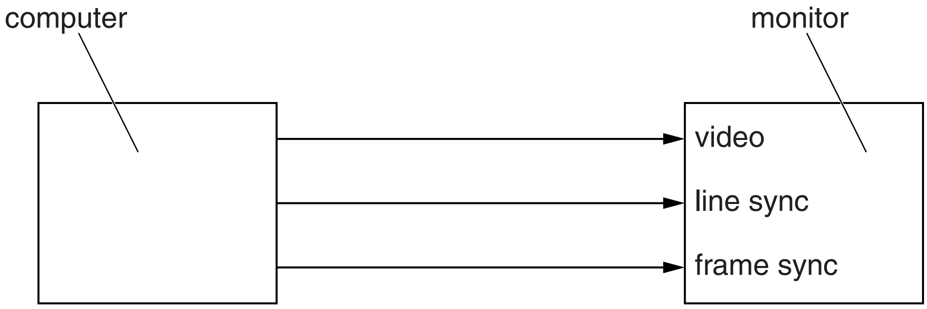

Fig. 1.1

(a) The analogue video signal is generated in the computer by a digital-to-analogue converter with the following specification:

- range 0 V to 1.27 V
- resolution 0.01 V

Explain why the input to the converter is a 7-bit word.

....

....

.... **[2]**

(b) The monitor has the following specification:

- 1 024 000 pixels per frame
- 60 Hz refresh rate

(i) The student decides to use a video cable with a bandwidth of 5 MHz.
Use calculations to explain why this bandwidth is too low.

[2]

(ii) Explain the effect this cable would have on the picture displayed by the monitor.

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.... **[2]**

(iii) The student decides to alter the refresh rate to solve this problem.
Explain why it would be better to use a cable with a higher bandwidth instead.

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.... **[3]**

(iv) The frequency of pulses along the frame sync cable is 60 Hz.
Calculate the frequency of the pulses along the line sync cable.
Each frame has 1 024 000 pixels in 1280 columns.

frequency = ... kHz **[2]**

[Total: 11]

2 Fig. 2.1 is an amplitude-frequency graph for a carrier wave which is amplitude modulated by an audio frequency signal.

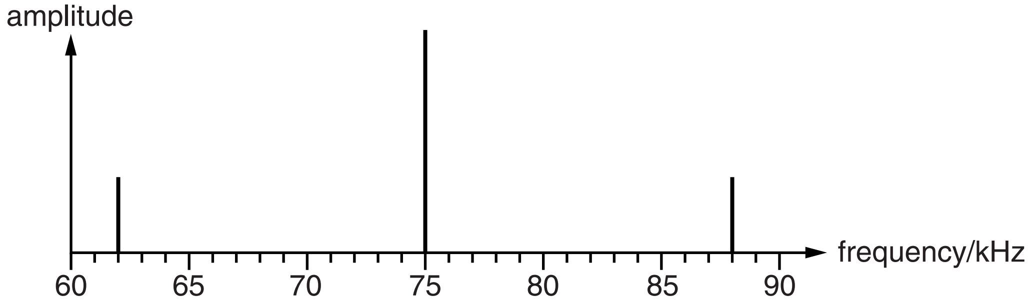

Fig. 2.1

(a) State the frequency of:

(i) the carrier wave

carrier frequency = ... kHz **[1]**

(ii) the audio frequency signal

audio frequency signal = ... kHz **[1]**

(b) Sketch a voltage-time graph for the amplitude modulated carrier on the axes of Fig. 2.2.

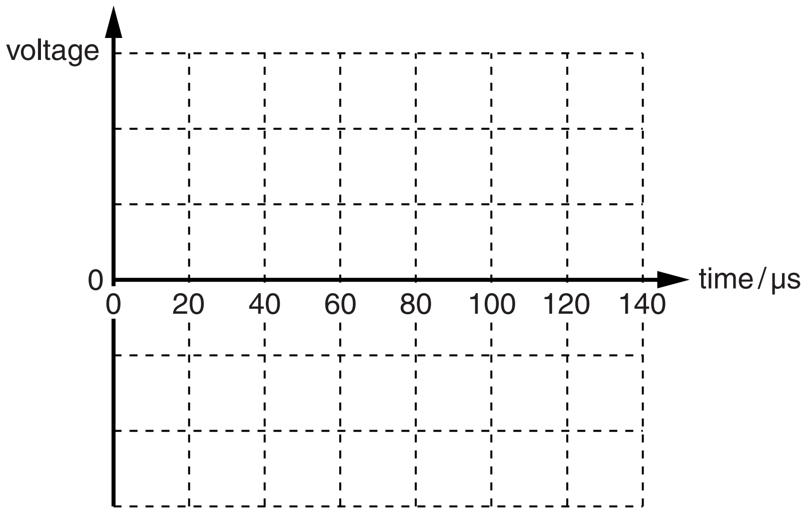

Fig. 2.2

[3]

(c) Fig. 2.3 is a circuit which can be used to amplitude modulate a carrier with an audio frequency (a.f.) signal.

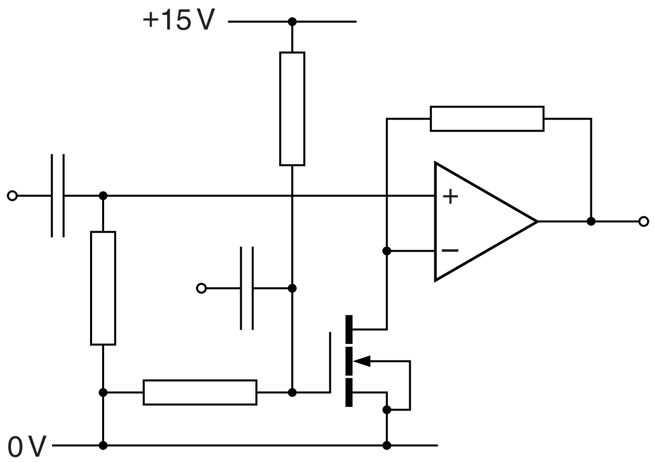

Fig. 2.3

(i) On Fig. 2.3, label the input for the carrier **C** and the input for the modulating a.f. signal **A**. **[1]**

(ii) Explain how the circuit is able to perform the operation of amplitude modulation.

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.... **[4]**

(iii) A relaxation oscillator is used to provide a square wave carrier signal for the modulator circuit. Draw a suitable circuit for the oscillator in the space below.
Show all component values and justify them.

[4]

[Total: 14]

3 Fig. 3.1 is a block diagram for a system which produces a frequency modulated carrier wave.

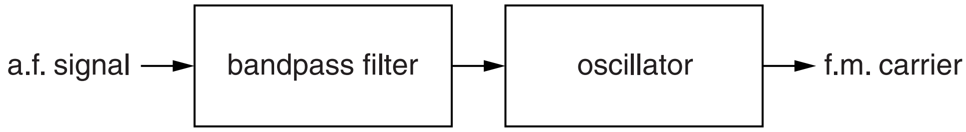

Fig. 3.1

(a) The bandpass filter restricts the bandwidth of the a.f. signal as shown in Fig. 3.2.

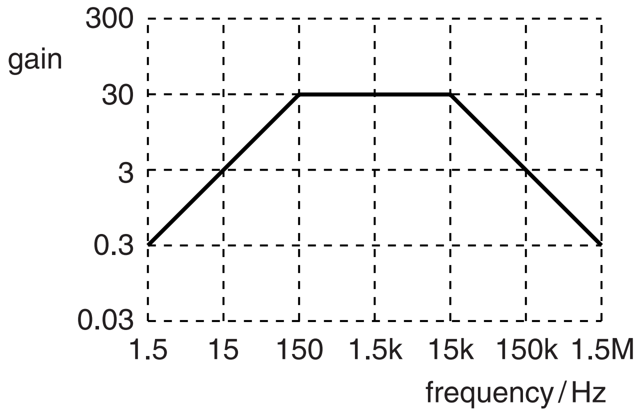

Fig. 3.2

(i) Draw a circuit for the bandpass filter on Fig. 3.3.
Show all component values and justify them.

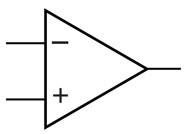

Fig. 3.3

[8]

(ii) Calculate the bandwidth of the frequency modulated (f.m.) carrier.

bandwidth = ... kHz **[2]**

(iii) Suggest why it could be important to restrict the bandwidth of the f.m. carrier.

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....

.... **[1]**

(b) The oscillator of Fig. 3.1 produces an f.m. carrier at its output from the filtered a.f. signal at its input.
Describe the transfer characteristic of the oscillator.

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.... **[3]**

[Total: 14]

4 Fig. 4.1 shows a block diagram and voltage-time graphs for a triangle wave generator for use in a pulse-width modulation system.

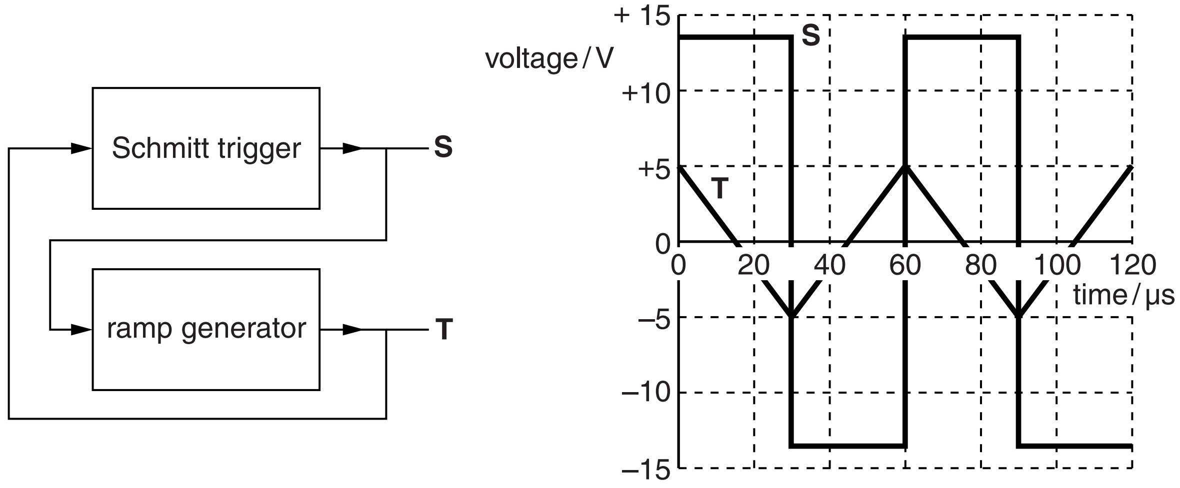

Fig. 4.1

(a) Complete Fig. 4.2 to show the circuit diagram **and** transfer characteristic for the Schmitt trigger. You do **not** need to show component values for the circuit.

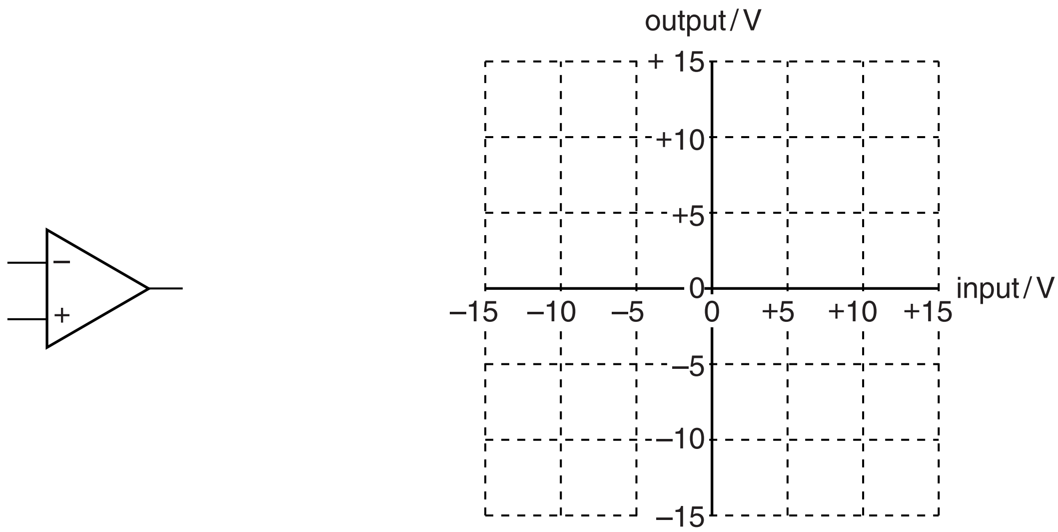

Fig. 4.2

[4]

(b) Using the graph of Fig. 4.1, calculate suitable component values for the ramp generator of Fig. 4.3.

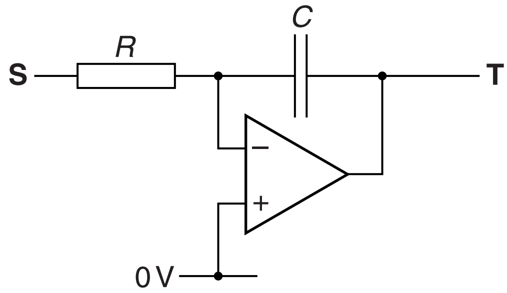

Fig. 4.3

R = ... Ω

C = ... F

[4]

(c) Explain the limits on the signal which can be successfully encoded when the triangle waveform generator of Fig. 4.1 is made part of the pulse-width modulator of Fig. 4.4.

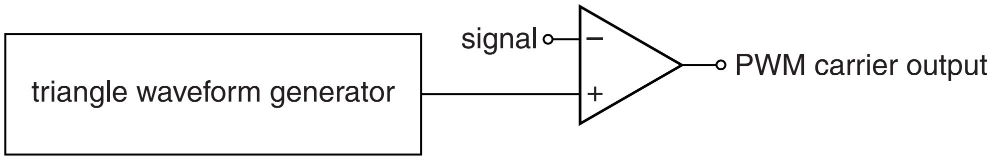

Fig. 4.4

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.... **[3]**

[Total: 11]

5 This question is about the reduction of noise and interference in communication systems.

(a) What is the difference between noise and interference?

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.... **[4]**

(b) Explain how the use of twisted-pair cable can reduce interference but not noise.

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.... **[4]**

(c) Explain how the use of a Schmitt trigger can reduce both noise and interference.

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.... **[2]**

[Total: 10]

6 Fig. 6.1 is an incomplete block diagram for a simple AM radio receiver.

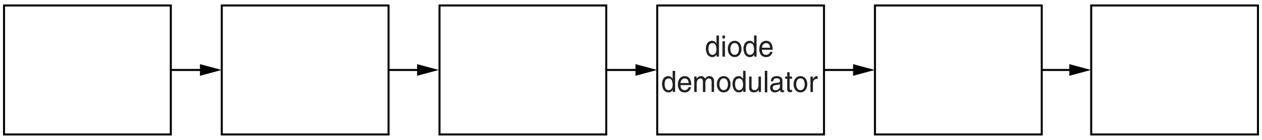

Fig. 6.1

(a) Complete the block diagram of Fig. 6.1 by choosing blocks from this list.

aerial **af amplifier** **loudspeaker**

ramp generator **rf amplifier** **Schmitt trigger** **tuned circuit**

[5]

(b) The diode demodulator can be assembled from a resistor, a capacitor and a diode.

(i) In the space below, draw a circuit diagram for the diode demodulator.
Label the input and output terminals.

[3]

(ii) Explain how the diode demodulator circuit works.

[3]

(c) Here are some changes which could be made to the simple AM receiver of Fig. 6.1.
Put a tick (✓) in the boxes next to the **two** changes which will increase the sensitivity of the receiver.

Increase the length of the aerial.

Increase the gain of the rf amplifier.

Decrease the gain of the af amplifier.

Increase the impedance of the loudspeaker.

Reduce the break frequency of the diode detector.

[2]

[Total: 13]

7 Figure 7.1 is a circuit diagram for a stacked filter in a superhet radio receiver.

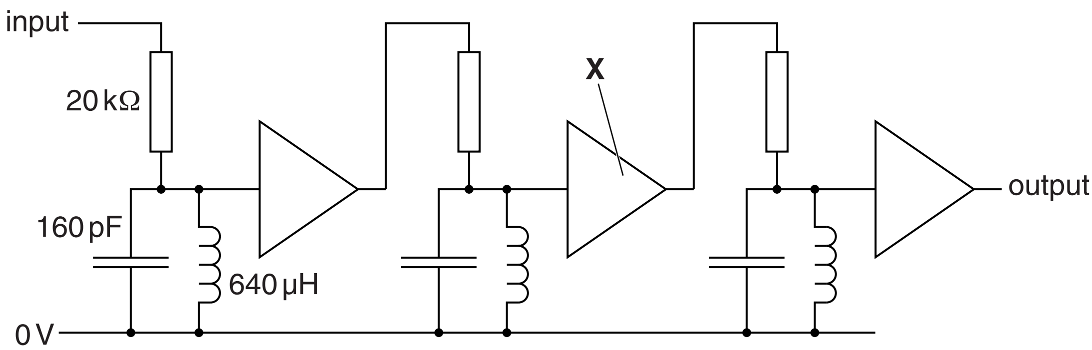

Fig. 7.1

(a) The first parallel LC circuit contains a 640 μH inductor.

(i) Show that the reactance of the inductor is about 200 Ω at a frequency of 50 kHz.

[2]

(ii) The graph of Fig. 7.2 shows how the reactance of the 160 pF capacitor depends on frequency. Sketch on the graph to show how the reactance of the 640 μH inductor depends on frequency. Label the graph **L**.

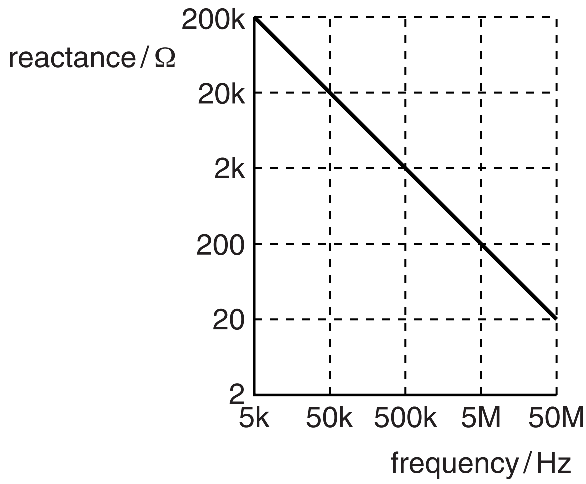

Fig. 7.2

[2]

(iii) Draw on Fig. 7.2 to show how the reactance of the 20 kΩ resistor depends on frequency. Label the graph **R**. **[1]**

(b) All three parallel LC circuits have 640 μH inductors, but they have slightly different capacitor values.
Explain why the three LC circuits in the filter need slightly different capacitors.

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.... **[3]**

(c) What is the component labelled **X**, and why is it included in the circuit of Fig. 7.1?

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.... **[3]**

[Total: 11]

8 Fig. 8.1 is the circuit diagram of a simple analogue-to-digital converter.

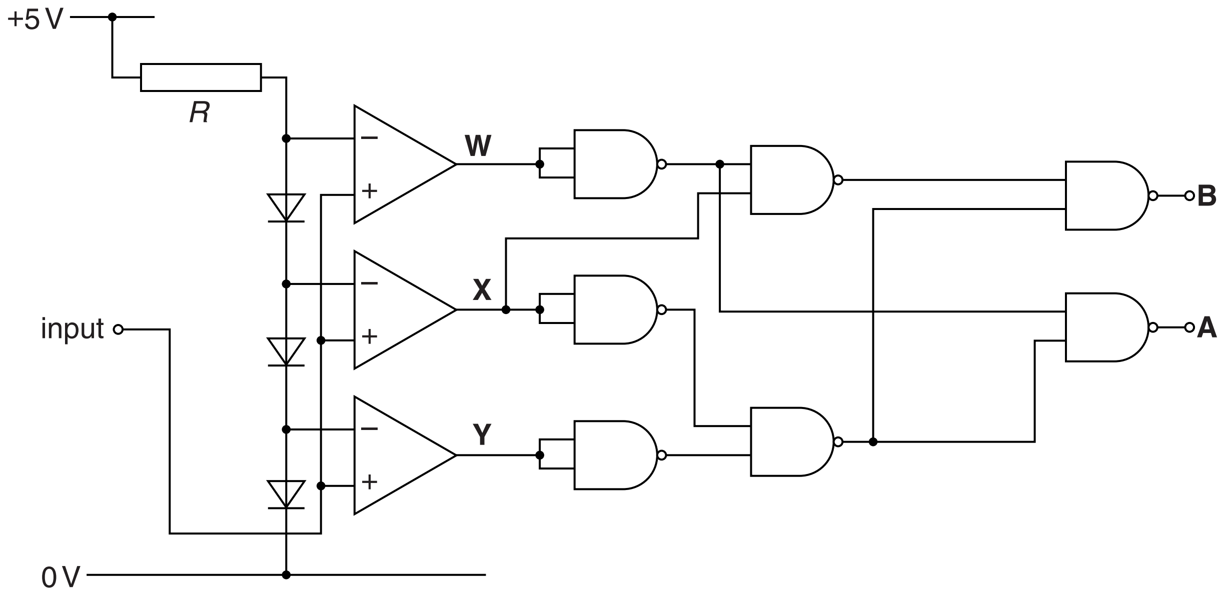

Fig. 8.1

(a) Each of the diodes is rated at 0.5 V, 2 mA.
Calculate a suitable value for the resistor *R* which limits the current in the diodes.

R = ... Ω **[2]**

(b) Each of the op-amps has outputs which saturate at +5 V or 0 V.

(i) Write down a Boolean expression for the output **B** in terms of the signals **W**, **X** and **Y**. Use the rules of Boolean algebra to simplify your answer.

[2]

(ii) Complete the table with **1** or **0**.

Input Signal	**W**	**X**	**Y**	**B**	**A**
0.25V					1
0.75V					0
1.25V					0
1.75V					1

[4]

(c) The converter has the following specification:

- resolution of 0.5V
- range of 2.0V
- word length of 2 bits

Explain how these three quantities are related to each other.

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....

....

.... **[2]**

(d) The converter has a response time of 15 μs.
Calculate the maximum input frequency that the converter can safely encode.

maximum input frequency = ... Hz **[2]**

[Total: 12]

9 Fig. 9.1 is the circuit diagram for a serial receiver of four-bit words.

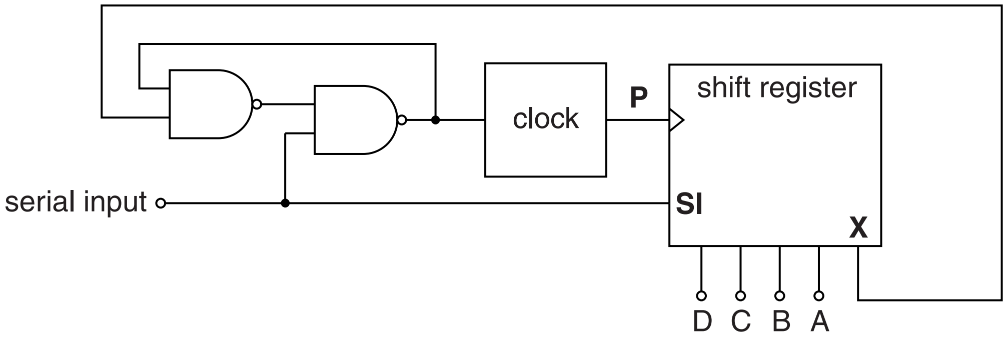

Fig. 9.1

(a) Explain why each four-bit word DCBA which arrives at the serial input is preceded by a 0 and followed by a 1.

....

....

.... **[2]**

(b) The receiver is designed to receive up to 2048 four-bit words per second. Suggest a suitable frequency for the clock of Fig. 9.1.

frequency = ... Hz **[2]**

(c) Complete the flip-flops of Fig. 9.2 to show how the shift register can be constructed.
Label all of the inputs and outputs.

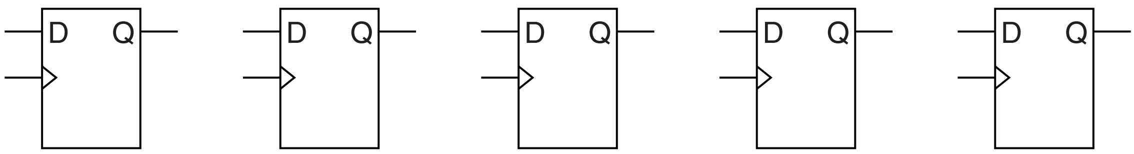

Fig. 9.2

[3]

(d) Complete the timing diagram of Fig. 9.3 for the circuit of Fig. 9.1.

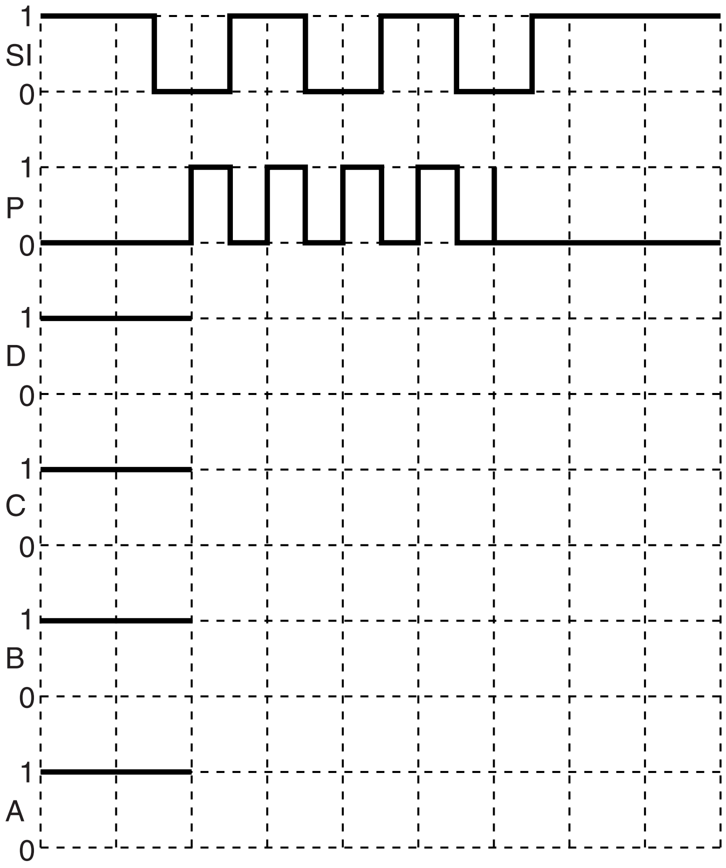

Fig. 9.3

[4]

[Total: 11]

Quality of Written Communication [3]

END OF QUESTION PAPER

PLEASE DO NOT WRITE ON THIS PAGE