OCR
RECOGNISING ACHIEVEMENT

Thursday 6 June 2013 – Afternoon

A2 GCE ELECTRONICS

F614/01 Electronics Control Systems

F/6280/7061/3

Candidates answer on the Question Paper.

OCR supplied materials:
None

Other materials required:
- Scientific calculator

Duration: 1 hour 40 minutes

F 6 1 4 0 1

Candidate forename		Candidate surname	

Centre number						Candidate number				

INSTRUCTIONS TO CANDIDATES

- Write your name, centre number and candidate number in the boxes above. Please write clearly and in capital letters.
- Use black ink. HB pencil may be used for graphs and diagrams only.
- Answer **all** the questions.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).
- Do **not** write in the bar codes.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **110**.
- You will be awarded marks for your Quality of Written Communication.
- You are advised to show all the steps in any calculations.
- This document consists of **20** pages. Any blank pages are indicated.

A scientific calculator may be used for this paper

DC (LEG/CGW) 61973/4

Microcontroller instructions

The microcontroller contains eight general purpose registers Sn, where n = 0, 1, 2 ... 7.
The microcontroller has an eight bit input port, I, an eight bit output port, Q, and an analogue input, ADC.

In the table of assembler instructions given below, Sd is the destination register and Ss the source register.

assembler	function
MOVI Sd,n	Copy the byte n into register Sd
MOV Sd,Ss	Copy the byte from Ss to Sd
ADD Sd,Ss	Add the byte in Ss to the byte in Sd and store the result in Sd
SUB Sd,Ss	Subtract the byte in Ss from the byte in Sd and store the result in Sd
AND Sd,Ss	Logical AND the byte in Ss with the byte in Sd and store the result in Sd
EOR Sd,Ss	Logical EOR the byte in Ss with the byte in Sd and store the result in Sd
INC Sd	Add 1 to Sd
DEC Sd	Subtract 1 from Sd
IN Sd,I	Copy the byte at the input port into Sd
OUT Q,Ss	Copy the byte in Ss to the output port
JP e	Jump to label e
JZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC, SHL or SHR was zero
JNZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC SHL or SHR was not zero
RCALL s	Push the program counter onto the stack to store the return address and then jump to label s
RET	Pop the program counter from the stack to return to the place the subroutine was called from
SHL Sd	Shift the byte in Sd one bit left putting a 0 into the lsb
SHR Sd	Shift the byte in Sd one bit right putting a 0 into the msb

There are three subroutines provided:

- readtable – copies the byte in the lookup table pointed at by S7 into S0. The lookup table is labelled table: When S7=0 the first byte from the table is returned in S0
- wait1ms – waits 1ms before returning
- readadc – returns a byte in S0 proportional to the voltage at ADC

Datasheet

Unless otherwise indicated, you can assume that:
- op-amps are run off supply rails at +15V and –15V
- logic circuits are run off supply rails at +5V and OV.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{out} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_d}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$ $\quad A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$ $\quad \overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$ $\quad A.B. + \overline{A}.C = A.B + \overline{A}.C + B.C$
amplifier gain	$G = -g_m R_d$
ramp generator	$\Delta V_{out} = -V_{in}\frac{\Delta t}{RC}$

Answer **all** questions.

1 Fig. 1.1 shows an incomplete MOSFET amplifier circuit.

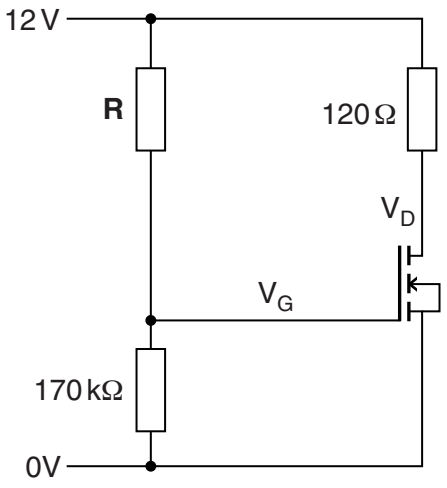

Fig. 1.1

(a) Add components and connections to Fig. 1.1 to show how an a.c. signal can be input and output from the amplifier.
Label the input and the output of the amplifier. **[2]**

(b) Calculate the value of **R** to make V_G = 3V.

R = ... kΩ **[3]**

(c) The graph in Fig. 1.2 shows how the drain current, I_{DS} through the MOSFET depends on the voltage at V_G.

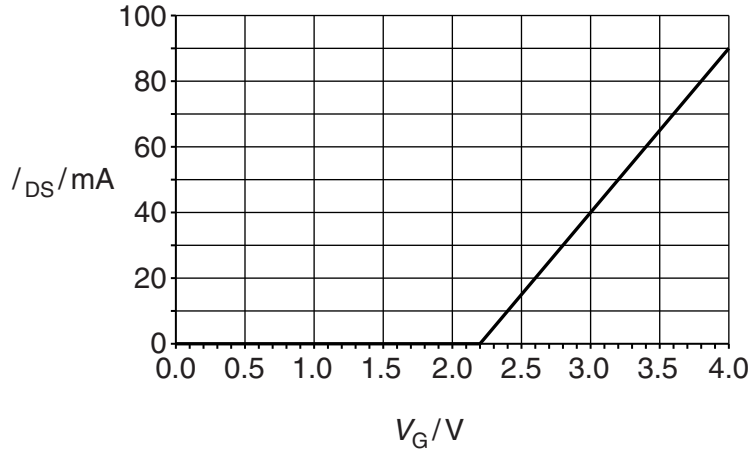

Fig. 1.2

(i) Use the graph to find the threshold voltage of the MOSFET.

threshold voltage = ... V **[1]**

(ii) Show that the voltage at V_D is about 7 V when V_G is 3 V.

[3]

(iii) Use information from the graph to calculate the transconductance of the MOSFET.

transconductance = ... S **[3]**

(iv) Show that the gain of the amplifier is –6.

[2]

(d) The graph below shows how the voltage V_G varies with time *t*.

(i) Draw on Fig. 1.1 to show how an oscilloscope can be connected to measure the voltage V_D. **[1]**

(ii) Draw on the axes of Fig. 1.3 to show how the voltage V_D varies with time.

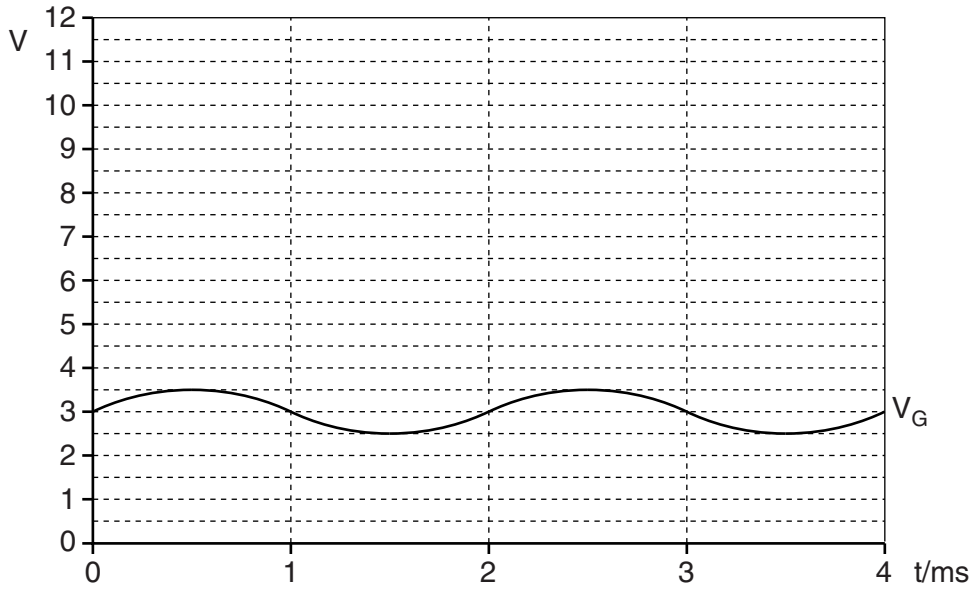

Fig. 1.3

[3]

(iii) Use the graph to find the frequency of V_G.

frequency = ... Hz **[1]**

[Total: 19]

2 Fig. 2.1 shows an incomplete block diagram of a switched mode power supply.

(a) Use the words below to complete the block diagram.

comparator **opto-isolator** **oscillator** **rectifier** **reference** **smoother** **transformer**

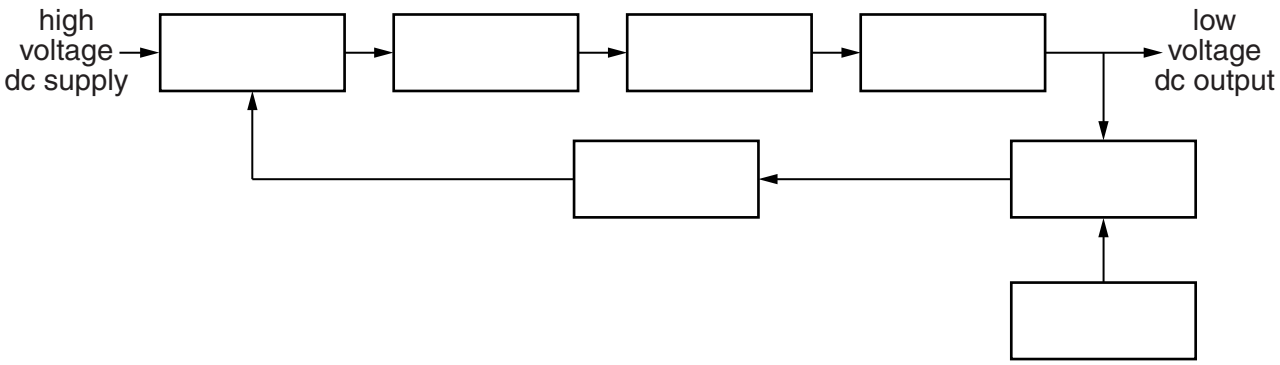

Fig 2.1 **[6]**

(b) Fig. 2.2 shows the circuit diagram of the full-wave rectifier in Fig. 2.1.

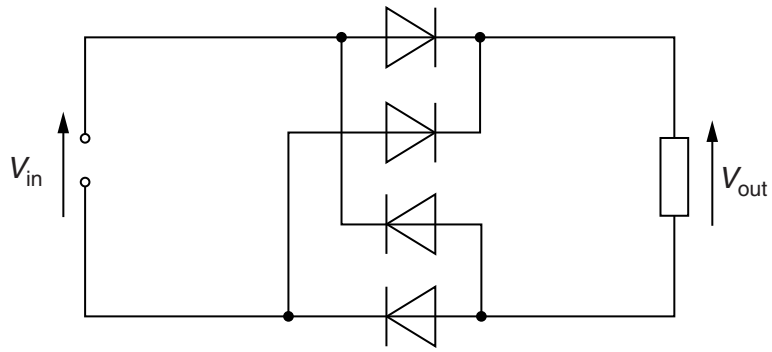

Fig. 2.2

Fig. 2.3 shows how the voltage at V_{in} varies with time t.

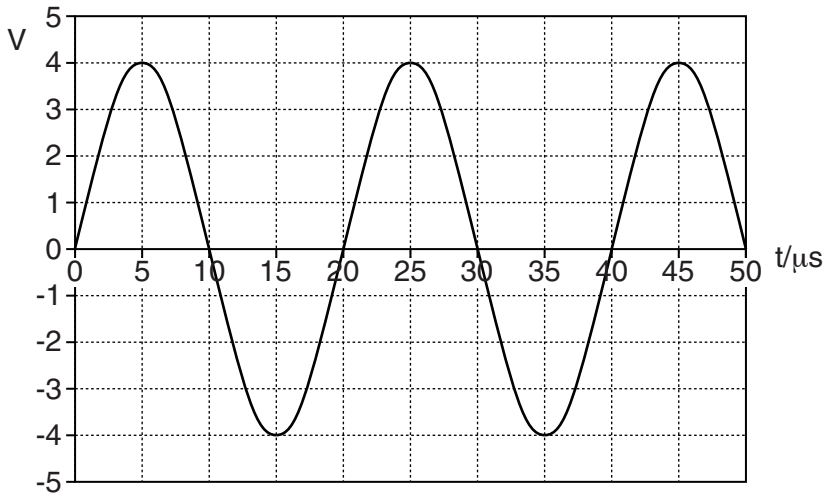

Fig. 2.3

Draw on the axes of Fig. 2.3 to show the voltage V_{out} from the rectifier in Fig. 2.2. **[4]**

(c) The opto-isolator contains an LED and a phototransistor.
Explain how an opto-isolator works by referring to the function of each of these components.

.....

.....

..... **[2]**

(d) Explain the function of the transformer in the power supply.

.....

.....

..... **[2]**

[Total: 14]

3 Fig 3.1 shows the incomplete block diagram of a system containing a microcontroller.

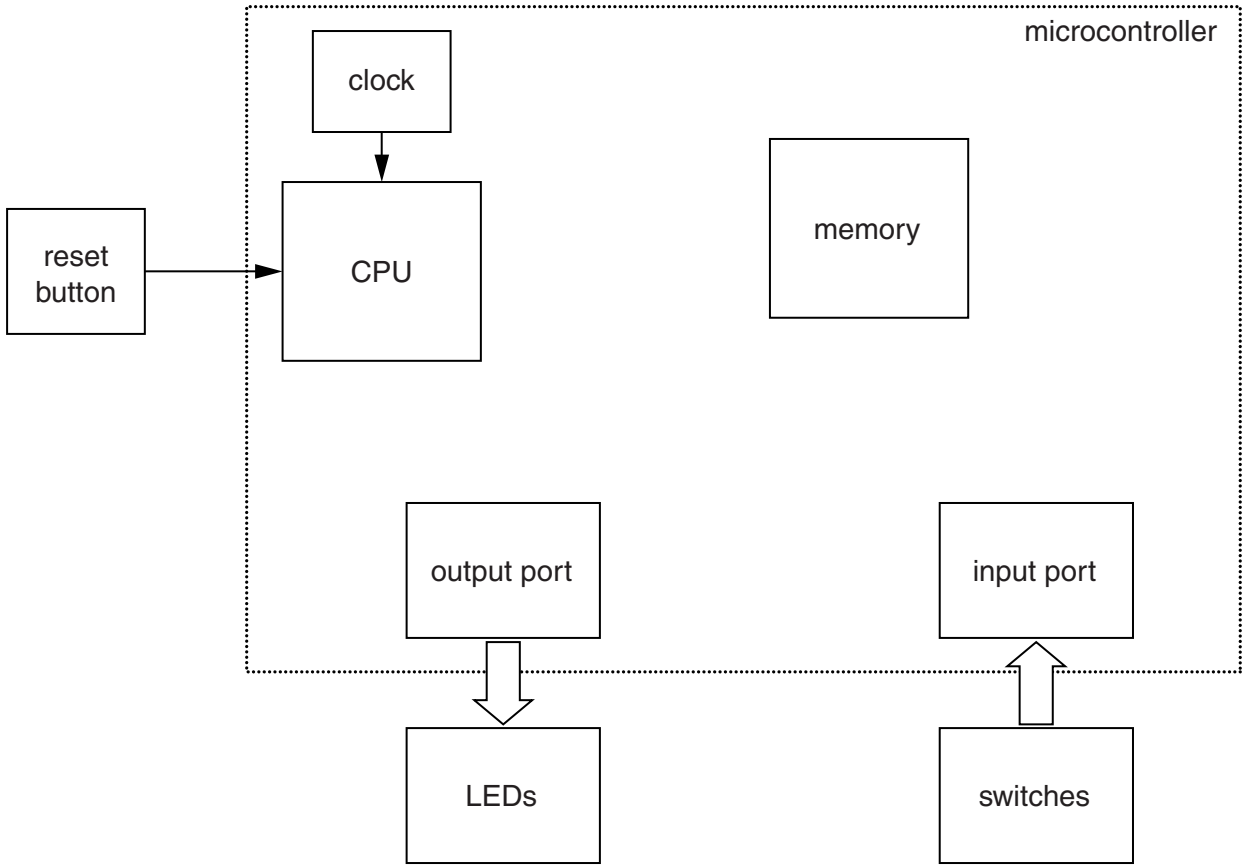

Fig. 3.1

(a) Complete the block diagram of the microcontroller by drawing and labelling:
the address bus, control bus and data bus.
Put arrow heads at the end of the buses to show the direction of flow of information. **[6]**

(b) Describe what happens in the CPU during one machine cycle.

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.....

.....

..... **[5]**

[Total: 11]

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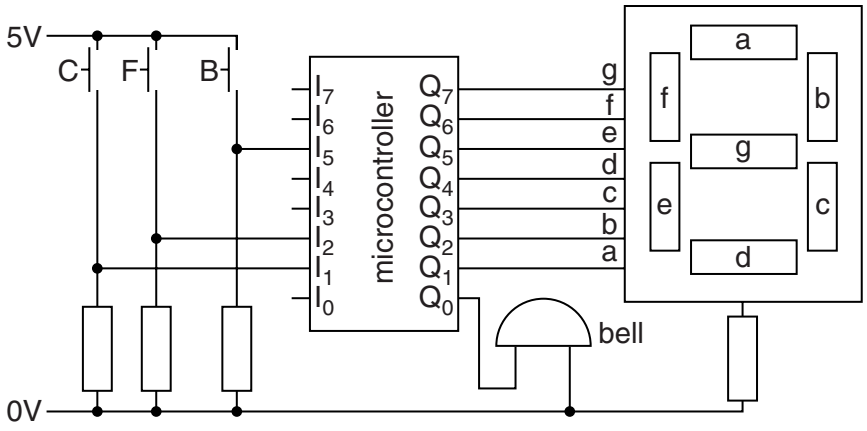
4 Fig 4.1 shows the circuit and main program for the door bell in a house.




```
start:    RCALL check1
          RCALL check2
          RCALL check3
          JP    start
```

Fig. 4.1

(a) Complete the subroutine `check1` so that the subroutines `show1` and `show2` are called when switch F is pressed otherwise the subroutine returns to the main program.

```
check1:   .....

          .....

          .....

          JZ    endf
          RCALL show1
          RCALL show2
endf:     RET
```

[4]

(b) Complete the subroutine `show1` to display F on the 7-segment display and turn the bell off.

```
show1:    MOVI S2,.....

          .....

          .....
```

[3]

(c) The subroutine `wait200ms` produces a delay of 200 ms.
Complete the subroutine `wait200ms`.

```
wait200ms:.....

delay:    RCALL wait1ms
          DEC   S5
          JNZ   delay
          RET
```

[2]

(d) Describe the effect of the subroutine `show2` on the output devices shown in Fig. 4.1.

```
show2:    MOVI  S3, 01      .....
          MOVI  S4, 06
loop:     EOR   S2, S3      .....
          OUT   Q, S2
          RCALL wait200ms   .....
          DEC   S4
          JNZ   loop        .....
          RET
                            .....
```

.....

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.....

..... **[4]**

(e) Write a subroutine to turn the bell on for 600 ms without affecting the display.

[8]

[Total: 21]

5 Fig 5.1 shows the circuit diagram for a full adder.

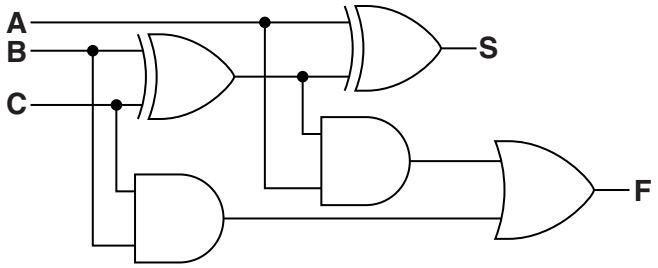

Fig. 5.1

(a) Complete the truth table for the full adder.

C	B	A	F	S
0	0	0		

[2]

(b) Fig 5.2 shows a system for adding binary numbers together.

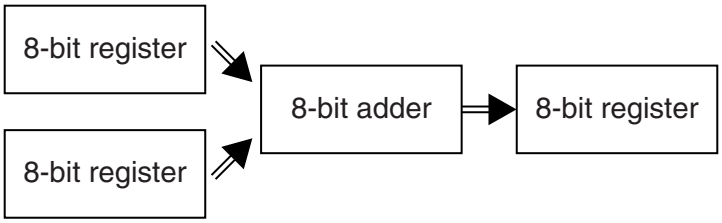

Fig. 5.2

(i) Complete the circuit in Fig. 5.3 for a 4-bit register for the parallel processing of binary words.

- Label the following:
- inputs A_0, A_1, A_2, A_3
- outputs Q_0, Q_1, Q_2, Q_3
- the signal X which makes the register store the word at the inputs

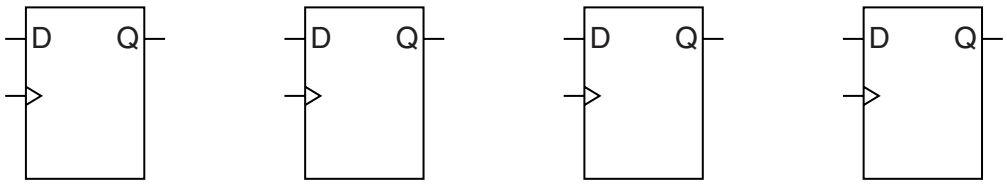

Fig. 5.3

[3]

(ii) Fill in the boxes to show the addition of the two binary numbers 0111 0110 and 0101 0100.

		0	1	1	1	0	1	1	0
	+	0	1	0	1	0	1	0	0
sum									
carry									

[3]

(c) Show how the decimal number –42 can be obtained using two's complement.

[3]

[Total: 11]

6 A circuit for controlling the position of a satellite dish is shown in Fig. 6.1.

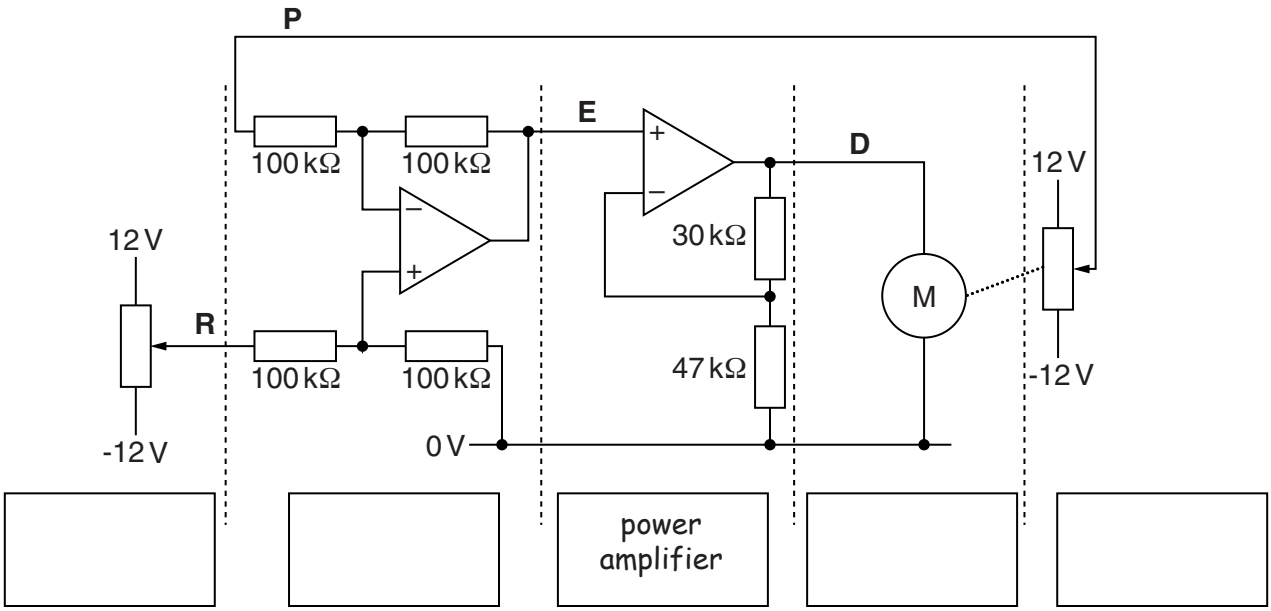

Fig. 6.1

(a) Label the sections of circuit diagram in Fig 6.1 using the labels. One of the labels has already been written in for you:

difference amplifier **motor** **position sensor** **power amplifier** **reference**

[1]

(b) Show that the voltage gain of the power amplifier is about 1.6.

[2]

(c) Name the component used to control the voltage at **R**.

..... **[1]**

(d) **P** is initially 5V. Then the user moves the dish by changing **R** to 2V.
For **R** = 2V and **P** = 5V:

(i) calculate the voltage at **E**

voltage at **E** = ...V **[2]**

(ii) calculate the voltage at **D**

voltage at **D** = ...V **[1]**

(iii) Explain how the circuit works to move the satellite dish to the set position. Refer to the voltages at R, P, E and D in your answer.

.....

.....

.....

.....

..... **[4]**

(e) Explain why the circuit uses proportional feedback instead of on-off feedback for controlling the position of the satellite dish.

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..... **[4]**

[Total: 15]

7 Fig. 7.1 shows the circuit diagram of a volatile memory cell.

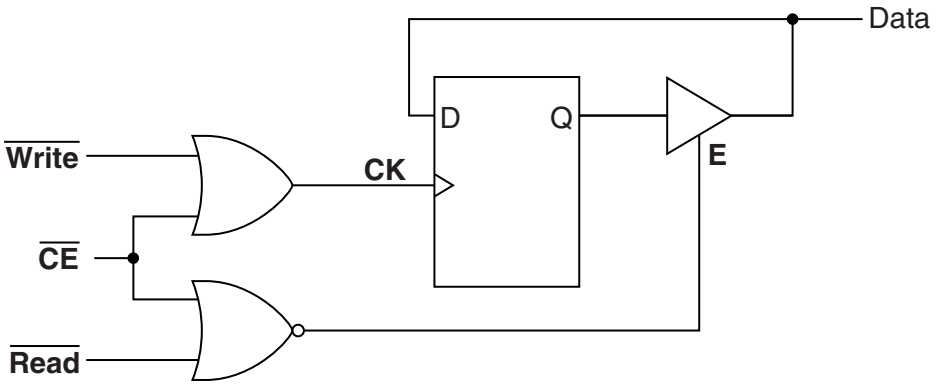

Fig. 7.1

(a) State what the word 'volatile' means in reference to a memory cell.

.....

..... **[1]**

(b) Complete the truth table for the logic system in the memory cell.

$\overline{\text{CE}}$	$\overline{\text{Read}}$	$\overline{\text{Write}}$	CK	E

[3]

(c) Describe the sequence of logic levels needed on $\overline{\text{CE}}$, Data, $\overline{\text{Read}}$ and $\overline{\text{Write}}$ to store a logic 1 in the memory cell.

.....

.....

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.....

..... **[5]**

(d) Fig. 7.2 shows a memory module.
Explain why the memory module contains 6 memory cells.

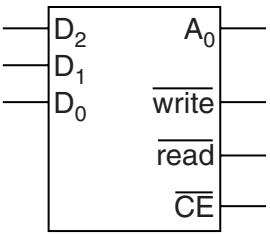

Fig 7.2

.....

.....

.....

..... **[2]**

(e) Complete the circuit diagram in Fig. 7.3 to show how the memory module in Fig. 7.2 can be built from memory cells and other components.

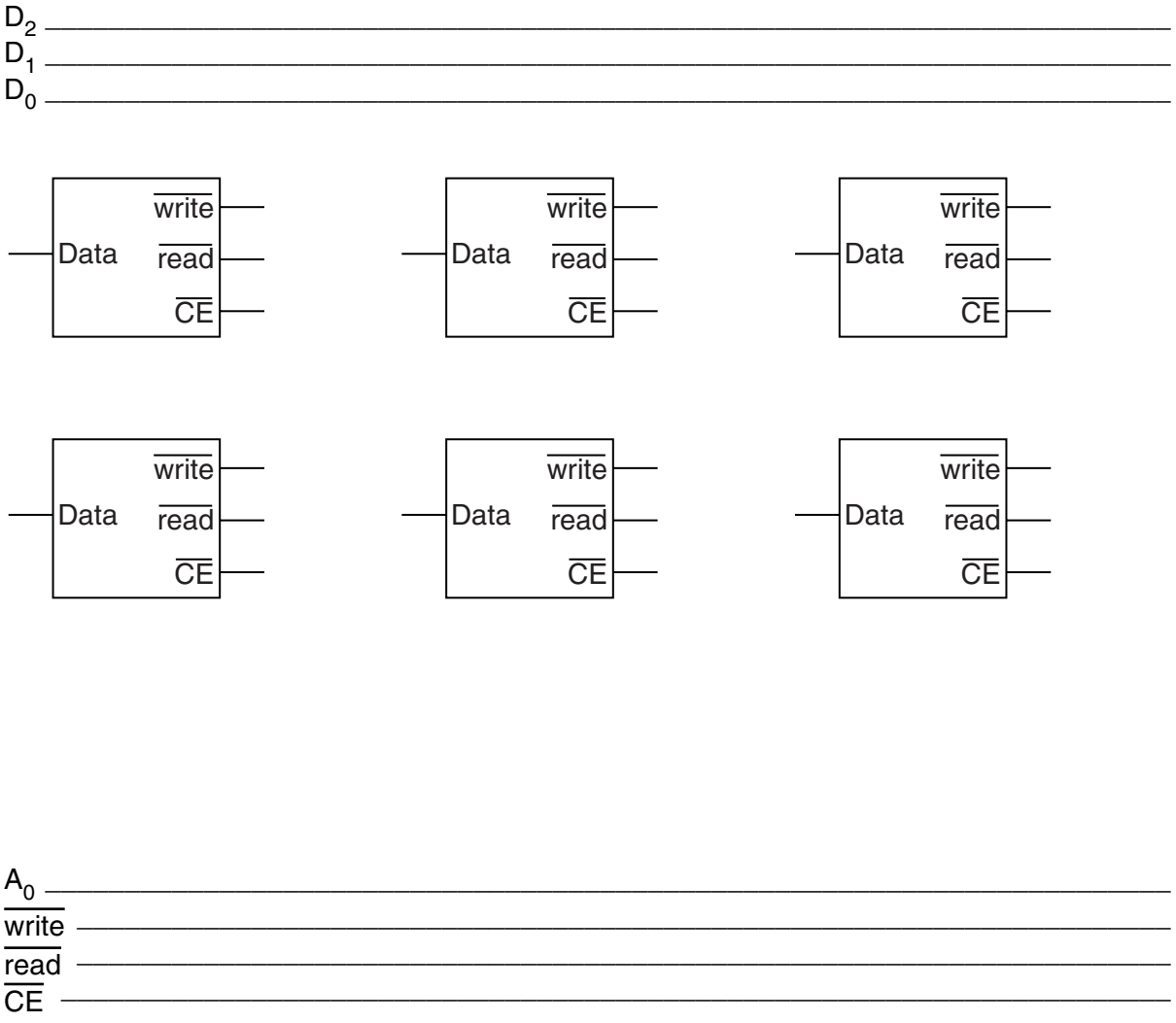

Fig. 7.3

[5]

[Total: 16]

Quality of Written Communication [3]

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