OCR
RECOGNISING ACHIEVEMENT

GCE

Electronics

Advanced GCE **A2 H465**

Advanced Subsidiary GCE **AS H065**

Examiners' Reports

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EXAMINERS' REPORTS

F611 Simple Systems

General Comments

Most candidates attempted all questions and there was no evidence that candidates were rushed; where questions where not attempted by some candidates these tended to be weaker candidates not attempting the more challenging questions.

Comments on Individual Questions

Question 1 was about a simple logic system. The question started with the completion of a truth table and writing a Boolean expression for one of the columns which was unproblematic for almost all candidates. Almost all candidates know how to make NOT gates and AND gates from NAND gates, a significant proportion of candidates could not remember or work out how to make a NOR gate from NAND gates or state clearly why using only NAND gates might be advantageous.

Question 2 was about a comparator system. Almost all candidates knew how to combine resistors to make to make a desired value. The potential divider calculations were straightforward for the majority of candidates. Most candidates could not explain that the op-amp input had a high impedance or drew (almost) no current in 2c. Simple calculations for the value of current limiting resistor in series with an LED continue to be a problem for most candidates with the majority not finding the correct pd across the resistor. The written explanations tend to discriminate well between candidates with much clear, logical thinking from the better candidates and some incorrect and confused ideas from weaker candidates.

Question 3 tested ideas about RC circuits. The calculation of time constant was straightforward and indicated that almost all candidates had no problems with k and μ and the use of standard form. Many candidates could not calculate the time for the voltage to fall to 2.5V, incorrect answers frequently halving the time constant. There were some good graphs and explanations of the operation of the circuit which showed good understanding from the stronger candidates.

Question 4 was about an astable circuit. Calculation of time period was straightforward for the vast majority of candidates. Many candidates could not calculate the required values of R and C for the astable but remembered that they needed to use at least 10kΩ for the resistor; most chose 10kΩ which made the calculation straightforward. The drawing of an oscilloscope on the circuit was straightforward but the drawing of the expected trace was more challenging with only the better candidates showing the correct period. When adding a switch and resistor to the circuit about a quarter of candidates did not know what to do with the resistor and placed it incorrectly. The speaker current calculation was unproblematic. About two thirds of candidates could choose the suitable MOSFET and almost all of them could explain their choice. A significant number of candidates thought that the power was significant and calculated the power in the speaker to choose a MOSFET.

Question 5. The block diagram was completed well but more than half candidates could not state that the arrows represented the flow of information; most incorrect answers showed confusion with other uses of arrows on lines in circuit diagrams or flow diagrams with "current" being a very common incorrect answer. Candidates know the characteristics of the LDR and can recognise its symbol. The graph of diode characteristics was drawn well by about half of the candidates, many candidates wrongly showed a reverse breakdown of a few volts. The best candidates could calculate the correct value for R to make the output 5V spotting that 07V was dropped across the diode, about half the candidates gained some marks through valid attempts e.g. correctly calculating the current through the 22kΩ resistor. Most candidates knew that F was a potentiometer and could suggest why it was included in the circuit.

Question 6 was about a truth tables and Boolean algebra. Quite a few candidates offered a simplified statement for W rather than the full expression from the truth table, which gained the mark. As in previous years, Boolean manipulation is a good discriminator, straightforward for the strong candidates and difficult for weaker candidates. Most candidates picked up some marks by showing some understanding of Boolean algebra. Candidates mostly know why power lines are not included in circuit diagrams but there was some confusion amongst a minority of candidates about logic gates and power. Using the Boolean expression to completing the truth table and design the logic circuit was straightforward for most candidates.

F612 Signal Processors

General Comments

The overall performance on this paper was very close to that of previous years. No candidate earned all of the marks available, although every mark on the paper was earned. Very few candidates earned marks in single figures. It was good to see that the paper discriminated well between weak and strong candidates.

There was no evidence that a significant number of candidates ran out of time before they had been able to complete the paper. The few questions which weak candidates chose not to answer were all aimed at candidates operating at grade A or above.

The microcontroller questions were better answered than in the previous two sessions, but many candidates still fail to explain the operation of a flowchart by considering its interaction with the input and output signals, relying instead on a direct translation of the symbols into English.

Although strong candidates show their calculations clearly and express their answers to an appropriate number of sig.figs., weak candidates often do not. This is especially important in 'show that' questions where marks are awarded for clearly showing each stage of a calculation as well as evidence that the candidate actually carried out the calculation.

One question asked candidates to describe how they would set about testing the transfer characteristic of a circuit. Weaker candidates either described a theoretical test or failed to mention any input and output devices. A number of candidates elected to use voltmeters to measure a.c. signals or used potentiometers to generate them, suggesting a lack of practical experience in this area.

Comments on Individual Questions

1 This question was designed to test the candidate's understanding of inverting amplifiers. It provided excellent discrimination. Part (a) was correctly answered by the majority of candidates, with a few confusing the input of the amplifier with the input of the op-amp. Although most candidates were able to correctly calculate the magnitude of the amplifier gain in part (b), a number failed to record that it was negative. Only the better candidates remembered that the inverting input of an op-amp is a virtual earth and were able to correctly draw the transfer characteristic of the amplifier. It was disappointing to find that many candidates attempted to draw this without the aid of a ruler. Part (c) taxed many weak candidates. Many chose to not answer part (i), and failed to realise that part (ii) was asking them to ask what they would do to test the circuit in the laboratory.

2 In previous sessions, candidates have found the microcontroller question to be the most challenging one. This year was little different. Despite a flying start with part (a), where weak candidates lost marks by omitting leading zeroes in hexadecimal quantities, the vast majority of candidates failed to explain the flowchart of part (b). Candidates need to realise that simply translating the flowchart segment into English cannot earn them any marks; they need to discuss the signals at the inputs or outputs in some detail to earn the marks with this type of question. Part (c) required candidates to draw a flowchart for themselves. Most had a go, but few earned all of the marks. It was nice to see that more candidates were restricting themselves to the symbols listed on the data sheet, but too many candidates had clearly had little practice at this sort of task.

3 This question about ports and registers also discriminated well between weak and strong candidates. Most of them were able to demonstrate a good understanding of flip-flop timing diagrams in part (a), with only weak candidates failing to describe flip-flop operation clearly enough to earn all of the marks in part (b). Too many assumed that the clock was triggered by levels instead of edges. Although many candidates were able to describe the function of a

register in a microcontroller, too many confused its construction with that of a binary counter. It was interesting that only a minority of strong candidates were able to completely describe the function of a microcontroller port.

4 This question about passive filters provided less discrimination than the previous questions. Most candidates had little difficulty with the break frequency calculation of part (a), but almost half failed to correctly identify the type of filter and many appeared to be guessing their way through the fill-the-gaps explanation of its action. Perhaps they had only met active filters based on op-amps? However, it was good to see that the majority of candidates could correctly draw the filter's transfer characteristic, with fewer than before dropping at other than 45° after the break frequency. Only a minority of candidates could give a practical reason for the inclusion of a tone control in the amplifier system of part (d) – a general description of a filter was not enough – and could explain why a large current was required at the output.

5 This question was about a one-shot sequential system. Candidates were presented with a circuit diagram and then asked a series of questions about detailed operation of parts of it. It was disappointing to find so many candidate unable to explain how the use of an AND gate to block or transmit pulses in part (a), with many assuming that a high signal at the clock input of the flip-flop would pass straight through to the Q output. In part (b), too many weak candidates ignored the signal resetting the counter and simply assumed that the oscillator had to have a frequency which was eight times that of the signal at S. The timing diagram of part (c) proved to be equally challenging, with only a minority of candidates able to earn all of the marks. Too many candidates appeared to be relying on memory rather than working out how each row was caused by the row above. Many candidates did not realise that a binary counter is triggered by falling edges at its input. Part (d) was about the use of flip-flops to make a binary counter. As expected, weak candidates failed to provide enough detail about the flip-flop operation in a one-bit counter, and didn't attempt to connect them together to make a register.

6 Impedance matching is one of the hardest concepts of the module, so this question proved to be most discriminating of the paper. The non-inverting amplifier calculation of part (a) was hard for weak candidates who chose the wrong formula from the data sheet or selected impractical resistor values of only a few ohms. Part (b) explored the candidates understanding of input and output resistance. Although strong candidates had no trouble in recognising the input resistance for part (i), many weak candidates failed to interpret the circuit diagram correctly and simply chose the output resistance of the sensor instead. Part (ii) required candidates to do a two-part calculation; just over half of the candidates were able to do this convincingly. Part (iii) proved to be the hardest question of the paper. A minority of candidates were aware that the input resistance needed to be at least ten times the output resistance of the previous stage for efficient signal transfer.

7 Although most candidates could explain the meaning of the term 'active-high reset' satisfactorily, only a minority could use the bistable circuit to explain this. Although strong candidates had no difficulty in earning all of the marks for the timing diagram of part (c), weaker candidates didn't realise that the outputs had to have opposite states at all times, and that they had to change as soon as one or other of the inputs went high. Candidates who failed to line up their rising and falling edges with a ruler risked the loss of a mark – too many freehand attempts failed to show that the outputs were changing on the rising edges of the input signals.

F613 Build and Investigate Electronic Circuits

In this third year of the current specification, moderators reported that the quality of the raw marking was much better than in previous years and that far fewer adjustments were necessary. This may be due to the fact that being the third year of this specification, centres have become used to its requirements and have adjusted successfully to the new marking criteria. It is interesting to note that some centres have approached this coursework by giving the candidates a 'mini project' which consists of a digital subsystem, an opamp subsystem, and a microcontroller subsystem. This is perfectly acceptable as long as there is clear demarcation of the three subsystems. Other centres have used the coursework as a teaching tool to demonstrate how a larger system is formed from smaller subsystems. They give the candidates a number of different subsystems to investigate which, when completed and connected together, form the larger system. This is good not just for those who will continue to do the A2 year but for all to see how larger systems are created from smaller ones.

As a result of the improved marking, it is only necessary to comment on a small number of the criteria which are still causing some problems.

Perhaps the most important consideration is the choice of subsystem. It must be one in which the candidates will be able to perform a good deal of testing. Some of the subsystems chosen, especially digital ones, may not provide sufficient scope to perform a full testing regime to satisfy the top mark for criterion 3a.

In order to score full marks for criterion 1a, candidates must fully describe the subsystem at component level. This has caused some problems, especially for opamp filter circuits. Some candidates were awarded 4/4 but were not fully describing the role of the capacitor and how its frequency dependent reactance affected the gain of the circuit.

The test plan (criterion 1b) is still causing trouble for some. This must be a **plan**, that is, it is done before any testing is performed and should fully describe how the subsystem is to be fully tested. The diagram that accompanies the test plan should show where testing equipment is to be placed, using the recognised symbols for the testing device.

Presentation of results was also noted by moderators. The problem here was especially with digital subsystems. A table of results showing the various states of the inputs/outputs is perfectly acceptable. However, **real** results must be shown. A table showing '1' and '0' for real results is not acceptable, especially if the test plan is poor and does not indicate how the results are to be taken.

F614 Electronic Control Systems

General Comments

Most candidates attempted all questions and there was no evidence that candidates were rushed with the majority of candidates achieving good marks throughout the paper. A significant minority of candidates did not attempt to answer 3(d)/3(e) about the opto-isolator and 5(c)/5(d) using the graph to calculate V_D for the MOSFET amplifier, this probably indicates a lack of confidence with this material for these candidates. It was pleasing to see that candidates have experience of programming and can understand programmes and write their own subroutines. The performance across the range of questions in the paper shows that the majority of candidates have a sound understanding of all of the topics in the specification.

Comments on Individual Questions

Question 1
1(a) Most candidates could complete the table accurately but there were some responses which did not show the logic states 0 or 1 with just 'low impedance' and 'high impedance' as answers, not necessarily in the correct place.
1(b) Many candidates stated what a tristate was but failed to state why the tristate was used (to allow many outputs to the same data bus/ to allow for a bi-directional bus).
1(c)/1(d) Explanations tend to discriminate well between the strong candidates and the weak candidates. Answers to parts (c) were sometimes found in (d) and vice versa, the marks were awarded wherever they were found. The stronger candidates gave very full and clear explanations to this question and gave more than enough for full marks, the weaker answers demonstrated some confusion, particularly about the role of the capacitor and the MOSFET.

Question 2
2(a) This was straightforward for most candidates but drew their attention to the function for (b).
2(b) Many candidates could complete this accurately but some made a few errors. There was evidence of candidates thinking through their answers with a little crossing out and changing of response with only a few completely random answers for the very weakest candidates.
2(c) There were a range of responses to this question. The common errors were using 5V for V_{in}, missing out the minus sign and not realising that the calculation of ΔV_{out} was the change in output so needed to be added to the 5V.

Question 3
3(a) Most candidates could explain why this was a closed loop system but many of the incorrect responses concentrated on the comparator rather than the feedback loop.
3(b) Was difficult for most candidates and many incorrect responses seemed to be discussing the difference between on-off and proportional feedback.
3(c) Most candidates could complete this but there were a significant proportion who could draw a rectifier but not make appropriate connections to it.
3(d) The strongest candidates could answer this well but the majority did not get full marks often having difficulty remembering the phototransistor. About one third of the candidates gained no marks for this part.
3(e) The marks were similar to 3(d) with some candidates recalling the safety function of the opto-isolator and some explaining its function in controlling the output voltage.
3(f) This question discriminated well between candidates with some very good answers but many partially correct. Common errors were to stabilise the top graph at 6V and failure to realise that the bottom graph was either high or low.
3(g) This question was intended to be stretching and proved challenging for most candidates.

Question 4

4(a) Candidates showed good familiarity with programming and could easily understand the first two lines of the program.

4(b) The majority of candidates could write the subroutine without problem, the most common error was from candidates who lost one mark by omitting the RET at the end of the subroutine.

4(c) Candidates found this subroutine slightly more challenging but could get the correct hex code. The most common error was jumping to the wrong place often 'loop'.

4(d) This question discriminated well between candidates with a full range of marks. Most candidates could tell that the subroutine turned off the heater and motor and blue LED and then turned on the yellow LED with some time delay. The most common errors did not say tat the yellow LED flashed and failed to identify the time delay as 100ms with many thinking that the delay was 64ms.

4(e) Nearly all candidates could identify an advantage of using subroutines but many described what a subroutine was rather than identifying a second advantage. Describing what happened to the registers at the end of a subroutine was more challenging, with some stating that the stack pointer stored the return address. The strongest candidates could provide very clear accounts of the registers and the stack at RET.

4(f) Good answers stated that the program went back to start and then referred to the output devices, weaker answers were confused about the effect of the reset pin on the output devices and did not notice that the program restarted.

Question 5

5(a) This was straightforward for candidates with almost all gaining full marks.

5(b) Calculation of the unknown resistor value was unproblematic.

5(c) Most candidates could read the value of the current from the graph and calculate the pd across the 180Ω resistor. The most common error was to neglect to calculate V_D by subtracting the pd across the resistor from the 15V supply. 5(d) About half the candidates realised that the quiescent value of V_D was to avoid clipping.

5(e) Candidates clearly understood threshold voltage and could get this mark, the very few problems seemed to be with reading the scale on the graph accurately.

5(f) Many candidates could identify the 180Ω resistor as being important but only the strongest candidates could accurately calculate g_m from the graph.

5(g)(f) This was intended to be a stretching question and was difficult for most candidates but there were some very good answers here and many candidates could recall some details of the MOSFET amplifier design and realised that MOSFETs do not all have the same characteristics and so gained some marks.

Question 6

6(a) Most candidates could calculate the number of memory cells as 16 but a number wrongly gave the answer 2^8=256.

6(b) Was often answered well but some candidates could only clearly explain the two data lines or the three address lines and so received half marks.

6(c) Pleasingly, a very high proportion of candidates could show how to connect up the two memory modules gaining full marks and showing good familiarity with this aspect of the specification.

6(d) was a more stretching task, almost all candidates could make a good start at this but only the strongest candidates could produce a fully functioning design. There were a wide variety of valid full mark solutions presented, not all of them efficient, showing that candidates had worked out how to do this rather than simply recalled a solution.

F615 Communication Systems

General Comments

The paper necessarily contains a number of stretch-and-challenge questions. These are characterised by a lack of scaffolding, requiring candidates to find their own way through to an explanation or calculation. Weak candidates tended to move straight on to the next question. This may not be a good strategy – it is surely better to have a go and risk earning a mark or two rather than leaving a blank space.

Centres need to realise that a paper of this length will be able to probe a candidate's understanding of most parts of the specification each year. It is therefore a good idea to ensure that candidates are introduced to all parts of the module and not allowed to miss out the more difficult parts, such as superhets, Schmitt triggers and ramp generators.

A large number of the marks for this paper are for synoptic tasks, some candidates would have benefited from revision of the relevant parts of the A/S course.

Candidates need to consider carefully their use of technical terms in their explanations of circuit operation. For example, it appears that some candidates equate voltage with amplitude and bandwidth with data transmission rate.

Finally, the paper contained a number of show-that questions. Weak candidates often approach these on a trial-and error basis. Good candidates earn the marks by explaining each step in full, with words or formulae, and quoting the answer to a number of sig. figs. which shows that they have actually done the calculation.

Comments on Individual Questions

1 This question on video communication was, as intended, a straightforward start to the paper. In part (a) the majority of candidates could name all five signals, although weak ones could often only name the two synchronisation ones. Too many good candidates provided insufficient detail in their account of the advantages of digital signals. Candidates need to look at the mark allocation and make sure that their answer contains at least the same number of distinct steps. The calculations of part (b) proved to be straightforward for the vast majority of candidates, with only a small minority unable to calculate the number of brightness levels from the number of bits per pixel. As always, the bandwidth calculation of part (c) only proved to be straightforward for strong candidates, with weak candidates often doubling the bit rate to find the bandwidth instead of halving it. Most candidates earned full marks for part (d), showing an excellent understanding of compression.

2 This question on radio receivers allowed most candidates to earn at least half of the marks Part (a) was probably the easiest question on the paper, with only a few candidates confusing the rf amplifier with the af one. It was good to find that in part (b) the vast majority of candidates could remember how to design an inverting amplifier from their AS work. Part (c) about selectivity and sensitivity was more challenging. Although most knew what selectivity was, too many weak candidates either seemed to think that sensitivity was the same thing or attempted to improve it by changes which were more appropriate to boosting the selectivity. Part (d) was about superhets. It was good to find that most candidates were able to complete the block diagram, but a disappointing number of candidates appeared to know little about the operation of the system. Part (ii) was designed as a stretch-and-challenge question, allowing the strongest candidates to show what they knew, but it was expected that weaker candidates should be able to earn a mark or two.

3 Pulse width modulation is a relatively recent addition to the specification, so it was expected that some candidates would not be as well prepared for this question as they were for the others. In fact, it was good to find that centres have done a good job in mastering this topic, so that candidates were able to make good headway. However, in part (a)(i) too many weak candidates felt that they had to use both the amplitude and frequency to calculate the period of the waveform – they were clearly uncomfortable with the idea of only using part of the information provided. The majority of sketches of the triangle waveform were excellent, although candidates who drew freehand without the aid of a ruler risked losing marks. As ever, many weak candidates assumed that the period was the time for only half of a cycle. The square wave sketch proved to be more challenging, with many candidates forgetting the saturation levels for op-amps, assuming the output had to be a logic signal alternating between 5 v and 0 V or getting the incorrect phase with respect to the triangle wave. Although the strongest candidates had no trouble earning all of the marks for their design of treble cut filter in part (b)(i), many weak candidates did not know the correct circuit and only earned credit for using resistor values in a sensible range. Part (b)(ii) was the second stretch-and-challenge question. Many weak candidates simply moved on to the next question, and only the strongest candidates were able to earn all of the marks by discussing the various factors which limit the amplitude and frequency of the af signal which the system can transmit. It was important in this question that each aspect was fully supported by a reason or a calculation, rather than every possible aspect being mentioned.

4 This question about an analogue-to-digital converter circuit was largely synoptic, testing the candidate's understanding of work done on the AS course. Part (a) should have been straightforward, but many weak candidates chose the wrong formula from the data sheet to calculate the frequency. The counter timing diagram of part (b) was only done completely correctly by the strongest candidates, with many candidates confusing the order of the outputs, triggering the counter on a rising edge or changing each output on the rising edge of the previous one. In part (c) only a minority of candidates wrote down the correct answer, with as many again forgetting to use the number of steps instead of the number of levels. , Part (d) proved to be just as hard. To obtain full marks candidates needed to use the same labels for inputs, outputs and clock as were used in the circuit at the start of the question. Part (e) discriminated well, with strong candidates taking care to explain what was happening at component level by reference to signals at the labels provided in the circuit diagram. However, only a minority of strong candidates were able to completely explain the frequency limits on the signal which was being sampled.

5 This question about frequency modulation proved to contain a mixture of easy and challenging tasks for candidates. It was disappointing to find in part (a)(i) that only a minority of candidates could write down a completely correct definition of frequency modulation – too many chose to use amplitude rather than voltage as the signal being coded by the frequency of the carrier. Although most candidates were able to successfully design a voltage divider for part (ii), only about half knew how to place the capacitor; the most popular incorrect siting was at the output, probably because it was the only terminal left with nothing connected to it. A number of weak candidates missed out part (b), although strong candidates had little difficulty in earning all of the marks. In drawing their voltage-time graph, many candidates forgot that the output was a logic signal.

6 This question was about asynchronous transmission of packets between computers along a single cable. Although most candidates could correctly complete the truth table of part (a) for the analogue switch, many found it very difficult to explain its inclusion in the system. Few candidates explained that two outputs connected together by a cable will not be able to maintain their signals, so a means of only allowing one output to be connected at a time is vital. In part (iii), many candidates assumed a synchronous system, with a master signal to allow each computer a time slot for placing data on the cable. Only a minority of strong candidates were able to correctly describe the protocols for asynchronous transmission of packets. Many understood erroneously that the start bit of a packet would make all the other computers

disconnect themselves from the cable, with the stop bit letting them know that they could connect again. The labelling of the start and stop bits of part (b) proved to be more challenging than expected, with many candidates not indicating their answer with enough precision to earn the mark. As always, only strong candidates are able to correctly explain the function of the stop bit. Both sections of part (c) provided excellent discrimination. Weak candidates discovered that dividing the two numbers provided returned an answer which looked similar to the one they needed to get, so failed to earn any marks for part (i). However, strong candidates were more selective in the information used to calculate their answer, and easily earned both marks. It was similar in part (ii).

7 This question about the operation of a triangle waveform generator was the most discriminating of all, with strong candidates earning all of the marks. In part (a) candidates were required do a show-that calculation for a Schmitt trigger. To earn the marks, they had to explain each stage clearly, not just write down a series of calculations. Some candidates applied the inverting amplifier gain formula to obtain their answer, others just found combinations of numbers which returned the correct value. Neither approach earned marks. Part (b) was even more challenging, facing candidates with a two-stage calculation and very little scaffolding. It didn't bother strong candidates, but weak candidates often chose to move on to part (c) where they were slightly more successful. Strong candidates tended to explain the changes in the state of each signal as time progressed. Weak candidates often lost marks by discussing the square and triangle waveforms separately without making clear the relationship between the two. Candidates who simply described the waveforms and their phase relationship with no explanation could only earn half of the marks.

F616 Design Build and Investigate Electronic Circuits

As with the AS coursework of this year, the raw marking of F616 was very well done Again, this may well be that centres have adjusted to the demands of the new coursework criteria.

As with every year, there was a great deal of variety in the circuits attempted by candidates, some of which were very ambitious indeed. Again, it must be stressed that the coursework module is a process and that the complexity of the circuit does not guarantee high marks; moreover, it is the quality of the written report which determines the final mark. It is always refreshing, though, to see the more challenging type of circuit attempted.

Even though the marking of the reports was very good this year, there are some points which have arisen from the moderation process. The following are the main points which moderators have highlighted.

Specifications (criterion 1b) were sometimes vague and vital information was missing. Some subsystems were not specified at all.

Whilst test plans (criterion 1c) are reinforced at AS level, candidates sometimes give this scant regard at this level, or just present results with no mention of a proposed test plan. It is vital that the testing of all subsystems and the final circuit is given serious consideration.

For the description of circuit behaviour (criterion 2b) high marks can only be awarded if the operation has been considered at component level.

Fault-finding (criterion 2e) is sometimes not mentioned in a candidate's report so if no mention is found, no marks can be awarded for this criterion.

For the testing of subsystems and the final circuit (criterion 3a), high marks can only be awarded if the testing has been *rigorous.* It has been noted that the final circuit can be poorly tested by some candidates.

The presentation of results (criterion 3b) should be in table or graph form and must be actual results, that is, not simulations.

Analysis of results (criterion 3c) can be difficult but candidates should be encouraged to write good subsystem specifications and to refer back to these as part of the results analysis.

Meeting the specification (criterion 3d) does rely on a good circuit specification. If this is poor, full marks for this section cannot be given.

When marking the quality of the circuit diagrams (criterion 4a), a correct circuit diagram should be looked for – some incorrect circuits were presented by candidates which clearly would not have worked as planned.

When microcontrollers are used in the circuit (and this is strongly encouraged), the program should be split into sections, like subsystems, which can then be designed and tested as separate subsystems. This avoids the presentation of long programs and the problems that this can cause candidates.

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