OCR
RECOGNISING ACHIEVEMENT

ADVANCED GCE

ELECTRONICS

F614

Control Systems

Candidates answer on the question paper.

OCR supplied materials:
None

Other materials required:
- Scientific calculator

Wednesday 8 June 2011
Morning

Duration: 1 hour 40 minutes

Candidate forename		Candidate surname	

Centre number						Candidate number				

INSTRUCTIONS TO CANDIDATES

- Write your name, centre number and candidate number in the boxes above. Please write clearly and in capital letters.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully. Make sure you know what you have to do before starting your answer.
- Write your answer to each question in the space provided. Additional paper may be used if necessary but you must clearly show your candidate number, centre number and question number(s).
- Answer **all** the questions.
- Do **not** write in the bar codes.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **110**.
- You will be awarded marks for the quality of your written communication where this is indicated in the question.
- You are advised to show all the steps in any calculations.
- This document consists of **16** pages. Any blank pages are indicated.

A calculator may be used for this paper

Turn over

Microcontroller instructions

The microcontroller contains eight general purpose registers Sn, where to n = 0, 1, 2 ... 7.
The microcontroller has an eight bit input port, I, an eight bit output port, Q, and an analogue input, ADC.

In the table of assembler instructions given below, Sd is the destination register and Ss the source register.

assembler	function
MOVI Sd,n	Copy the byte n into register Sd
MOV Sd,Ss	Copy the byte from Ss to Sd
ADD Sd,Ss	Add the byte in Ss to the byte in Sd and store the result in Sd
SUB Sd,Ss	Subtract the byte in Ss from the byte in Sd and store the result in Sd
AND Sd,Ss	Logical AND the byte in Ss with the byte in Sd and store the result in Sd
EOR Sd,Ss	Logical EOR the byte in Ss with the byte in Sd and store the result in Sd
INC Sd	Add 1 to Sd
DEC Sd	Subtract 1 from Sd
IN Sd,I	Copy the byte at the input port into Sd
OUT Q,Ss	Copy the byte in Ss to the output port
JP e	Jump to label e
JZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC, SHL or SHR was zero
JNZ e	Jump to label e if the result of the last ADD, SUB, AND, EOR, INC, DEC SHL or SHR was not zero
RCALL s	Push the program counter onto the stack to store the return address and then jump to label s
RET	Pop the program counter from the stack to return to the place the subroutine was called from
SHL Sd	Shift the byte in Sd one bit left putting a 0 into the lsb
SHR Sd	Shift the byte in Sd one bit right putting a 0 into the msb

There are three subroutines provided:
- readtable – copies the byte in the lookup table pointed at by S7 into S0. The lookup table is labelled table: When S7=0 the first byte from the table is returned in S0
- wait1ms – waits 1ms before returning
- readadc – returns a byte in S0 proportional to the voltage at ADC

Datasheet

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
voltage gain	$G = \frac{V_{out}}{V_{in}}$
open-loop op-amp	$V_{\text{out}} = A(V_+ - V_-)$
non-inverting amplifier gain	$G = 1 + \frac{R_f}{R_{\text{d}}}$
inverting amplifier gain	$G = -\frac{R_f}{R_{in}}$
summing amplifier	$-\frac{V_{out}}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} \ldots$
break frequency	$f_0 = \frac{1}{2\pi RC}$
Boolean Algebra	$A.\overline{A} = 0$ $A + \overline{A} = 1$ $A.(B + C) = A.B + A.C$ $\overline{A.B} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}.\overline{B}$ $A + A.B = A$ $A.B. + \overline{A}.C = A.B + \overline{A}.C + B.C$
amplifier gain	$G = -g_{\text{m}}R_{\text{d}}$
ramp generator	$\Delta V_{out} = -V_{in}\frac{\Delta t}{RC}$

Answer **all** questions.

1 Fig. 1.1 shows a memory cell.

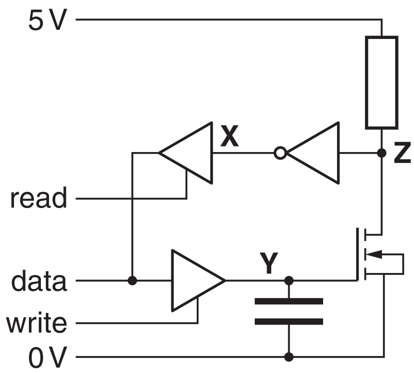
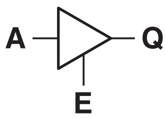


Fig. 1.1

(a) The memory cell uses tri-states. Complete the truth table for one of the tri-states.



A	**E**	**Q**
0	*0*	*High impedance*

[4]

(b) State why a tri-state is used in Fig. 1.1 to connect **X** to the data-bus.

.... **[1]**

(c) Explain how the components in the memory cell can be used to store a 1. Your answer should include the sequence of signals at read, data and write.

....

....

....

.... **[5]**

(d) Explain how the components in Fig. 1.1 allow the 1 to be read at a later time.

....

....

....

.... **[3]**

[Total: 13]

2 Fig. 2.1 shows an op-amp circuit to control the brightness of a bulb.

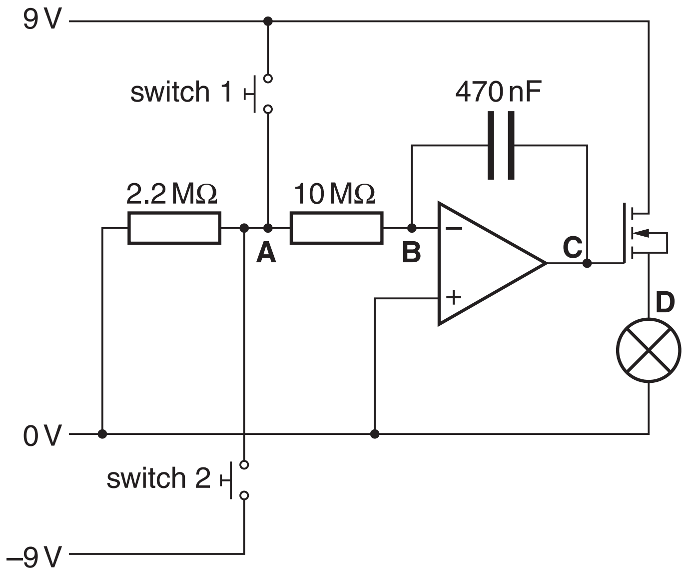


Fig. 2.1

(a) Put a ring around the type of op-amp circuit in Fig. 2.1.

difference amplifier **non-inverting amplifier** **ramp generator** **voltage follower**

[1]

(b) Explain how the circuit works by filling in the gaps using the words below. Each word or phrase can be used once, more than once or not at all.

constant	**immediately negative**	**increasing**
decreasing	**immediately positive**	**zero**

When the circuit is first turned on, the voltage at **C** is 0V.

When switch 2 is pressed the voltage at **A** is .... which means that the

voltage at **C** is .... and the brightness of the lamp is ....

Then no switches are pressed. The voltage at **A** is .... and the voltage at

B is .... which means that the voltage at **C** is ....

[6]

(c) Sometime after the start the voltage at **C** is 5V.
Switch 1 is then pressed for 2s. Calculate the voltage at **C**.

Voltage = ... V **[4]**

[Total: 11]

3 Fig. 3.1 shows the block diagram of a switched mode power supply.

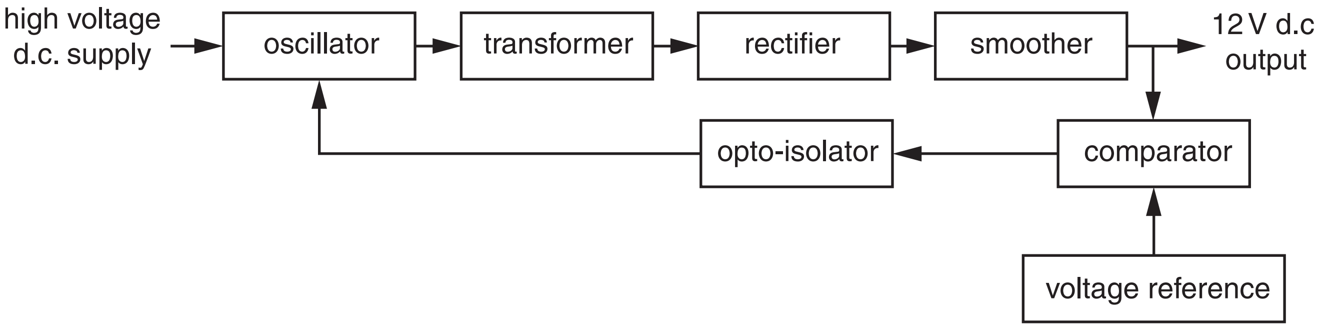


Fig. 3.1

(a) The system in Fig. 3.1 is a closed-loop control system.
State how the block diagram shows this.

....

.... **[1]**

(b) Explain the advantage of using closed-loop systems over open-loop systems.

....

....

.... **[2]**

(c) Complete Fig. 3.2 by drawing the circuit diagram of the rectifier and smoother part of the switched-mode power supply.

[3]

Fig. 3.2

(d) By stating the two components in an opto-isolator explain how it works.

....

....

....

.... **[4]**

(e) Explain why the opto-isolator is used in the switched mode power supply.

....

....

.... **[3]**

(f) Fig. 3.3 shows the voltage reference and comparator of the switched mode power supply. The output of the comparator saturates at +12 V and 0 V.

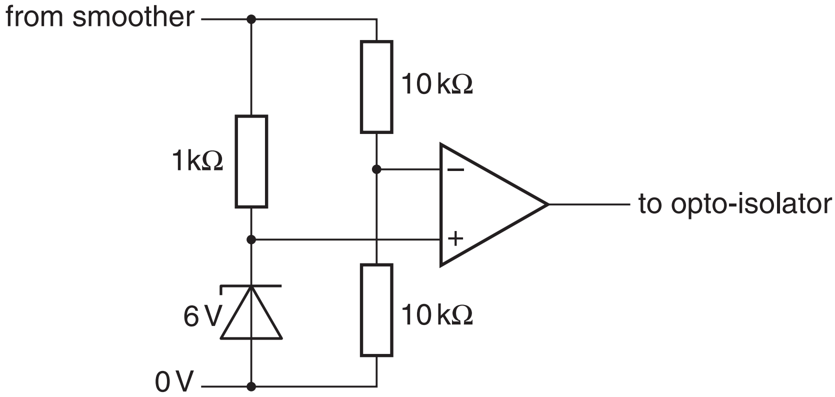
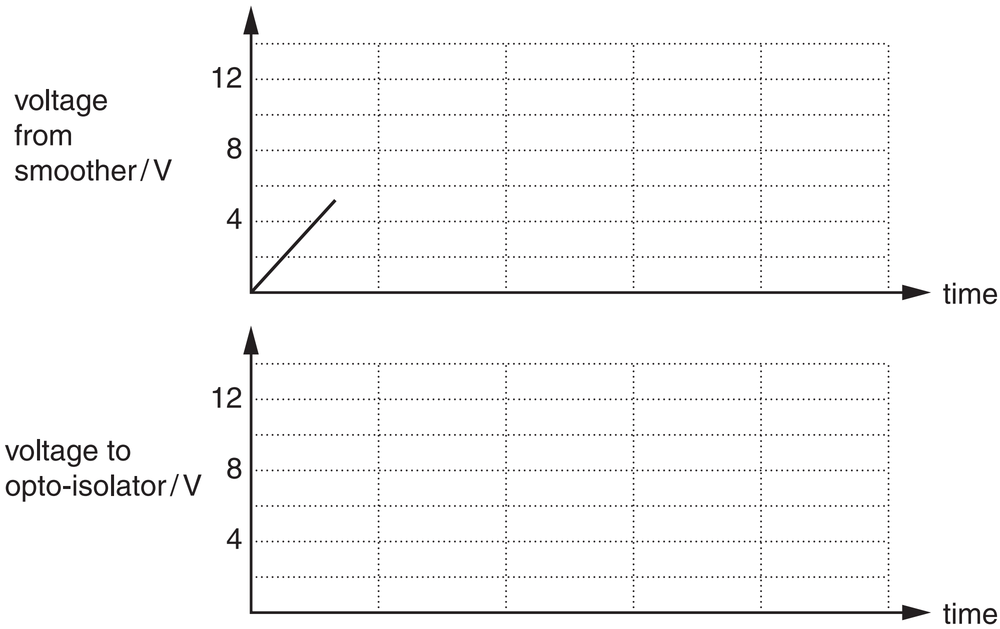


Fig. 3.3

Complete the graphs below to show how the voltage from the smoother and the voltage from the comparator vary with time after the power supply is turned on.



[6]

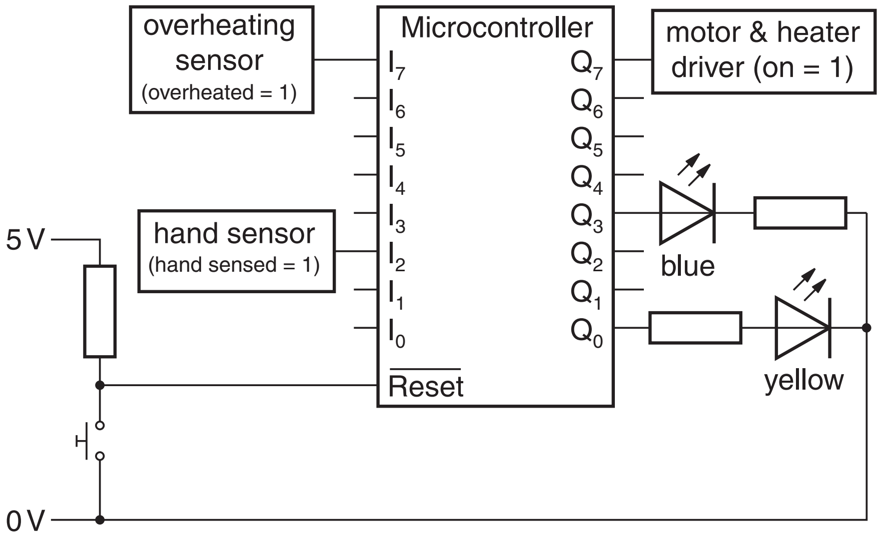
(g) Suggest why a 12 V zener diode was not used in the comparator and voltage reference circuit.

....

.... **[2]**

[Total: 21]

4 Fig. 4.1 shows the circuit and main program for controlling an electric hand drier.




```
start:  MOVI   S0,08
        OUT    Q,S0
loop:   MOVI   S0,04
        IN     S1,I
        AND    S1,S0
        JZ     start
        RCALL  check
        RCALL  dry
        JP     loop
```

Fig. 4.1

(a) Use the first two lines of the main program to explain how the hand drier shows that it is ready to operate when it is first turned on.

....

....

.... **[3]**

(b) The subroutine ‘dry’ turns on the motor & heater driver and the blue LED. Write the code for the subroutine dry. Use the microcontroller instructions on page 2.

dry: ....

....

.... **[4]**

(c) The first two lines of the subroutine ‘check’ tests if the system has overheated. Complete the subroutine below.

```
check:  MOVI   S0,   ........
        IN     S1,   I
        AND    S0,   S1

        ........  ................
        RCALL fault
skip:   RET
```

[3]

(d) Explain how the subroutine 'fault' works and describe what it does to the outputs.

```
fault:   MOVI   S4, 00
         MOVI   S5, 01
stop:    OUT    Q,  S4      ..........................................
         EOR    S4, S5      ..........................................
         MOVI   S7, 64      ..........................................
repeat:  RCALL  wait1ms     ..........................................
         DEC    S7          ..........................................
         JNZ    repeat      ..........................................
         JP     stop        ..........................................
```

Description of the effect on the outputs: ....

....

.... **[9]**

(e) The program for controlling the hand drier uses subroutines.

(i) State two advantages of using subroutines when writing programs.

....

....

.... **[2]**

(ii) Describe what happens to the program counter and the stack pointer when the microcontroller executes the RET function/returns from a subroutine.

....

....

....

.... **[3]**

(f) State and explain what happens to the output devices of Fig. 4.1 when the switch is pressed and released.

....

....

....

.... **[3]**

[Total: 27]

5 Fig. 5.1 shows the circuit for an amplifier built by a teacher.

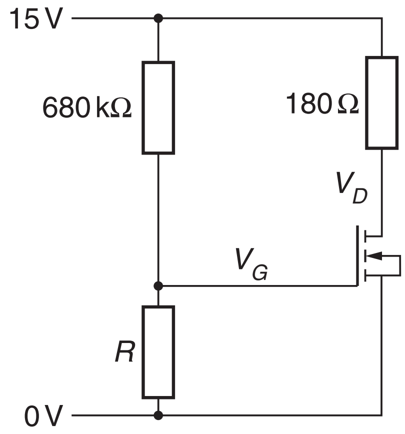


Fig. 5.1

(a) Draw on Fig. 5.1 to show how two capacitors can be added to the circuit to connect a.c. input and output circuits. Label the input and the output. **[4]**

(b) Calculate the value of the resistor R to make the voltage $V_G = 3\text{V}$.

R = ...kΩ **[3]**

(c) The graph in Fig. 5.2 shows I_{DS} against V_{GS} for the MOSFET in Fig. 5.1.

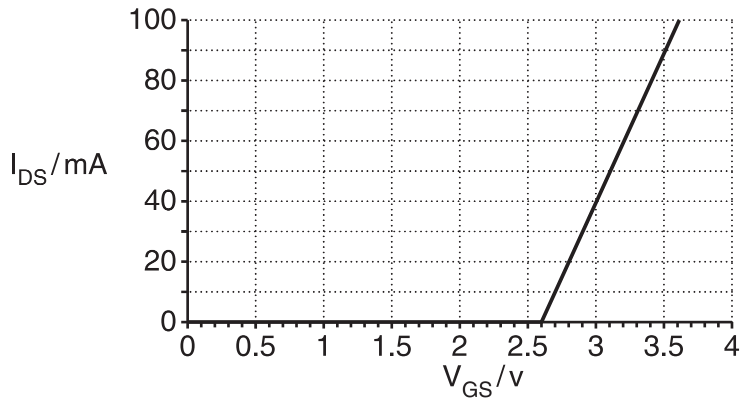


Fig. 5.2

Use information from the graph in Fig. 5.2 to show that the voltage V_D is about half the supply voltage.

....

....

.... **[3]**

(d) Suggest why the circuit has been designed to have V_D at this value.

....

....

.... **[2]**

(e) Use the graph in Fig. 5.2 to find the threshold voltage of the MOSFET.

MOSFET threshold voltage = ... V **[1]**

(f) Use the graph to calculate the gain of the amplifier.

gain = ... **[4]**

(g) A student accurately builds a copy of the teacher's circuit in Fig. 5.1 using new components. The circuit does not work well as an amplifier. When the student tests their circuit they find that $V_D = 1\,V$. Suggest why the student's circuit is not operating in the same way as the teacher's circuit.

....

....

.... **[3]**

(h) Draw a MOSFET amplifier design that could be copied and would still work well. You do not need to show component values.

[2]

[Total: 22]

6 Fig. 6.1 shows an 8 × 2 bit memory module.

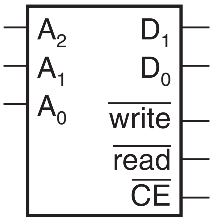


Fig. 6.1

(a) State the number of memory cells there are in this 8 × 2 bit memory module.

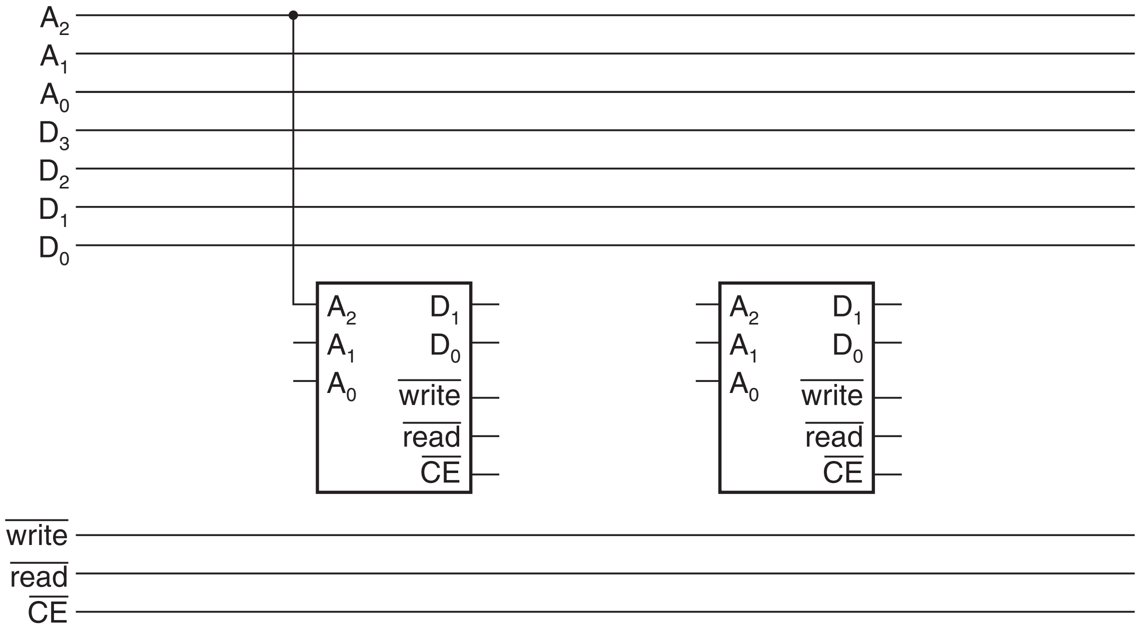
.... **[1]**

(b) Explain why an 8 × 2 bit memory module has three address lines (A_0, A_1 and A_2) and two data lines (D_0 and D_1).

....

.... **[2]**

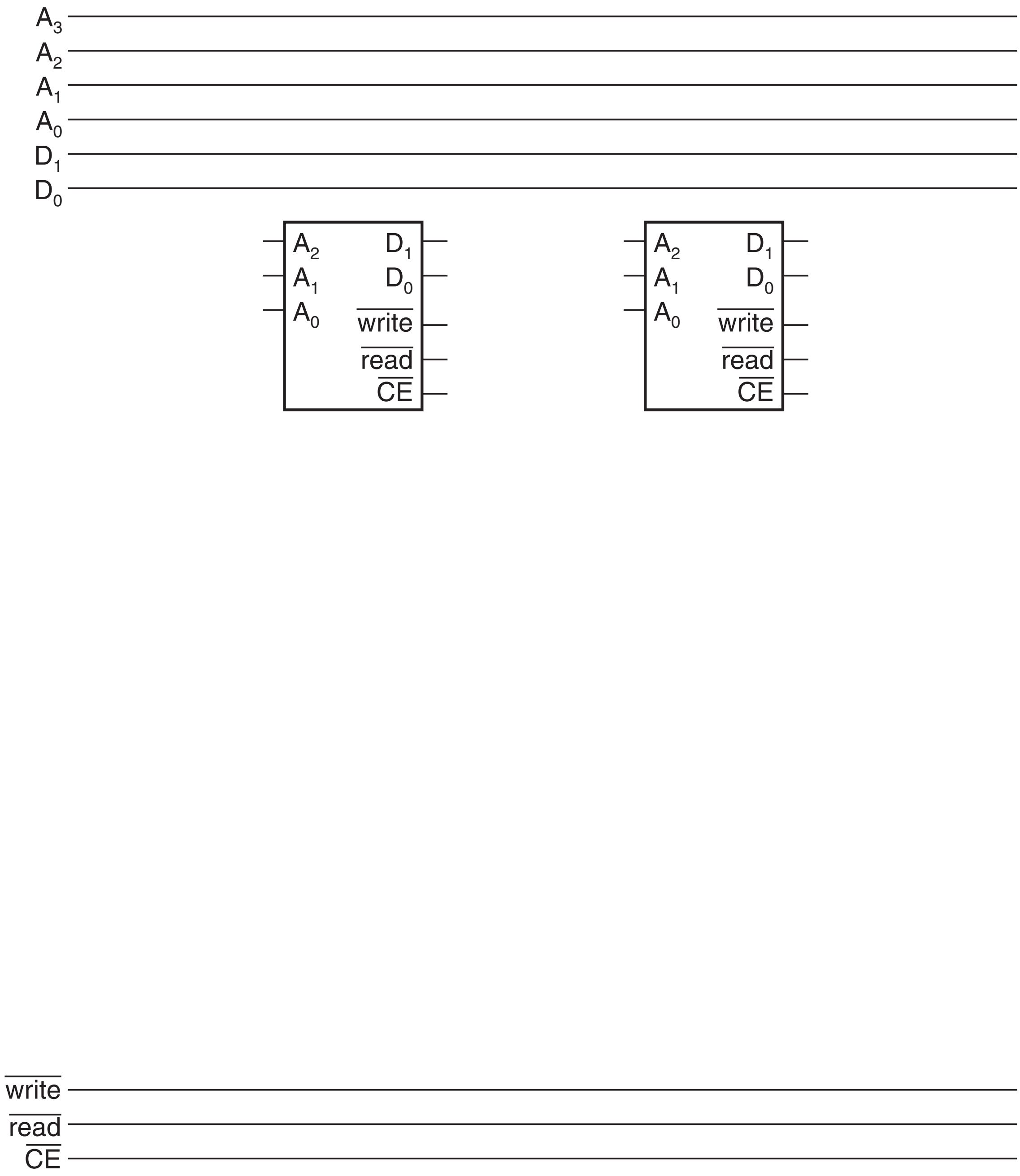
(c) Complete the diagram in Fig. 6.2 to show how two of these 8 × 2 memory modules can be combined to make a 8 × 4 bit memory.



[4]

Fig. 6.2

(d) Complete the diagram in Fig. 6.3 to show how two of these 8 × 2 memory modules can be combined to make a 16 × 2 bit memory.



[6]

Fig. 6.3

[Total: 13]

Quality of Written Communication [3]

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