THIS IS A NEW SPECIFICATION

OCR
RECOGNISING ACHIEVEMENT

ADVANCED GCE

ELECTRONICS

Unit F611: Simple Systems

F611

Candidates answer on the question paper

OCR Supplied Materials:
None

Other Materials Required:
- Scientific calculator

Monday 18 May 2009
Morning

Duration: 1 hour 30 minutes

Candidate Forename		Candidate Surname	

Centre Number						Candidate Number				

INSTRUCTIONS TO CANDIDATES

- Write your name clearly in capital letters, your Centre Number and Candidate Number in the boxes above.
- Use black ink. Pencil may be used for graphs and diagrams only.
- Read each question carefully and make sure that you know what you have to do before starting your answer.
- Answer **all** the questions.
- Do **not** write in the bar codes.
- Write your answer to each question in the space provided, however additional paper may be used if necessary.

INFORMATION FOR CANDIDATES

- The number of marks is given in brackets **[ ]** at the end of each question or part question.
- The total number of marks for this paper is **90**.
- You will be awarded marks for the quality of written communication where this is indicated in the question.
- Unless otherwise indicated, you can assume that:
  - op-amps are run off supply rails at +15V and –15V
  - logic circuits are run off supply rails at +5V and 0V
- You are advised to show all the steps in any calculations.
- This document consists of **16** pages. Any blank pages are indicated.

A calculator may be used for this paper

SPA (SHW 00175 2/08) T65358/6

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Data Sheet

Unless otherwise indicated, you can assume that:

- op-amps are run off supply rails at +15V and –15V
- logic circuits are run off supply rails at +5V and 0V.

resistance	$R = \frac{V}{I}$
power	$P = VI$
series resistors	$R = R_1 + R_2$
time constant	$\tau = RC$
monostable pulse time	$T = 0.7RC$
relaxation oscillator period	$T = 0.5RC$
frequency	$f = \frac{1}{T}$
Boolean Algebra	$A.\overline{A} = 0$
	$A + \overline{A} = 1$
	$A.(B + C) = A.B + A.C$
	$\overline{A.B} = \overline{A} + \overline{B}$
	$\overline{A + B} = \overline{A}.\overline{B}$
	$A + A.B = A$
	$A.B = \overline{A}.C = A.B + \overline{A}.C + B.C$

Answer **all** the questions.

1 Fig. 1.1 shows a logic system.

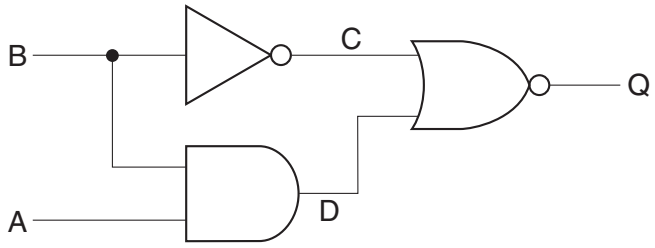


Fig. 1.1

(a) Complete this truth table for the logic system.

B	A	C	D	Q
0	0			
0	1			
1	0			
1	1			

[3]

(b) Use the truth table to write down a Boolean expression for Q in terms of B and A.

Q = ... **[1]**

(c) Show in the space below how a logic system made from only NAND gates can replace the circuit of Fig. 1.1.

[2]

(d) Use Boolean algebra or a truth table to justify your NAND gate circuit.

[2]

[Total: 8]

2 The circuit of Fig. 2.1 is part of a sensor circuit.

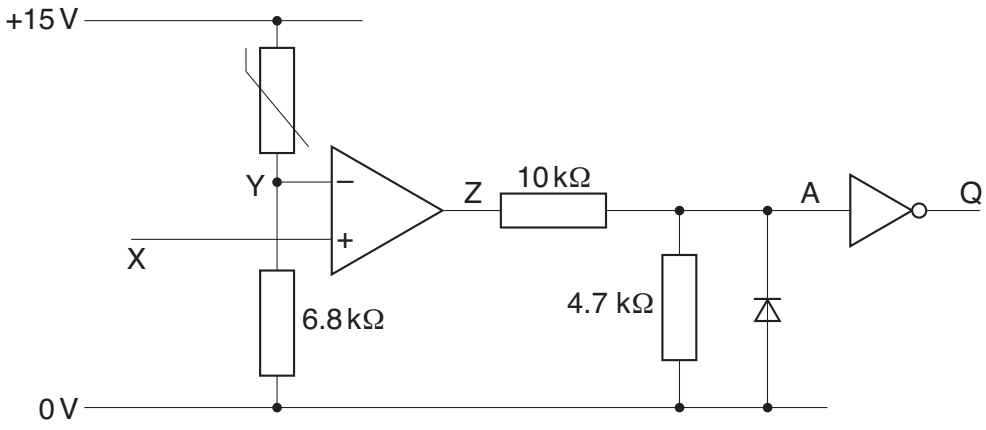


Fig. 2.1

(a) The circuit contains a thermistor.

(i) Put a circle around the thermistor. **[1]**

(ii) Describe the electrical properties of a thermistor.

.....

.....

..... **[2]**

(b) A potentiometer is missing from the circuit of Fig. 2.1.

It allows the voltage at X to be varied from 0 V to +15 V.

(i) On Fig. 2.1, show how the potentiometer should be connected. **[2]**

(ii) Explain what happens to the voltage at Z when the voltage at X is slowly increased from 0 V to +15 V.

.....

.....

.....

.....

.....

..... **[3]**

(iii) On Fig. 2.1, show how a voltmeter should be connected to measure the voltage at Z. **[1]**

(c) The network of two resistors and a diode between the output of the op-amp and the NOT gate converts the signal at Z into logic 1 or logic 0.

(i) Explain why the diode can be ignored when Z is at +13V.

.....

.....

..... **[2]**

(ii) Calculate the voltage at A when Z is at +13V.

voltage = ... V **[3]**

(iii) State the voltage at A when Z is at –13V. Give a reason for your answer.

.....

.....

.....

..... **[3]**

(iv) Use your answers to **(ii)** and **(iii)** to comment on the idea that this network provides logic 1 or logic 0 at A.

.....

.....

..... **[2]**

[Total: 19]

3 The circuit of Fig. 3.1 uses a relaxation oscillator to make a sound.

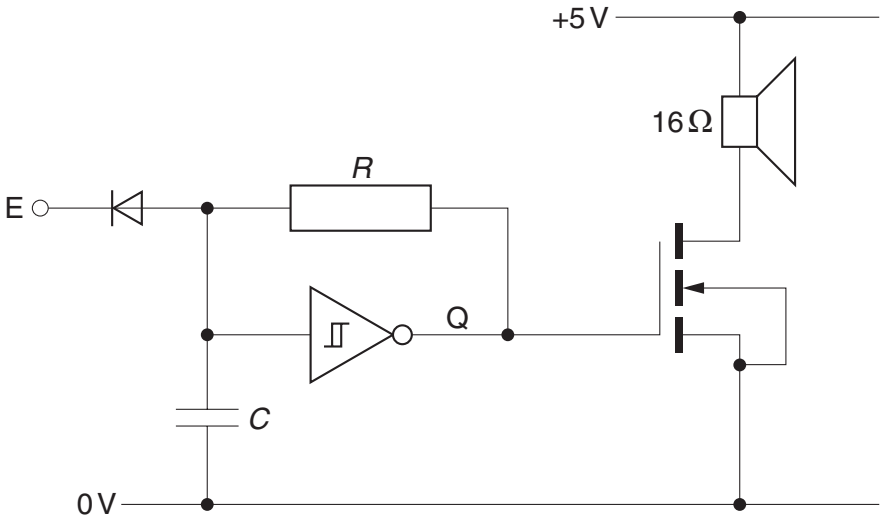


Fig. 3.1

(a) (i) Suggest values of resistor *R* and capacitor *C* which will make the period *T* of the oscillator 200 μs.

R = ...

C = ... **[3]**

(ii) Calculate the frequency of the oscillator.

frequency = ... kHz **[2]**

(b) A double-beam oscilloscope is connected to the circuit to monitor the signals at the input and output of the Schmitt trigger NOT gate. The screen of the double-beam oscilloscope is shown in Fig. 3.2.

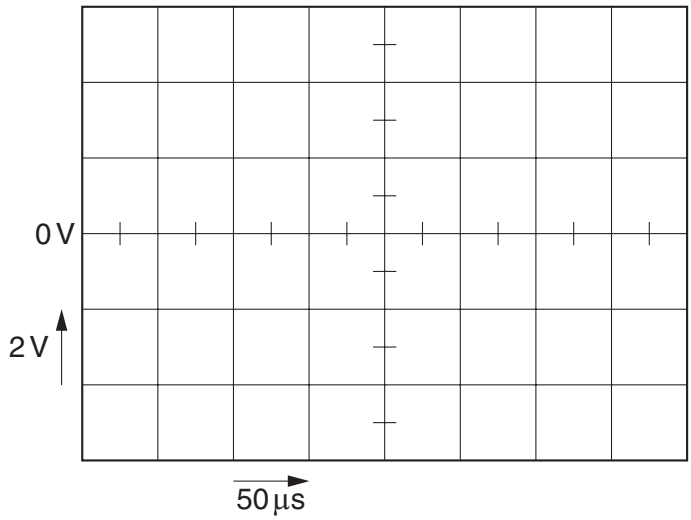


Fig. 3.2

(i) The timebase is set to 50 μs per division.

The vertical amplifier is set to 2 V per division with 0 V at the centre of the screen.

Draw on Fig. 3.2 to show the signal at the **output** of the NOT gate. **[3]**

(ii) The screen of Fig. 3.2 also shows the signal at the input of the NOT gate.

The trip points of the Schmitt trigger NOT gate are +2.0 V and +3.0 V.

Draw on Fig. 3.2 to show the signal at the **input** of the NOT gate. **[3]**

(iii) Show on Fig. 3.1 how the oscilloscope should be connected to monitor just the signal at the **input**. **[2]**

(c) The circuit of Fig. 3.1 contains a MOSFET.

(i) Why is the MOSFET necessary?

.....

..... **[1]**

(ii) On Fig. 3.1, label the gate, drain and source of the MOSFET. **[1]**

(iii) Describe how the drain-source resistance of the MOSFET depends on the gate-source voltage.

.....

.....

..... **[2]**

(d) Calculate the **average** power of the loudspeaker in Fig. 3.1.

average power = ... W **[3]**

[Total: 20]

4 The circuit of Fig. 4.1 contains a single logic gate.

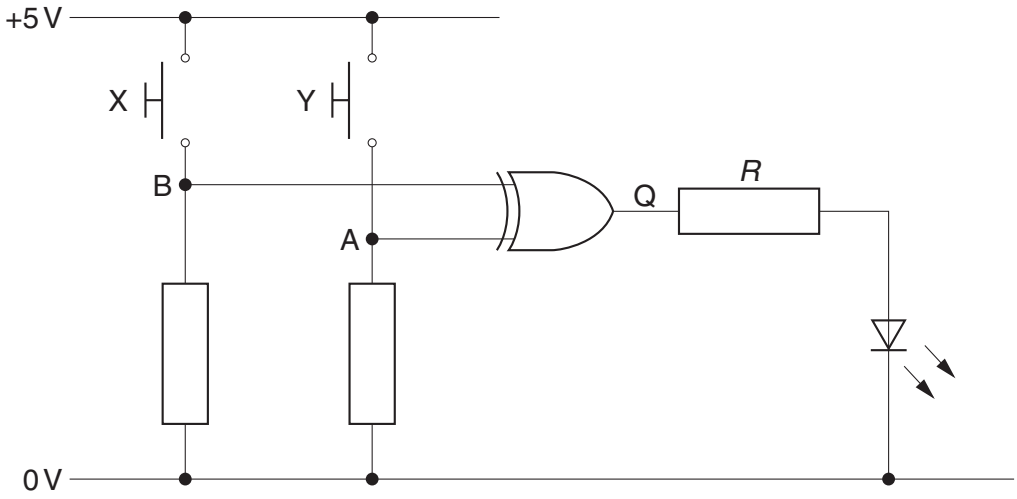


Fig. 4.1

(a) Fig. 4.1 is an incomplete block diagram for the circuit of Fig. 4.1.

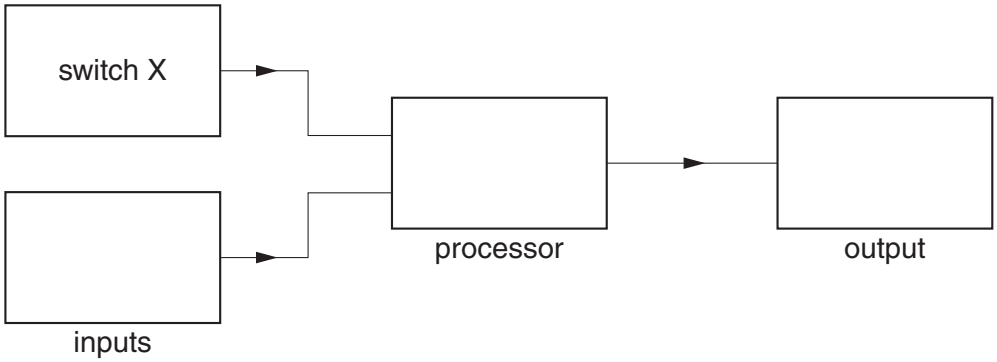


Fig. 4.2

(i) Complete the block diagram of Fig. 4.2. **[3]**

(ii) What do the arrows on a block diagram show?

.....

..... **[1]**

(b) (i) Complete the truth table for the circuit of Fig. 4.1.

switch X	switch Y	B	A	Q	state of LED
open	open	0	0	0	off

[4]

(ii) Describe the behaviour of the circuit.

.....

.....

.....

..... **[2]**

(c) The LED is connected to the logic gate by a resistor.

(i) Explain why the resistor is necessary.

.....

.....

..... **[2]**

(ii) The voltage drop across the LED is 1.7 V when its power is 5.0 mW.

Show that the current in the LED is about 3 mA.

[1]

(iii) Calculate a suitable value for the resistor *R*.

R = ... Ω **[2]**

(d) Fig. 4.1 is a circuit diagram. Suggest why the supply rail connections to the logic gate have not been shown.

.....

..... **[1]**

[Total: 16]

5 Here is the truth table for a logic system. It has inputs C, B and A, and outputs P and Q.

C	B	A	P	Q
0	0	0	1	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

(a) (i) Write down a Boolean expression for **Q** in terms of C, B and A.

[3]

(ii) Use Boolean algebra to show that $Q = \overline{C}.\overline{A} + B.\overline{A}$.

[3]

(iii) Show in the space below how the circuit for Q can be assembled from NOT, AND and OR gates.

[3]

(b) A Boolean expression for P is $P = \overline{C} + B$.

(i) Show in the space below how the circuit for P can be assembled from **two** NAND gates.

[2]

(ii) Use Boolean algebra to justify your arrangement of NAND gates.

[2]

(iii) Explain the advantages of assembling a logic system using only NAND gates.

.....

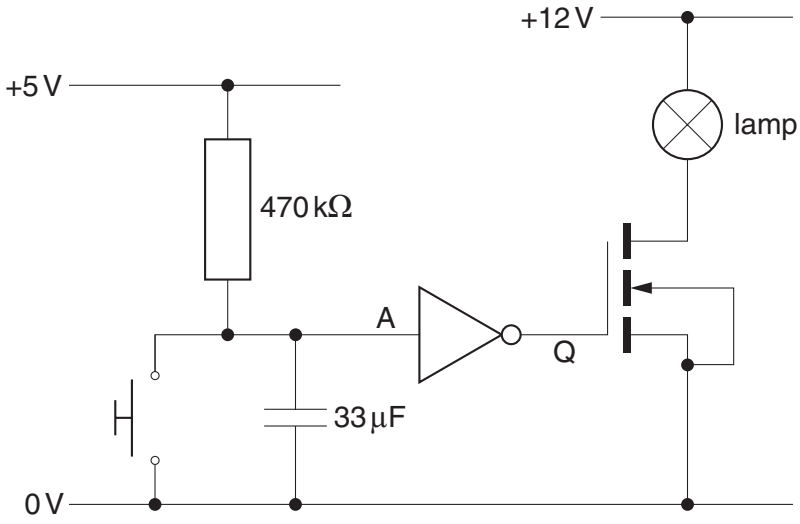
.....

..... **[2]**

[Total: 15]

6 The circuit of Fig. 6.1 contains an RC network.

The table shows the behaviour of the logic gate.



signal at A	signal at Q
< 2.5 V	+5 V
> 2.5 V	0 V

Fig. 6.1

(a) Calculate the time constant of the RC network.

time constant = ... s **[2]**

(b) Explain why the lamp comes on as soon as the switch is pressed.

.....

.....

.....

..... **[3]**

(c) Explain, in detail, what happens to the lamp when the switch is released.

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.....

.....

..... **[4]**

Quality of Written Communication **[3]**

[Total: 12]

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