Teacher Resource Bank

GCE Electronics

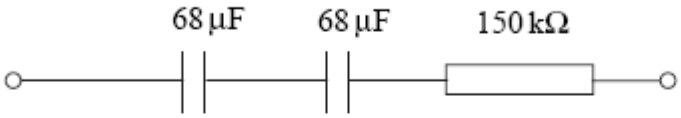
Exemplar Examination Questions

- ELEC2 Further Electronics

ELEC2 – Further Electronics

Capacitors in Series and Time Constant (ELE1, Q3, 2007)

3 The RC circuit shown below is used in a simple timer.



(a) Calculate

(i) the combined capacitance of the two capacitors in this circuit,

.....

.....

(ii) the time constant of this circuit.

.....

(4 marks)

(b) The timer switches when the capacitors are discharged to half the power supply voltage.
Neglecting any current taken by the timing circuit and assuming the capacitors are initially fully charged. Calculate

(i) how long it will take for the capacitors to discharge to half the power supply voltage,

.....

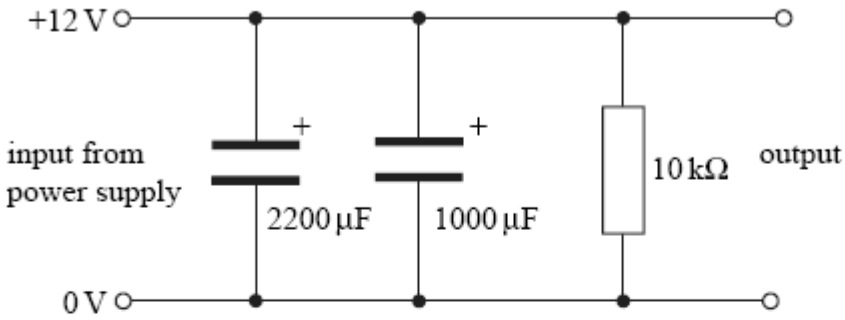
(ii) approximately how long it will take for the capacitors to totally discharge.

.....

(3 marks)

Capacitors in Parallel and Time Constant (ELE1, Q3, 2006)

3 Two capacitors are connected in parallel to smooth the output of a power supply. A resistor is connected across the capacitors to discharge them when the power supply is switched off.



(a) Calculate

(i) the current through the resistor when the power supply is on,

.....

(ii) the combined capacitance of the two capacitors,

.....

(iii) the time constant of this circuit, assuming there is no load connected to the output.

.....

.....

(5 marks)

(b) When the power supply is switched off, the capacitors will start to discharge. Assume no load is connected to the power supply output.

(i) How long will it take for the capacitors to discharge to 6 V?

.....

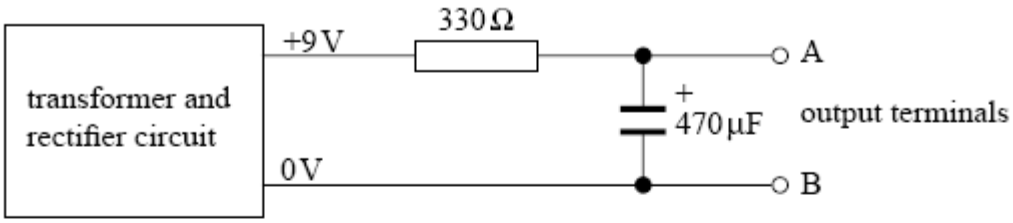
(ii) How long will it take for the capacitors to effectively totally discharge?

.....

(5 marks)

Time Constant (ELE1, Q2, 2008)

2 The output stage of a power supply is shown below.



2 (a) (i) Calculate the current through the resistor when the output terminals are connected together.

.....

2 (a) (ii) Calculate the power dissipation of the resistor at this current.

.....

(4 marks)

2 (b) (i) Calculate the time constant of this circuit, assuming no load is connected to its output.

.....

2 (b) (ii) The 9 V supply is switched on and the capacitor is initially uncharged. Approximately how long will it take for the output voltage to reach 9 V?

.....

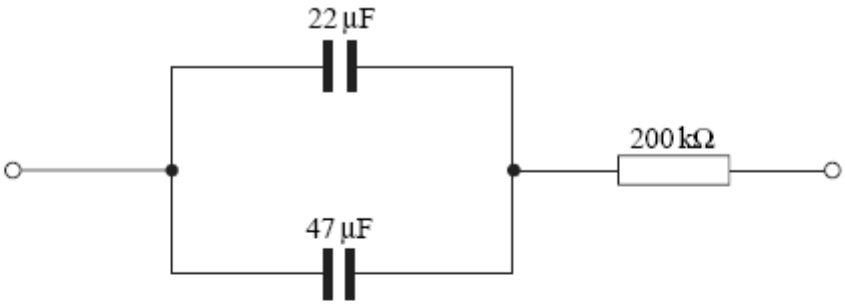
2 (b) (iii) A load resistance of 10 kΩ is connected between the output terminals. Calculate the approximate time taken for the output voltage to reach 0 V after the 9 V supply is switched off.

.....

(6 marks)

Time Constant and Capacitors in Parallel (ELE1, Q2, 2005)

2 The RC circuit shown below is used in a simple timer.



(a) (i) Calculate the combined capacitance of the two capacitors in the circuit.

.....

(ii) Calculate the time constant of the circuit.

.....

(3 marks)

(b) Both capacitors are initially uncharged. When connected to a power supply, calculate:

(i) the time for the capacitors to charge to half the power supply voltage;

.....

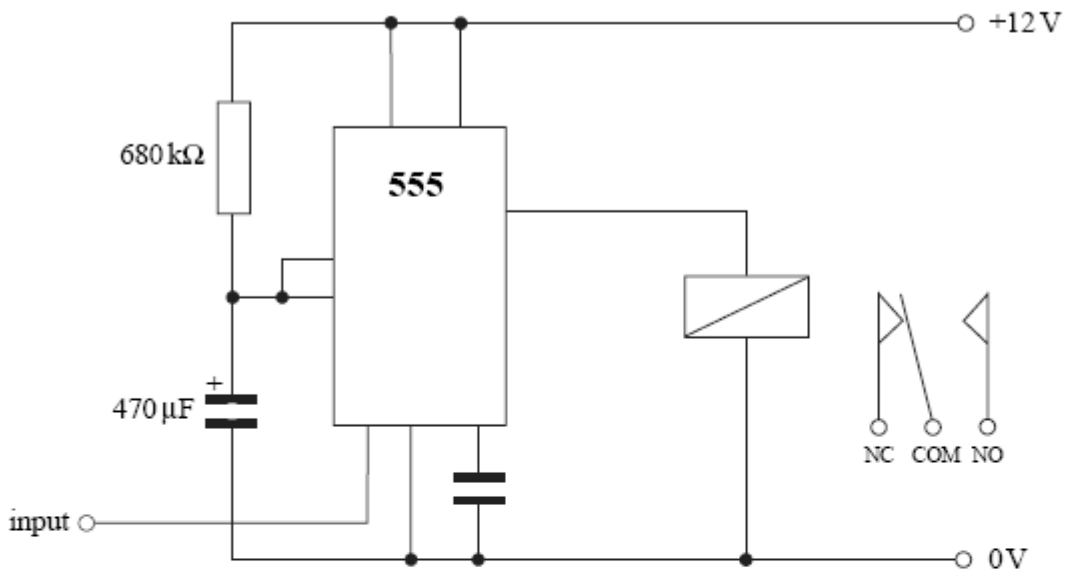
(ii) the time for the capacitors to become fully charged.

.....

(4 marks)

555 Monostable and Relay (ELE1, Q7, 2005 – ELE1, Q6, 2006)

7 A 555 monostable circuit is used to control an electromagnetic relay.



(a) Using the equation from the data sheet, calculate the time period of the monostable circuit.

.....

(2 marks)

(b) How should the input change to set the monostable into its unstable state?

.....

(1 mark)

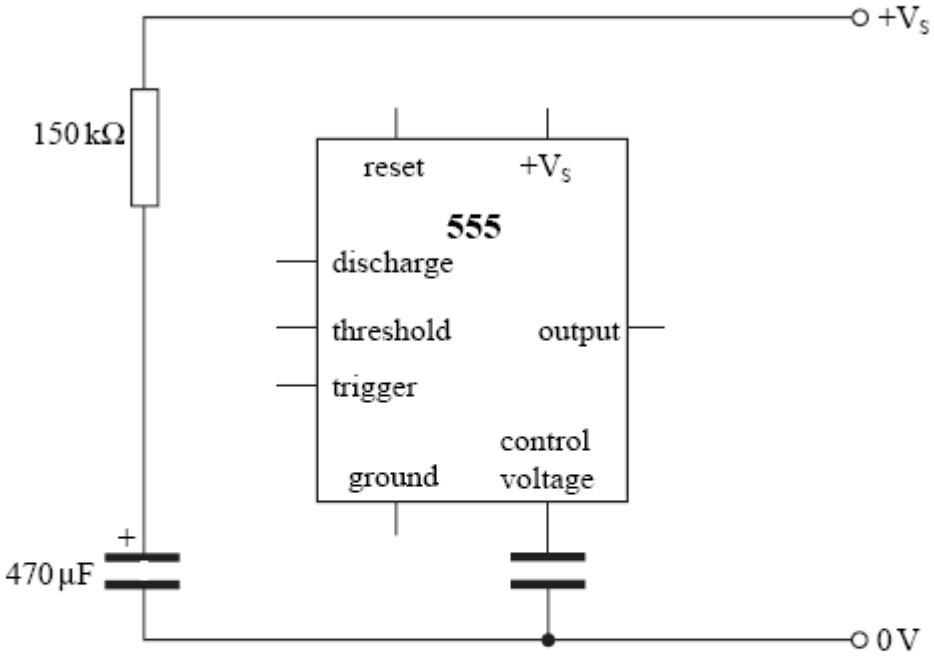
(c) Which contact on the relay would be connected to the common terminal (COM) when the monostable output is high?

.....

(1 mark)

6 A 555 monostable circuit is used to control the time for which a lamp is on.

(a) Complete the circuit diagram below to show how the 555 timer IC is connected as a monostable. Label the input to this circuit.



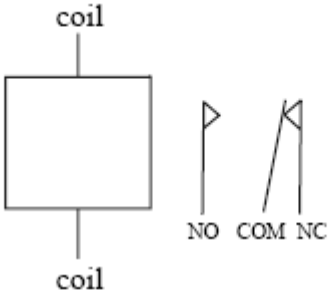
(6 marks)

(b) Calculate the time period of the output pulse from the monostable.

.....

(2 marks)

(c) The current drawn by the lamp is too high for it to be connected directly to the 555 IC output.
The electromagnetic relay shown below is used.



The coil is powered when the monostable output goes high.
Which **two** connections would be used to switch on the lamp?

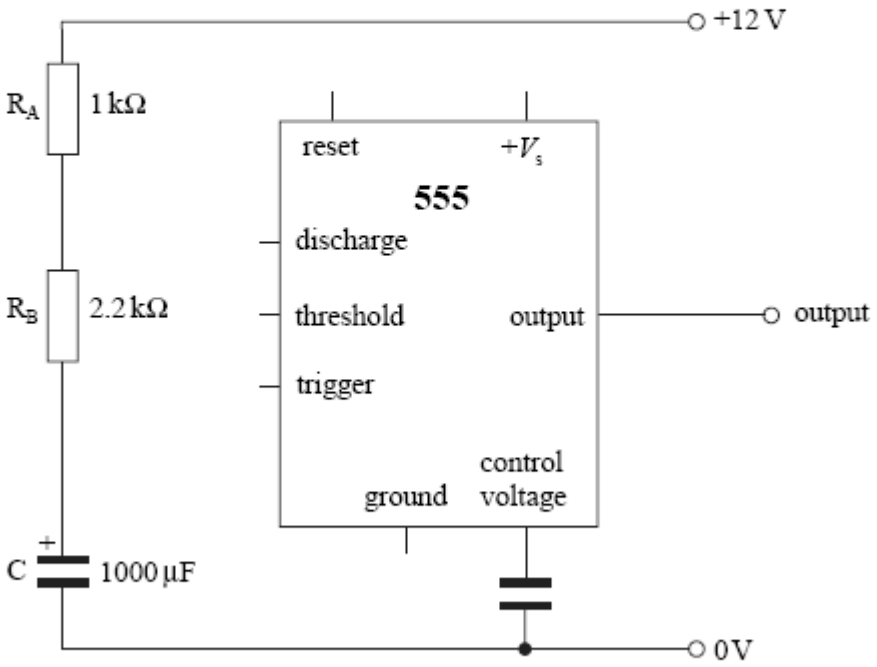
..... and .....

(2 marks)

555 Astable (ELE1, Q4, 2005 – ELE1, Q5, 2007)

4 A 555 timer IC is used in a circuit to generate control pulses for an industrial process.

(a) Complete the circuit diagram below to show how the timer IC is connected as an astable.



(6 marks)

(b) Calculate:

(i) using the equation from the data sheet, the time that the output is low (t_L);

.....

.....

(ii) using the equation from the data sheet, the time that the output is high (t_H).

.....

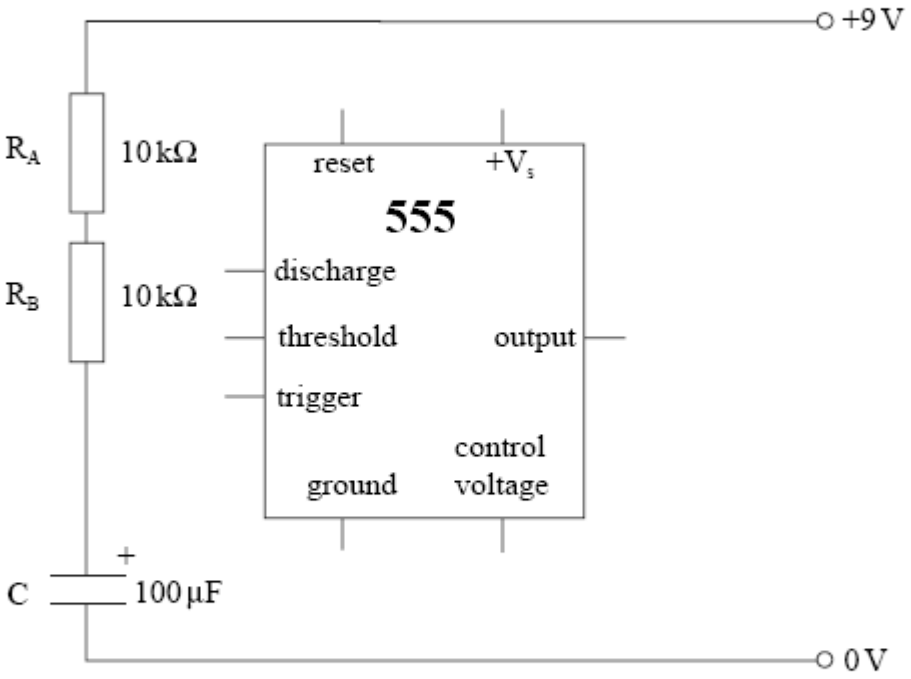
.....

(4 marks)

5 A 555 timer IC is connected as an astable.

(a) (i) Complete the circuit diagram below to show how the 555 timer IC is connected as an astable.

(ii) Draw an LED and series resistor connected to the output so that the LED lights when the output is high.



(6 marks)

(b) (i) Calculate the time for which the LED will be on.

.....

.....

(ii) Calculate the time for which the LED will be off.

.....

.....

(iii) Calculate the frequency of the output pulses.

.....

.....

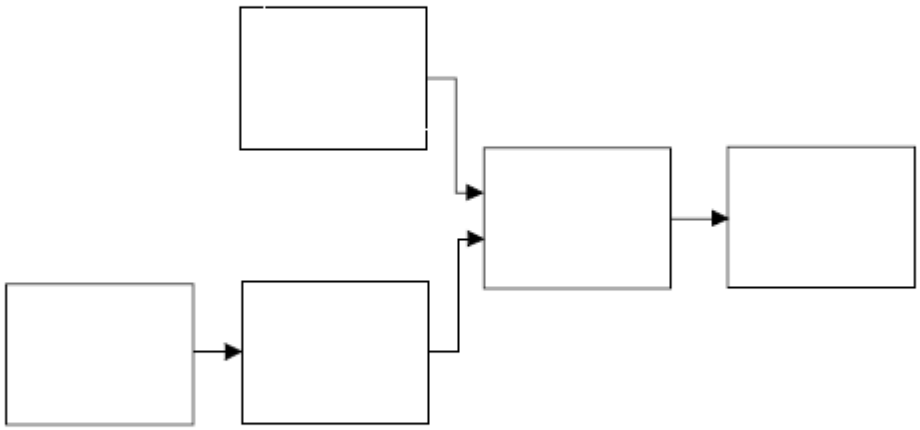
(6 marks)

Comparator and 555 Astable (ELE1, Q5, 2008)

5 A student designs a noise warning system to alert the user to the presence of a noise level likely to damage hearing. An LED flashes on and off when the noise level exceeds a safe value.

5 (a) Label each subsystem in the system diagram below to show a possible design for the noise warning system using the following subsystems:

NOR gate **astable** **comparator** **LED** **sound sensor**



(5 marks)

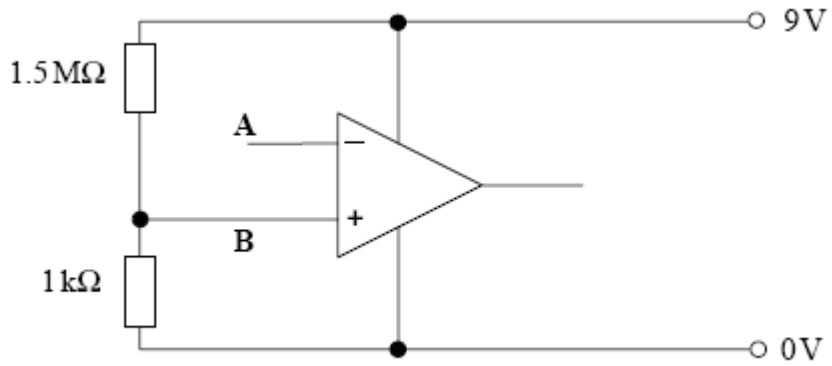
5 (b) In which subsystem could

5 (b) (i) an op-amp be used.....

5 (b) (ii) a 555 IC be used?.....

(2 marks)

5 (c) The comparator circuit diagram is shown below.



5 (c) (i) Calculate the voltage at point **B** in this circuit

.....

.....

The signal from the sound sensor is connected to point **A** in the comparator circuit. What voltage would you expect from the output of this circuit when

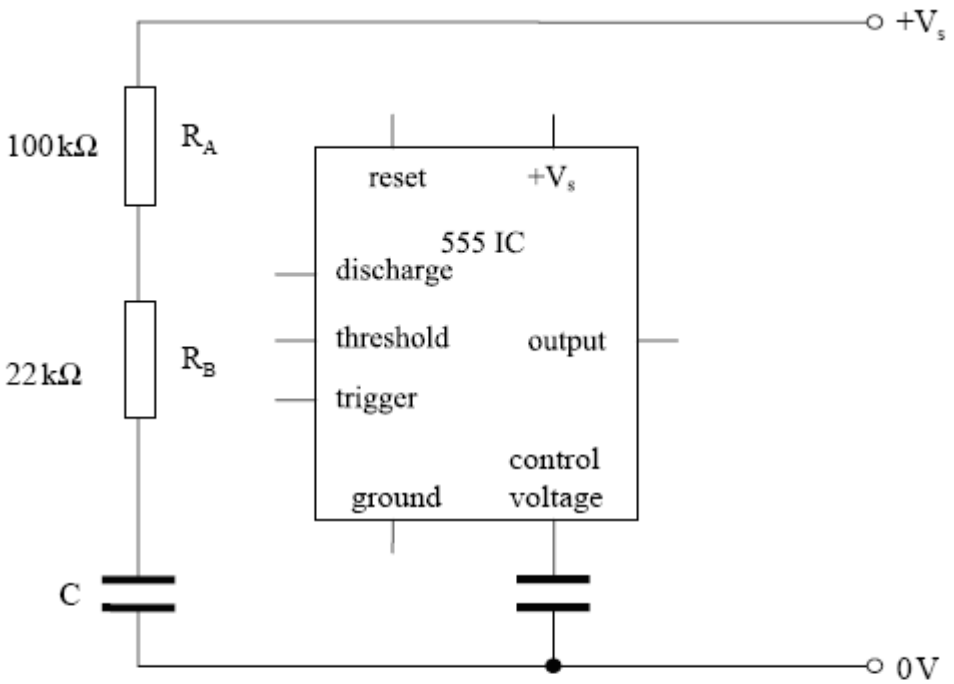
5 (c) (ii) the voltage at **A** is 4 mV .....

5 (c) (iii) the voltage at **A** rises to 10 mV? .....

(4 marks)

5 (d) Part of the astable circuit diagram is shown below.

5 (d) (i) Complete the circuit by drawing in the wire links required.



5 (d) (ii) Given the values shown on the circuit diagram for R_A and R_B, calculate the value of C required to give an output frequency of 2 Hz.

.....

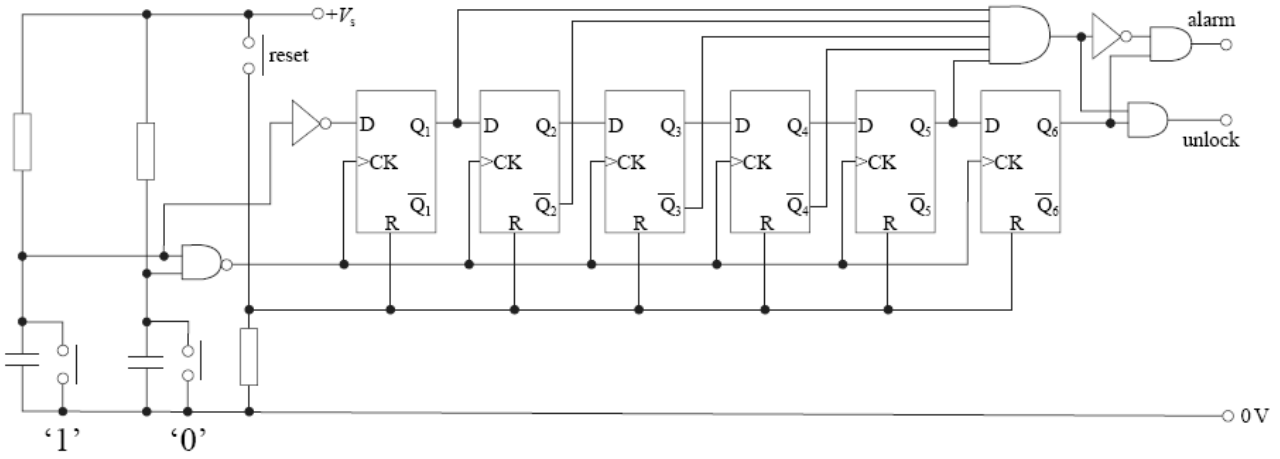
.....

.....

(7 marks)

Shift Register (ELE2, Q6, 2005 – ELE2, Q6, 2008 – ELE2, Q6, 2007)

The circuit diagram for a combination lock is shown below. It consists of a 6-bit shift register plus additional logic circuits.



To operate the lock, the circuit is first reset and then a binary number is entered by pressing the '1' and '0' switches. If an incorrect number is entered an alarm is sounded.

Use the diagram printed on **page 14** to answer Question 6.
Detach **page 14** and study the diagram before answering Question 6.

6 (a) Explain how a shift register operates.

.....

.....

.....

.....

(4 marks)

(b) Each of the input switches has an associated resistor and capacitor circuit.
Explain the function of this circuit.

.....

.....

(1 mark)

(c) Explain what will happen when the '1' input switch is pressed.

.....

.....

.....

(2 marks)

(d) State a binary number that can be entered for the system to unlock.
Explain your reasoning.

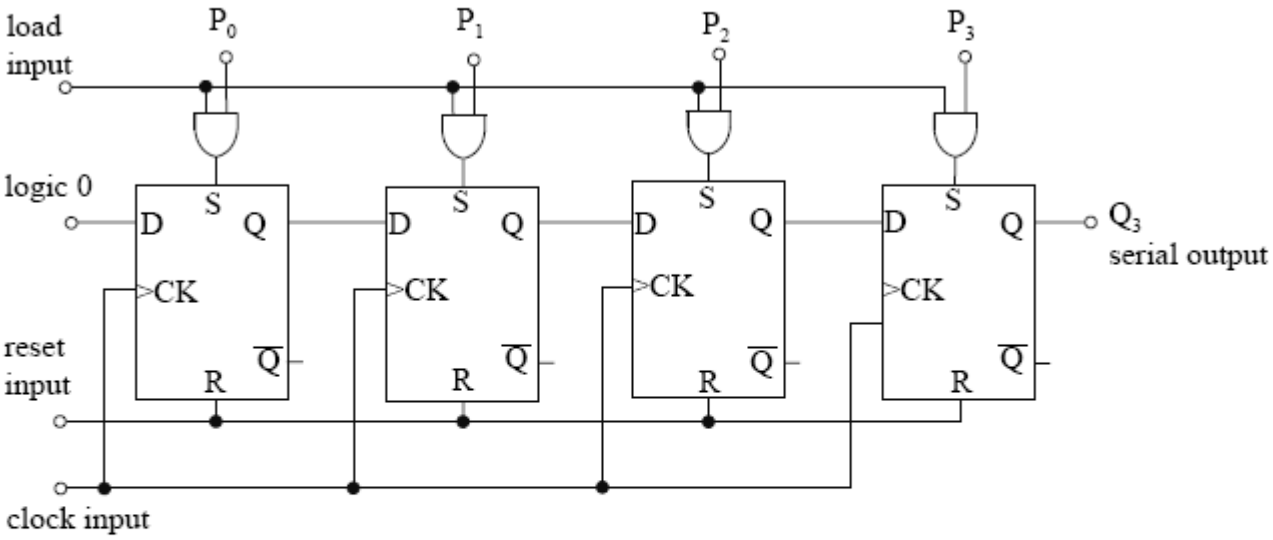
.....

.....

.....

(2 marks)

6 The shift register circuit below is used by a student to convert parallel data to serial data. The parallel data is sent to P_0, P_1, P_2 and P_3 and the serial output is taken from Q_3.



6 (a) Explain how a shift register works.

.....

.....

.....

(3 marks)

6 (b) (i) Explain why it is necessary in this circuit to reset the shift register before loading new parallel data.

.....

.....

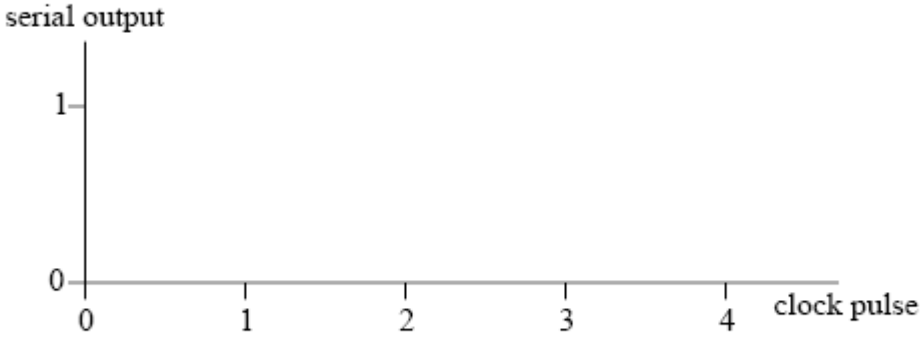
6 (b) (ii) State the logic level of the load input for parallel data to be loaded into the shift register.

.....

.....

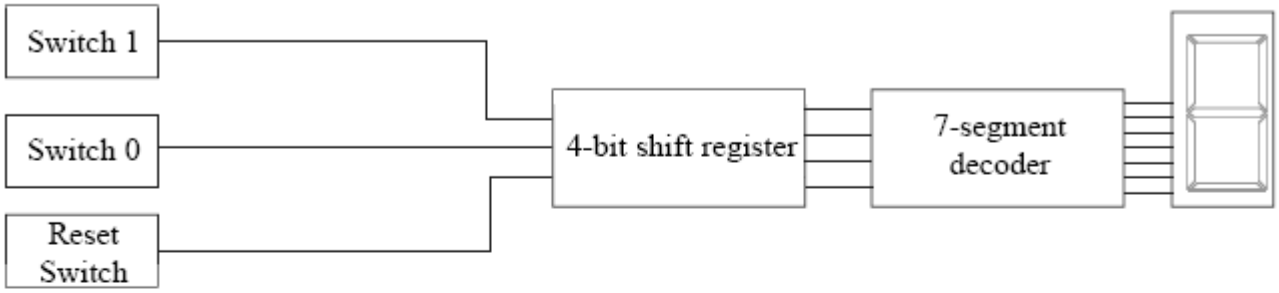
(2 marks)

6 (c) The hexadecimal number **B** is loaded into the shift register. Sketch onto the diagram below the serial output.



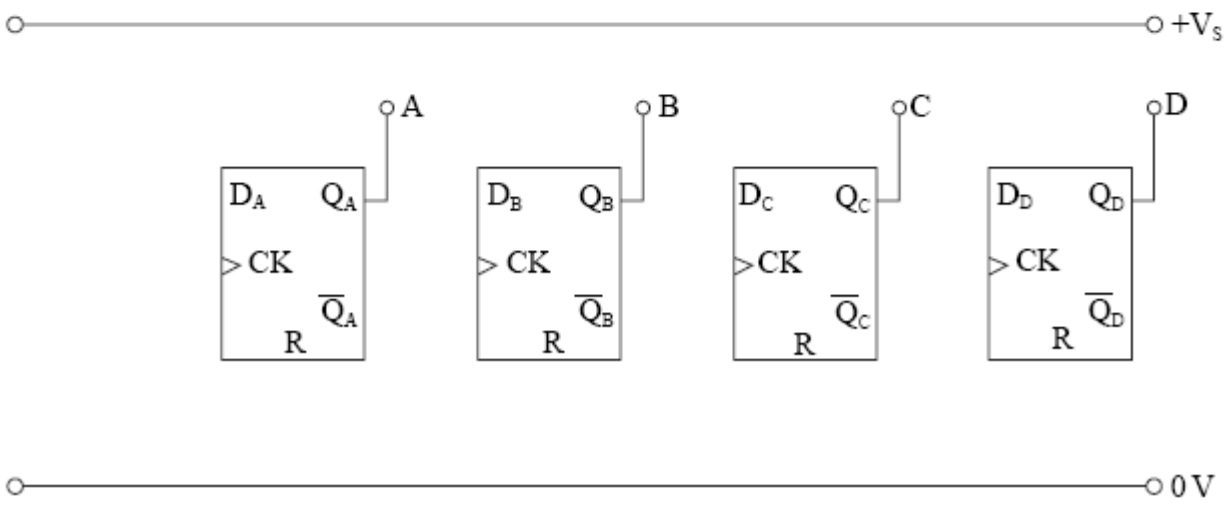
(4 marks)

6 An electronic system is required so that binary numbers can be entered and converted to a hexadecimal output on a 7-segment display. The system diagram is shown below.



When switch 1 is pressed, the serial input to the shift register is set to logic 1 and a clock pulse is generated to enter the logic 1 into the shift register.
When switch 0 is pressed, the serial input to the shift register is set to logic 0 and a clock pulse is generated to enter the logic 0 into the shift register.
When the reset switch is operated, the outputs of the shift register are set to logic 0.

(a) (i) Complete the diagram below to show how the four D-type flip-flops should be connected to form a 4-bit shift register and clearly label the serial input.



(ii) If the reset terminals of the D-type flip-flops are active high, mark onto the diagram above where you would connect the reset switch and any other components that you need.

(6 marks)

(b) The 7-segment decoder has to be especially designed to enable the display to show the hexadecimal numbers above 9. The representation of these numbers must be completely different to the representation of the numbers from 0 to 9.
Complete the table below and shade in the appropriate segments of the display to represent the hexadecimal numbers.

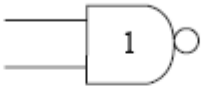
Binary	Decimal	Hexadecimal	Display
1010	10	A	
1011	11	B	
	12		
	13		
1110	14	E	
	15		

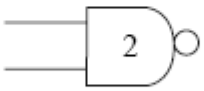
(3 marks)

NAND Gate Bistable (ELE2, Q1, 2006)

1 Latches are used in a system that determines which contestant in a quiz responds first. Each latch is constructed from two NAND gates.

(a) (i) Complete the circuit diagram below for the latch and add pull up resistors onto the two inputs.





(ii) Label the outputs **Q** and $\overline{\mathbf{Q}}$ and the corresponding inputs $\overline{\mathbf{SET}}$ and $\overline{\mathbf{RESET}}$.

(6 marks)

(b) Explain how the latch circuit functions. Assume that **Q** is initially at logic 0.

.....

.....

.....

.....

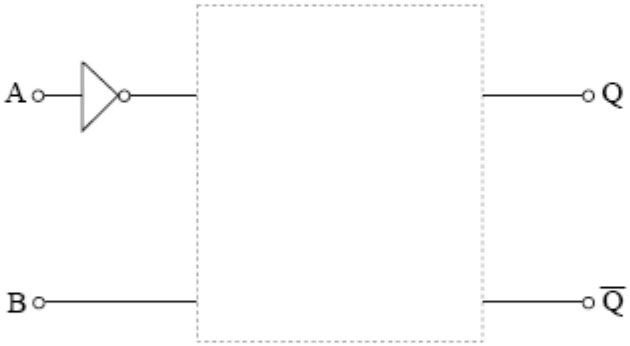
.....

(3 marks)

NAND Gate Bistable and MOSFET (ELE2, Q3, 2005)

3 The diagram below shows a drinking water trough for farm animals.

The water level is detected by sensors A and B which give a logic 0 when dry and a logic 1 when wet. They are connected to the circuit below.



(a) Complete the circuit diagram, within the dotted box, for a NAND gate bistable latch.

(2 marks)

(b) State the logic state of Q when:

(i) the water trough is empty .....

(ii) water enters the trough and sensor B becomes wet .....

(iii) water continues to enter the trough and sensor A becomes wet .....

(iv) the water level then falls and sensor A becomes dry .....

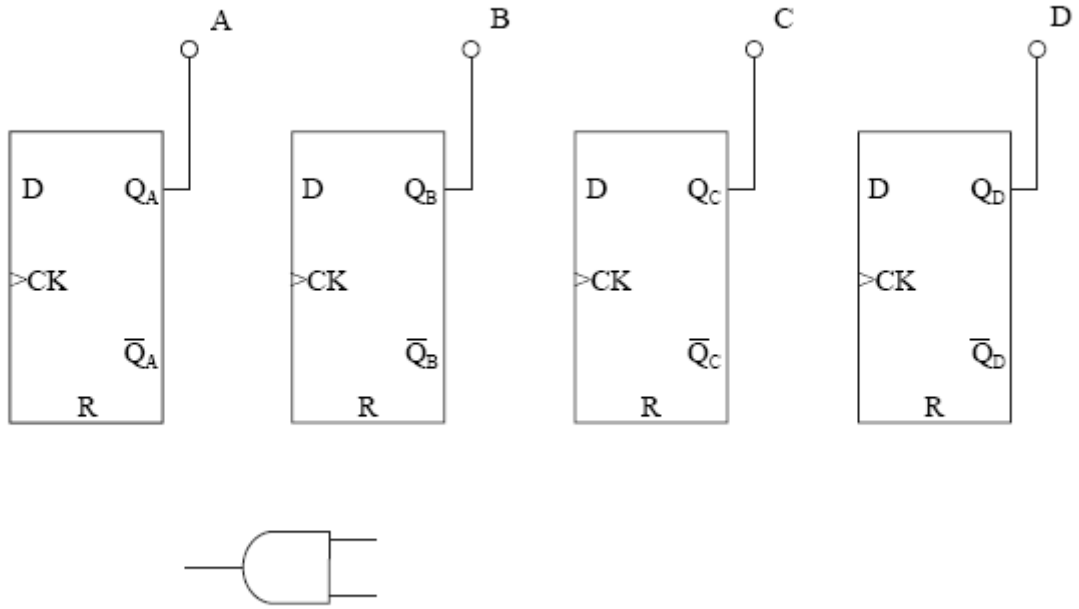
(4 marks)

(c) The whole system operates from a 12 V supply. The electric water valve contains an elecromagnet and water flows when there is more than 8 V connected across it. Draw a circuit diagram in the space below to show how an n-channel MOSFET could be used to interface the bistable latch to the water valve.

(3 marks)

Counter and Boolean (ELE2, Q5, 2005)

5 (a) Complete the circuit diagram below to show how four D-type flip-flops can be used to form a modulo 10 counter, with outputs A, B, C and D.



(4 marks)

(b) An automatic bread maker has 10 discrete processes which are listed below. The processes are controlled by the modulo 10 counter.

number	process	action
0	OFF	Add ingredients
1	Mix ingredients	Motor on
2	Warm ingredients	Heater on
3	Pause	Add yeast
4	Mix dough	Motor on
5	Warm ingredients	Heater on
6	Mix dough	Motor on
7	Warm ingredients	Heater on
8	Cook	Heater on
9	STOP	Alert that bread is cooked

Explain why the Boolean expression for the heater being on is

$$\overline{D}.\overline{C}.B.\overline{A} + \overline{D}.C.\overline{B}.A + \overline{D}.C.B.A + D.\overline{C}.\overline{B}.\overline{A}$$

.....

.....

.....

.....

(2 marks)

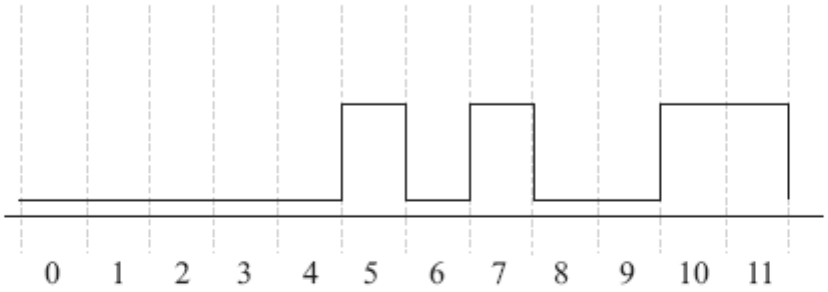
(c) Show that the expression simplifies to

$$\overline{A}.\overline{C}.(D \oplus B) + \overline{D}.C.A$$

(3 marks)

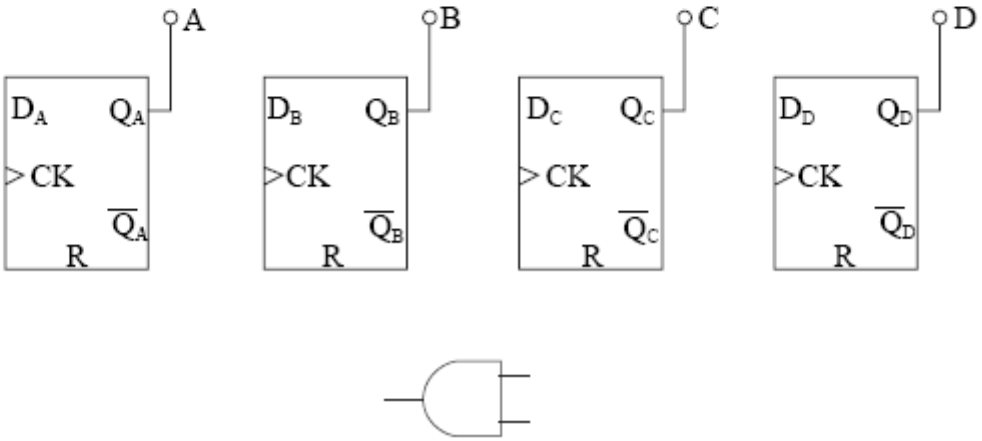
Counter (ELE2, Q1, 2007)

1 In order to test the serial interface of a computer, a small team of electronics students plan to construct a piece of test equipment that will produce the sequence of pulses shown in the diagram below.



They begin by constructing a modulo-12 counter using four D-type flip-flops.

(a) Complete the circuit diagram below to show how this could be achieved.



(4 marks)

(b) They next decide that they should show the sequence of pulses in a truth table which is shown below.

Step number	Counter Output D	Counter Output C	Counter Output B	Counter Output A	Pulse
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1

They now devise a logic gate circuit to combine the outputs of the counter to produce the required sequence of pulses. They correctly decide that the Boolean expression for the gates is:

$$\overline{D}.C.\overline{B}.A + \overline{D}.C.B.A + D.\overline{C}.B.A + D.\overline{C}.B.\overline{A}$$

(i) Explain the origin of the terms in the above expression.

.....

.....

.....

(ii) Simplify the above expression.

.....

.....

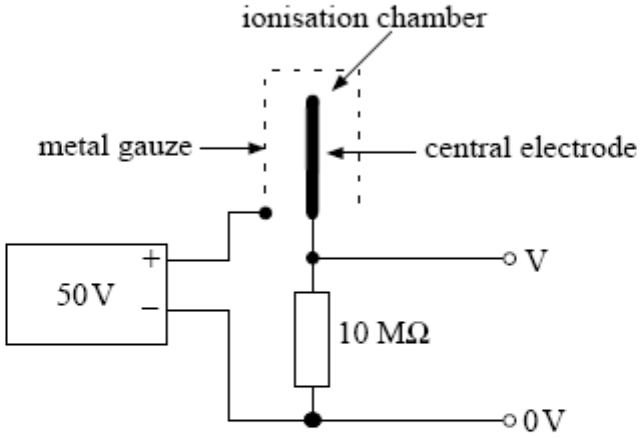
.....

.....

(5 marks)

Non-Inverting Amplifier (ELE2, Q2, 2008)

2 An ionisation chamber for detecting radioactivity consists of a metal gauze cylinder surrounding a central electrode. The metal gauze is held at a voltage of +50 V with respect to the central electrode. When radiation enters the chamber the gas is ionised and a very small current flows which is directly related to the strength of the radiation. This small current passes through a 10 MΩ resistor.



2 (a) (i) The maximum current that the detector can produce is 2×10^{-10} A. Calculate the corresponding voltage across the 10 MΩ resistor.

.....

.....

2 (a) (ii) The voltage is to be displayed on a digital meter which has a maximum sensitivity of 200 mV. Calculate the voltage gain required for an amplifier to interface the digital meter to the ionisation chamber.

.....

.....

(4 marks)

2 (b) It is decided to use a non-inverting op-amp amplifier to provide this gain. State and explain what important property makes a non-inverting amplifier a suitable choice.

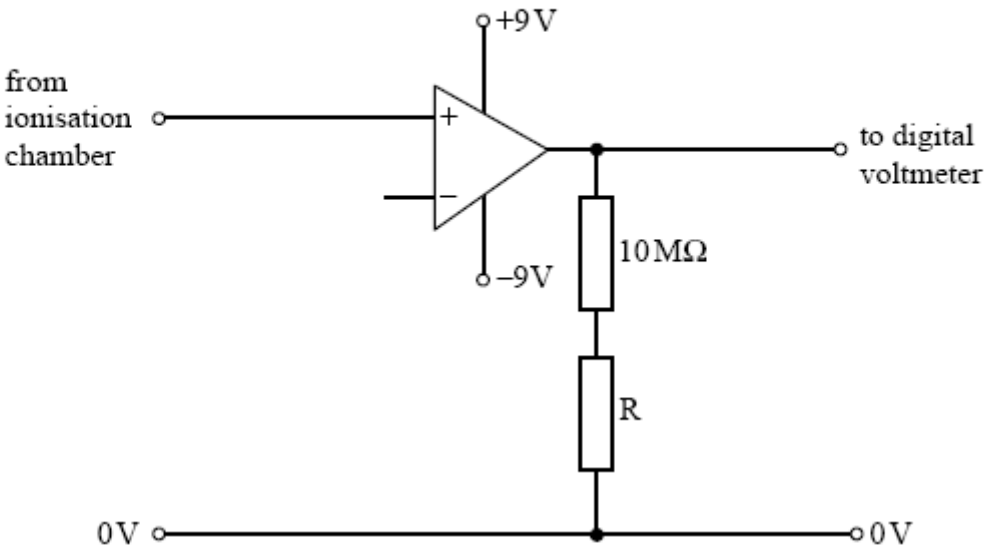
.....

.....

.....

(2 marks)

The partly drawn circuit diagram for a non-inverting amplifier is shown below.



2 (c) (i) Complete the circuit diagram by adding the missing connection.

2 (c) (ii) Calculate the value of R needed to produce the voltage gain you have calculated in part (a)(ii).

.....

.....

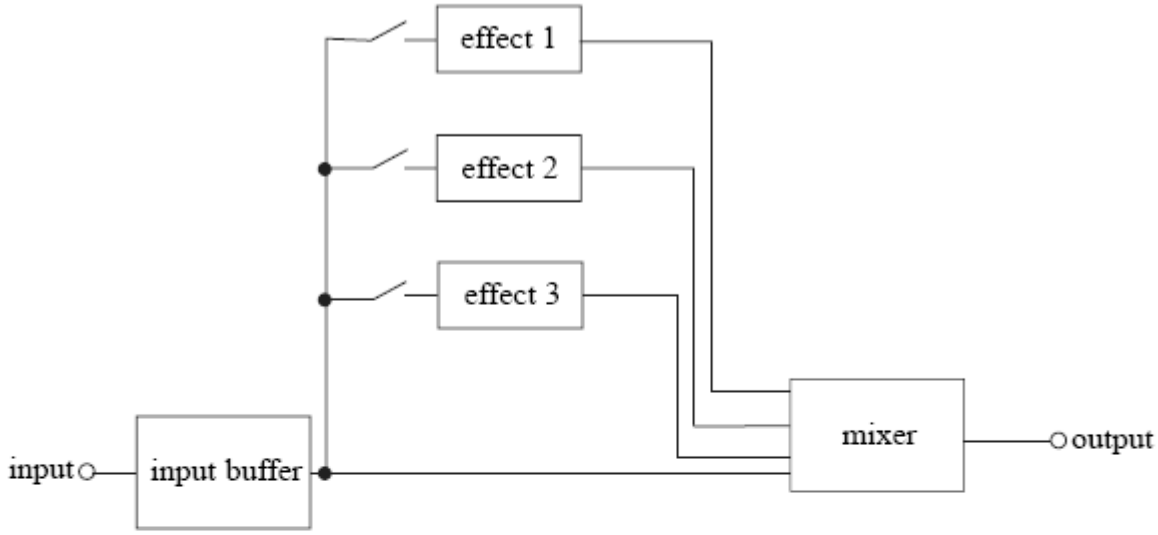
.....

.....

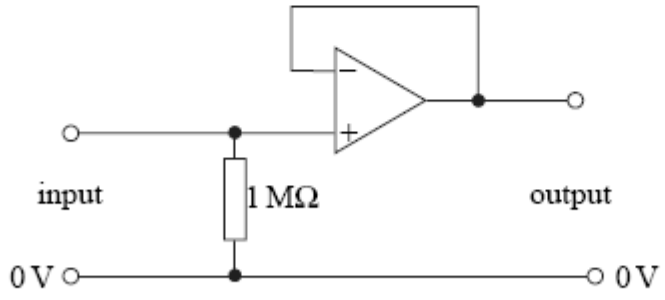
(3 marks)

Voltage Follower, Summing Amplifier, Inverting Amplifier (ELE2, Q6, 2006)

6 A system diagram for a guitar effects unit is shown below. The whole system operates from a ±12 V supply.



(a) The circuit diagram for the input buffer is shown below.



(i) State the voltage gain of this circuit.

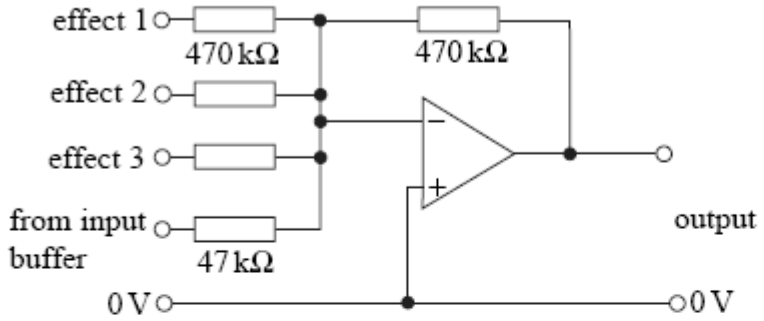
.....

(ii) State the input resistance of this circuit.

.....

(2 marks)

(b) The circuit diagram for the mixer is shown below.



(i) What voltage gain does the mixer circuit give to effect 1?

.....

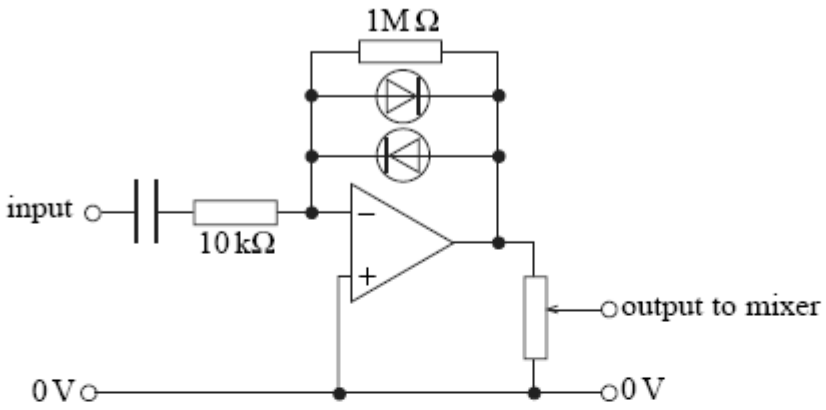
(ii) With the three effects switched off, state **two** differences between the signal at the input and the output of the whole system.

.....

.....

(3 marks)

(c) The circuit diagram for effect 1 is shown below.



(i) Clearly label a virtual earth point on this circuit with the letter **P**.

(ii) Estimate the maximum and minimum signal output voltage from this circuit.

.....

.....

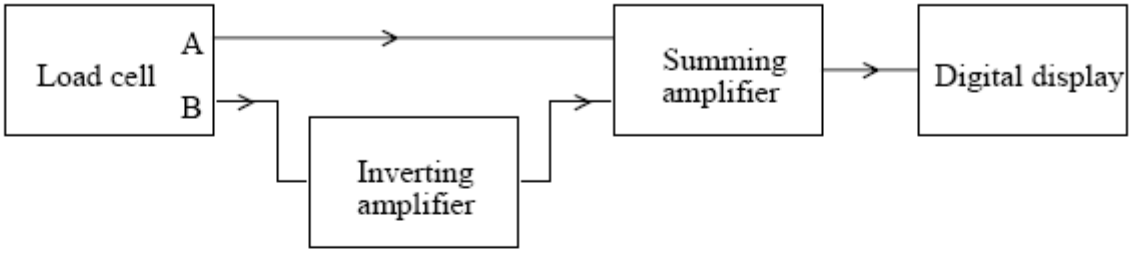
(iii) What is the function of the potentiometer?

.....

(4 marks)

Inverting and Summing Amplifiers (ELE2, Q5, 2007)

5 The system diagram for an electronic balance (weighing machine) is shown below. The balance is powered by a ±9 V supply.

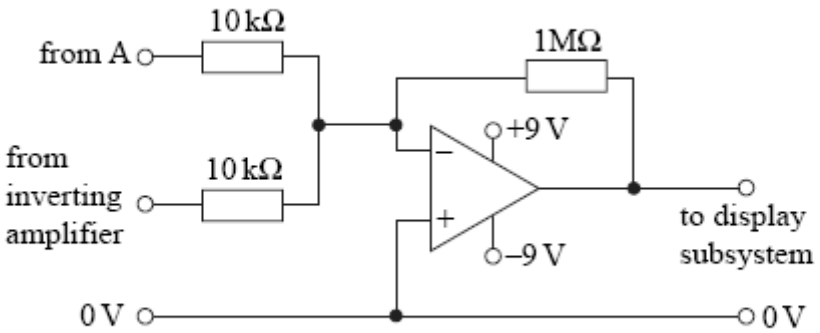


The load cell has a differential output and when there is no force on the load cell, outputs A and B are both at 0 V. When there is a force on the load cell, then output A produces an output of $-v$ and output B produces an output of $+v$, where v is a small voltage which is proportional to the force on the load cell.

(a) Output B is passed through an amplifier with a voltage gain of −1. In the space below draw the circuit diagram of an op-amp based amplifier with a voltage gain of −1 and state suitable values for any resistors that you use.

(4 marks)

(b) The circuit diagram for the summing amplifier is shown below.



(i) Label the virtual earth point on the amplifier with the letter X.

(ii) Calculate the output voltage from the summing amplifier when the output voltage from the load cell is ±*v*.

.....

.....

(3 marks)

(c) The digital display is a voltmeter, with a maximum reading of 1.99 V. The output from the load cell is ±5 mV when there is a load of 1 kg.

(i) Calculate the maximum load that the weighing machine can measure and display.

.....

.....

(ii) Calculate the smallest change in load that can be detected.

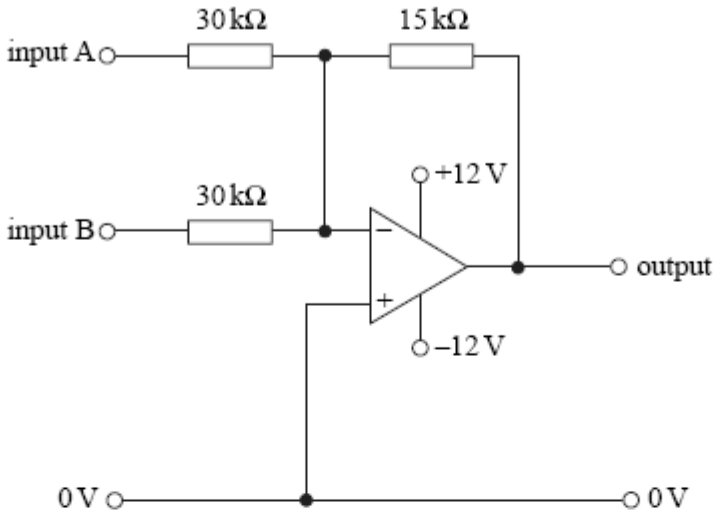
.....

.....

(2 marks)

Summing Amplifier (ELE2, Q4, 2005)

4 The circuit diagram for a summing amplifier is shown below.



(a) Label a virtual earth point in the circuit above with the letter **P**. *(1 mark)*

(b) If input B is connected to 0 V and an audio signal of 2 V amplitude is connected to input A, calculate the amplitude of the output signal.

.....

.....

(2 marks)

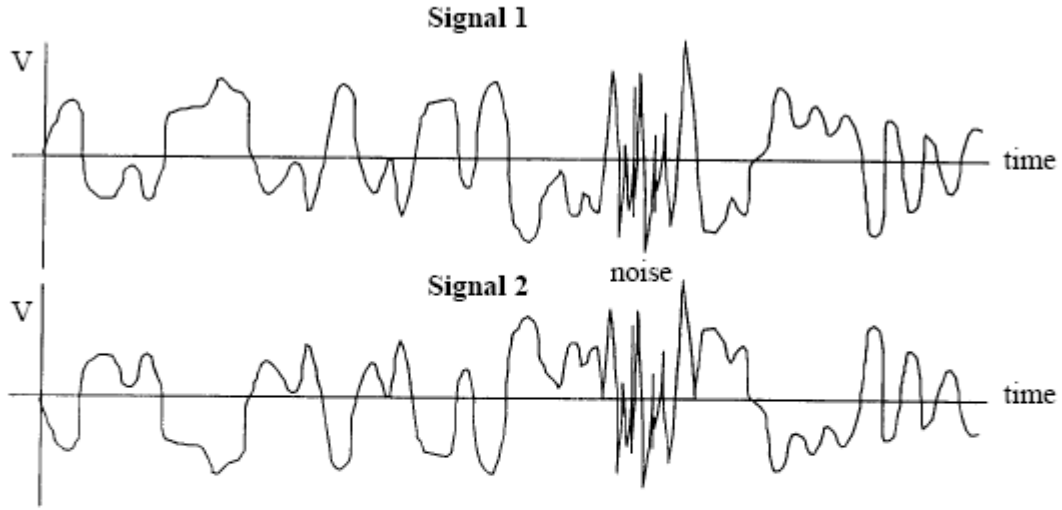
(c) With the audio signal still connected to input A, input B is disconnected from 0 V and connected to input A. What will be the amplitude of the output signal in this case?

.....

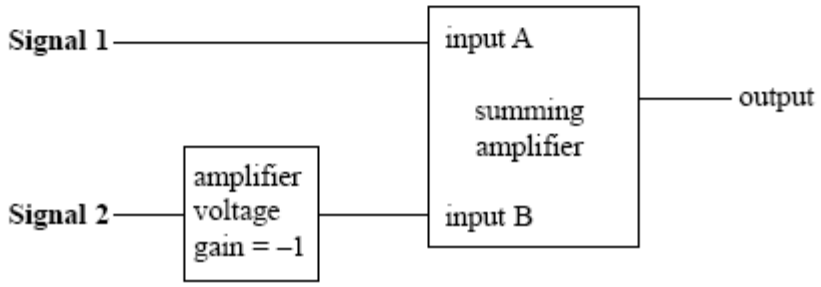
.....

(1 mark)

(d) A microphone gives two audio signal outputs with respect to 0 V. **Signal 2** is inverted compared to **Signal 1**. The signals received at the far end of a long cable carrying the microphone signal are shown below. The noise interfering with both signals is the same.



Signal 1 is connected to input A of a summing amplifier. **Signal 2** is passed through an amplifier with a voltage gain of –1 and then connected to input B of the summing amplifier, as shown in the diagram below.



(i) What is the effect of the amplifier with a voltage gain of –1 on **Signal 2**?

.....

.....

(ii) Explain how this arrangement is able to reduce significantly the effect of noise, picked up by the long cable, on the microphone signal.

.....

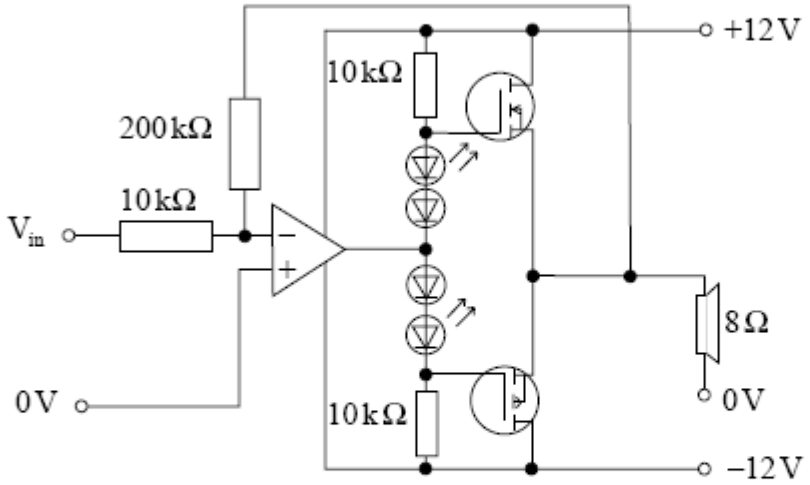
.....

.....

(5 marks)

Power Amp (ELE2, Q4, 2008 – ELE2, Q7, 2007 – ELE2, Q7, 2005 – ELE2, Q4, 2006)

4 A student wants to amplify the output from the sound card on his computer so that he can use loudspeakers instead of headphones. His sound card gives a maximum peak output voltage of 500 mV. He wants to use an amplifier circuit that he has found on a website, but needs to decide if it will be suitable.
The circuit diagram is shown below.



4 (a) Show that the peak voltage developed across the loudspeaker will be approximately 10 V when there is an input of 500 mV.

.....

.....

(2 marks)

4 (b) Calculate the rms output power into the loudspeaker under these conditions.

.....

.....

(2 marks)

The student is concerned that the amplifier will suffer from *cross-over distortion*.

4 (c) (i) Explain what is meant by cross-over distortion.

.....

.....

.....

4 (c) (ii) State what measures have been taken to reduce cross-over distortion in the circuit.

.....

.....

(3 marks)

4 (d) With the circuit constructed and working, the student finds that the MOSFETs become very hot. His teacher recommends that he should bolt each MOSFET to a heatsink.

State **two** important features of an efficient heatsink.

.....

.....

(2 marks)

7 A student wants to build a bass guitar practice amplifier.
A large 4 Ω loudspeaker and power supply are available.
The power supply provides ±15 V at a maximum current of 4 amps.
The peak output signal from the guitar is 75 mV.

(a) (i) Show that the voltage gain needed from the amplifier is approximately 200, if the amplifier just saturates on the peak signal from the guitar.

.....

.....

(ii) The amplifier contains an op-amp with a voltage gain-bandwidth product of 6×10^5 Hz. Calculate, showing your working, the maximum frequency at which the amplifier will saturate when using the guitar as an input.

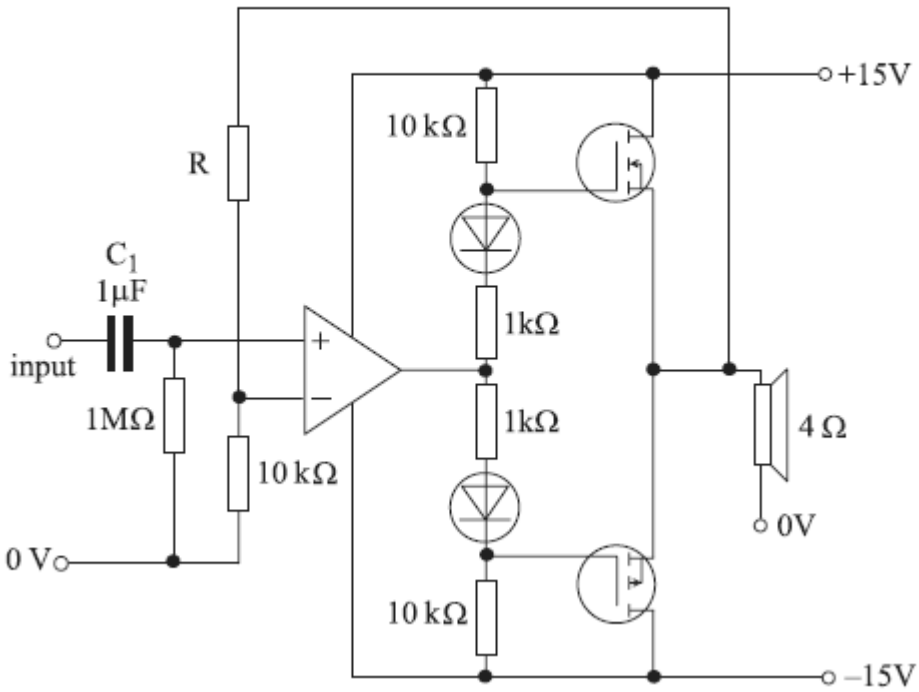
.....

.....

.....

(2 marks)

The circuit diagram for the amplifier is shown below.



(b) (i) Estimate the input impedance of the amplifier circuit, stating any assumption that you make.

.....

.....

(ii) Calculate a value for the feedback resistor R so that the overall amplifier circuit will have a voltage gain of 200. State any assumption that you make.

.....

.....

.....

.....

.....

.....

(6 marks)

(c) When the amplifier has been constructed, the student is concerned that it should not suffer from cross-over distortion. In order to check this the current passing through the drain of the n-channel MOSFET is measured and has a value of 50 mA when there is no input signal to the amplifier.

(i) What is cross-over distortion?

.....

.....

.....

(ii) Explain whether the amplifier will suffer from cross-over distortion.

.....

.....

.....

(3 marks)

(d) (i) Show that the maximum theoretical output power of the amplifier is approximately 28W rms.

.....

.....

.....

(ii) State **two** reasons why the maximum output power is likely to be less than this in practice.

.....

.....

.....

(4 marks)

(e) In operation, the MOSFETs become very hot and so the student decides to bolt them onto heat sinks.
State **three** important design features of efficient heat sinks.

.....

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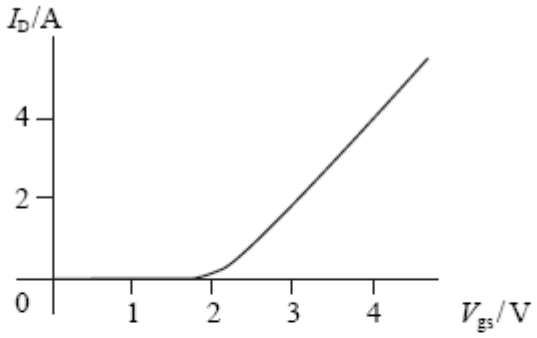
.....

.....

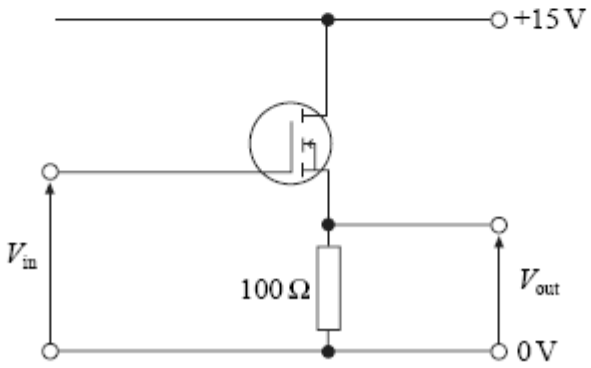
.....

(3 marks)

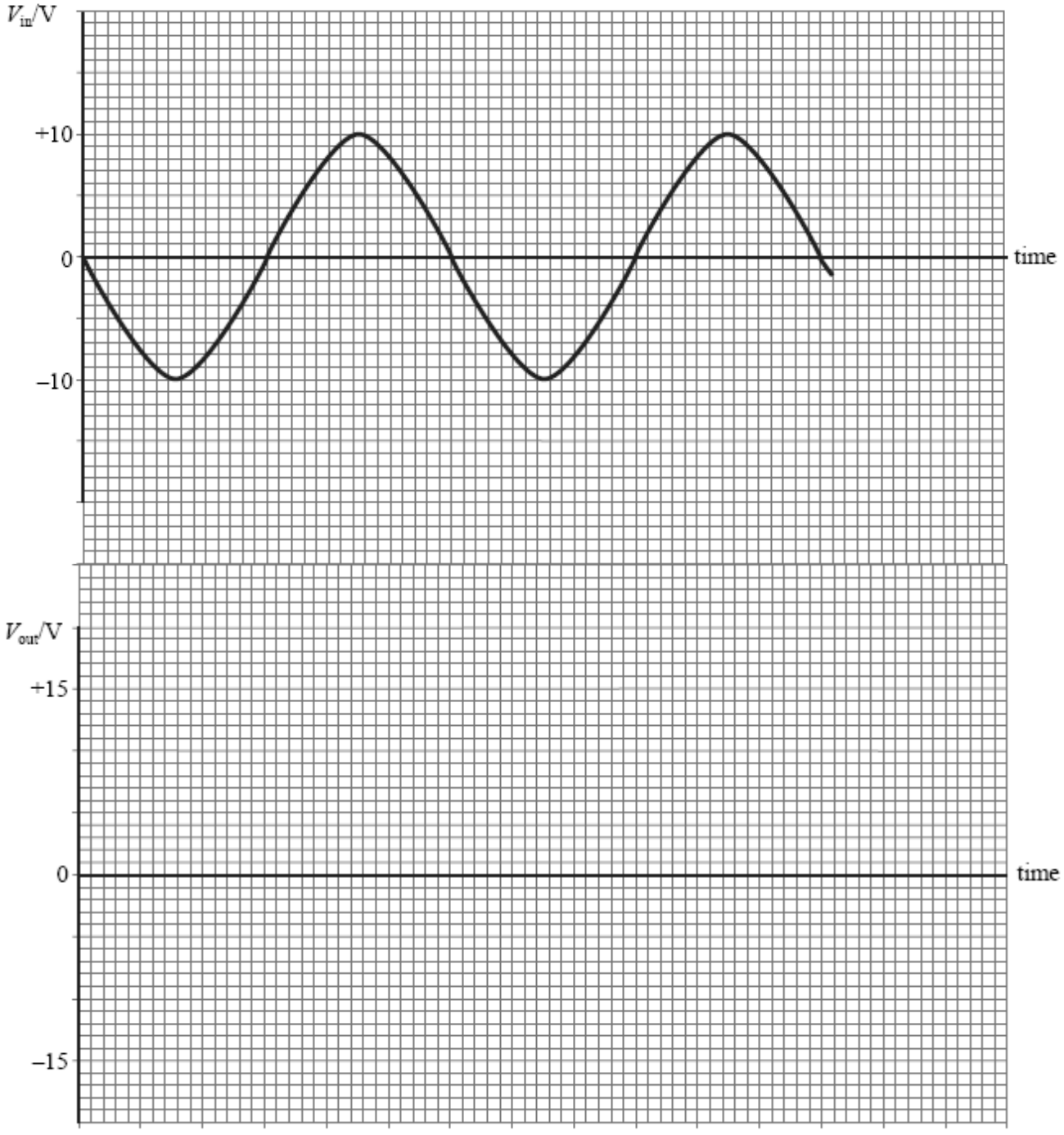
7 The I_D/V_{gs} characteristic for a power MOSFET is shown below.



The MOSFET is connected as a source follower as shown in the circuit below.

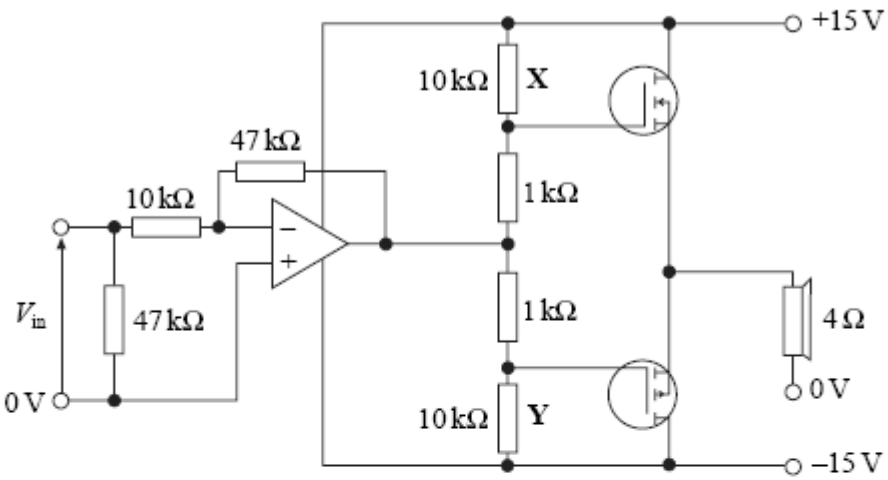


(a) An alternating voltage of 10 V amplitude is supplied to the input of the source follower as shown in the graph below.
Sketch a graph on the axes to show the corresponding output voltage.



(3 marks)

A matched pair of n-channel and p-channel MOSFETs are connected as shown in the circuit diagram below.



(b) (i) What is the name given to this arrangement of MOSFETs?

.....

(ii) Estimate the voltage gain of this circuit, showing your working.

.....

.....

(3 marks)

(c) At low volume levels, the output signal is distorted.

(i) State the name of this type of distortion.

.....

(ii) Explain how this distortion arises.

.....

.....

.....

(iii) With no input signal, estimate the reading that you would observe on an ammeter placed in the drain circuit of either MOSFET.

.....

(4 marks)

(d) This distortion can be reduced by decreasing the value of the resistors **X** and **Y**. Suggest, with reasoning, suitable new values for these resistors.

.....

.....

.....

(3 marks)

(e) State another way in which the low volume distortion can be reduced.

.....

.....

(2 marks)

(f) Estimate, showing your reasoning, the maximum undistorted rms output power to the speaker.

.....

.....

.....

(3 marks)

4 A power amplifier consists of an op-amp driving an n-channel and a p-channel MOSFET arranged as a push-pull circuit.

(a) Explain what is meant by the term *push-pull*.

.....

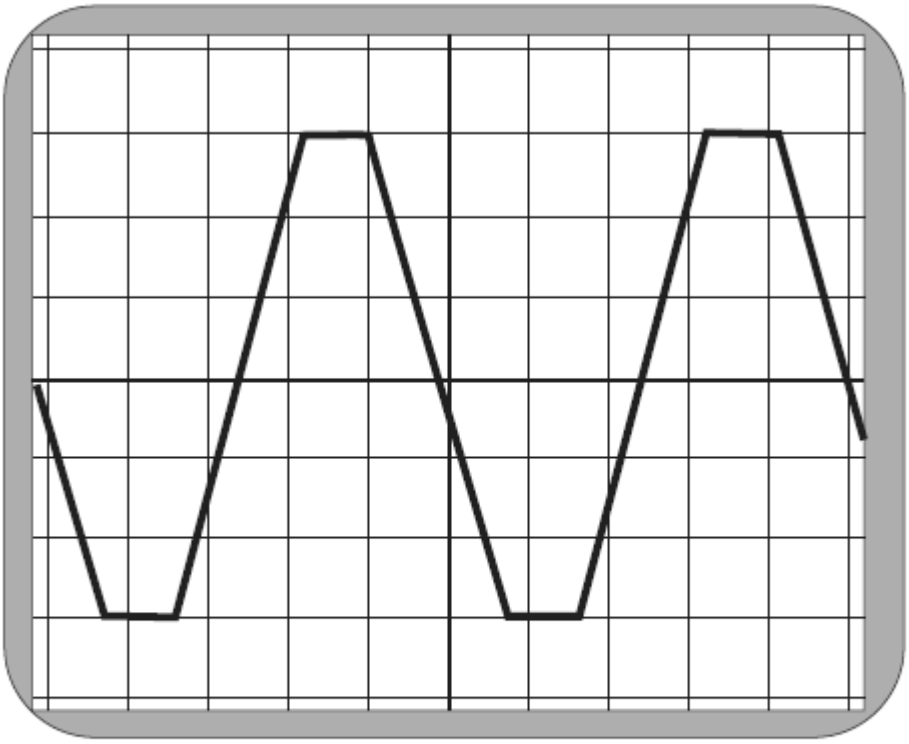
.....

.....

.....

(2 marks)

(b) The amplifier is driven by a sine wave test signal. When operating at full volume into a 4 Ω loudspeaker, an oscilloscope trace of the output shows some distortion as shown below.



(i) State **one** electrical property of the amplifier system that causes this distortion.

.....

(ii) If the y-scale of the oscilloscope trace is 5 V per division, show that the maximum undistorted rms power output of the amplifier into a 4 Ω loudspeaker would be approximately 28 watts.

.....

.....

.....

(iii) Calculate the rms current through the loudspeaker at this power.

.....

.....

(4 marks)

(c) The push-pull amplifier circuit operates from a ±18 V power supply. When the amplifier is delivering 28 W to the loudspeaker, show that the power supplied to the amplifier is approximately 34 W.

.....

.....

(2 marks)

(d) Explain what happens to the energy that is supplied to the amplifier but not dissipated in the loudspeaker.

.....

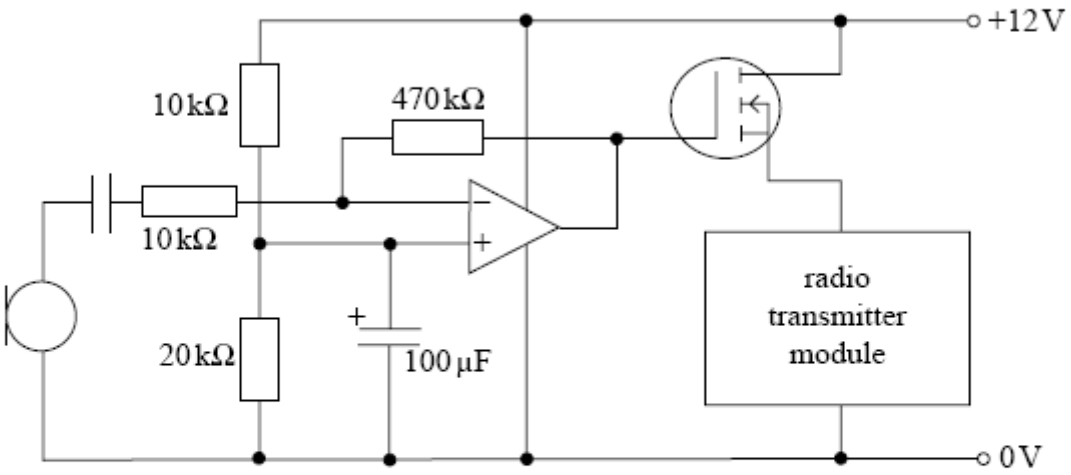
.....

(1 mark)

Op-Amp and Source Follower (ELE2, Q3, 2008)

3 Part of the circuit diagram for a low power radio transmitter is shown below.

The audio amplifier controls the current through the radio transmitter module.



3 (a) (i) Label the source connection of the MOSFET with an S.

3 (a) (ii) What is the name for the circuit arrangement in which the MOSFET is being used?

.....

(2 marks)

3 (b) (i) Show that the voltage at the non-inverting input of the op-amp is 8 V.

.....

.....

3 (b) (ii) With no input signal from the microphone, explain why the voltage on the gate of the MOSFET is also 8 V.

.....

.....

.....

3 (b) (iii) If the turn on value of V_{gs} for the MOSFET is 2 V, what is the voltage across the radio transmitter module, when there is no signal from the microphone?

.....

(4 marks)

3 (c) (i) Calculate the voltage gain of the op-amp amplifier.

.....

.....

3 (c) (ii) If the microphone gives an output of 40 mV, estimate the voltage change that occurs across the radio transmitter module, showing your working.

.....

.....

.....

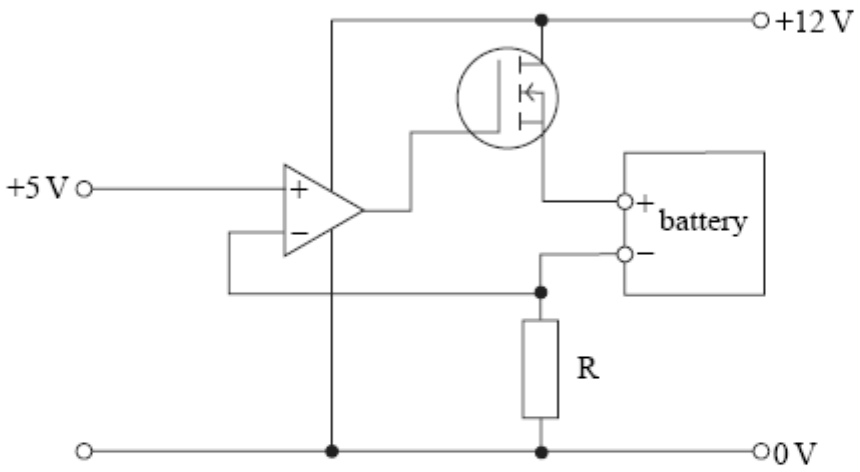
.....

(3 marks)

MOSFET Source Follower / Constant Current Generator (ELE2, Q4, 2007)

4 The NiMH rechargeable battery in a digital camera needs to be charged at a constant current of 200 mA.

The circuit diagram for the constant current generator is shown below.



(a) If the output of the op-amp is not saturated, explain why the voltage at the inverting input of the op-amp must be 5 V.

.....

.....

.....

.....

(2 marks)

(b) The inverting input of the op-amp is connected to the resistor R. Calculate the value of R so that a current of 200 mA can pass through the battery.

.....

.....

(2 marks)

(c) (i) What is the function of the MOSFET?

.....

(ii) Why is it needed in this application?

.....

(2 marks)

(d) As the battery is charged, the voltage across its terminals rises. Explain how this circuit maintains a constant current through the battery.

.....

.....

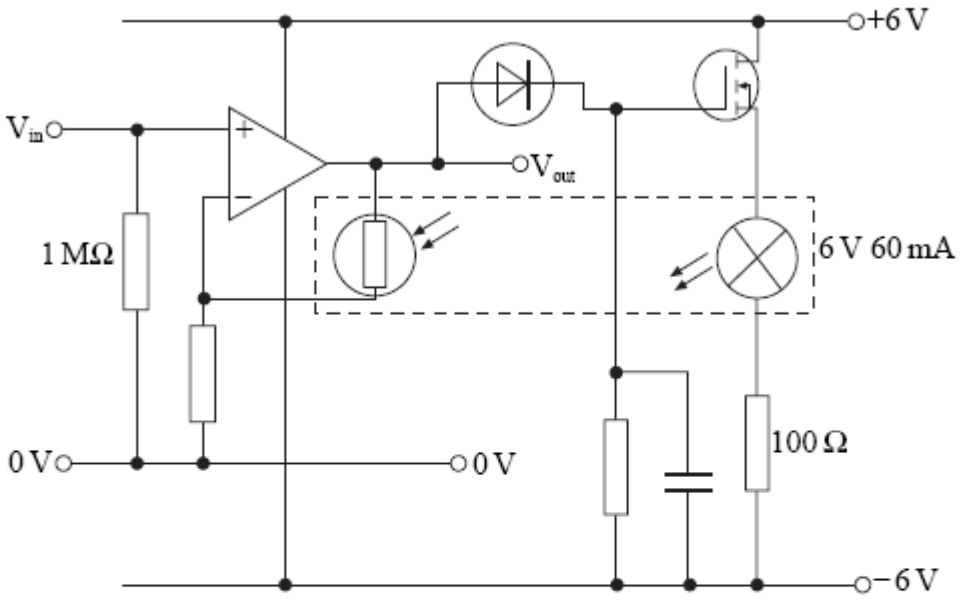
.....

.....

(3 marks)

MOSFET Source Follower and Non-Inverting Amplifier (ELE2, Q5, 2006)

5 The circuit diagram below was found in an analogue sound recording studio.



The lamp and LDR are in a sealed container so that only light from the lamp illuminates the LDR.
The output from the op-amp goes to a MOSFET circuit via a diode.

(a) Name the circuit arrangement for this MOSFET.

.....

(1 mark)

(b) With no input signal to the op-amp, explain why the MOSFET gate voltage is −0.7 V.

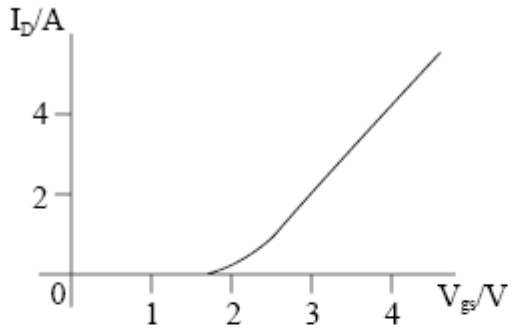
.....

.....

.....

(1 mark)

(c) The characteristic for the MOSFET is shown below.



When the lamp is just lit, estimate, giving a reason for your answer, the voltage difference between the gate and the source of the MOSFET in the circuit diagram on **page 10**.

.....

.....

(2 marks)

(d) (i) Explain why the voltage on the gate of the MOSFET will increase when there is an input signal to the amplifier.

.....

.....

(ii) What effect will this increase in voltage have on the brightness of the lamp?

.....

(iii) What effect will this increase in voltage have on the resistance of the LDR?

.....

(iv) What effect will this increase in voltage have on the voltage gain of the amplifier?

.....

(4 marks)

(e) Suggest a use for this complete circuit.

.....

(1 mark)

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Teacher Resource Bank

GCE Electronics

Exemplar Exam Questions – Mark Scheme

- ELEC2: Further Electronics

Capacitor in Series and Time Constant (ELE1, Q3, 2007)

3 (a) (i) $1 \div 68 + 1 \div 68$, or $(68 \times 68) \div (68 + 68) = 34\mu F$✓✓

(ii) $34 \times 10^{-6} \times 150 \times 10^{3} = 5.1s$✓✓

(4 marks)

(b) (i) $T = 0.69RC$, $0.69 \times 5.1 = 3.5s$✓✓

(ii) $5RC = 5 \times 5.1 = 25.5s$✓

(3 marks)
(Total 7 marks)

Capacitors in Parallel and Time Constant (ELE1, Q3, 2006)

3 (a) (i) $I = V/R = 12/10^{4}$✓ = 1.2 mA✓

(ii) 2200 + 1000 = 3200µF✓

(iii) $T = RC = 10^{4} \times 3.2 \times 10^{-3}$✓ = 32s✓

(5 marks)

(b) (i) 6/12 = ½ Vs✓ $T = 0.69RC$✓ $0.69 \times 32 = 22s$✓

(ii) $5RC = 5 \times 32$✓ = 160s✓

(5 marks)
(question total 10 marks)

Time Constant (ELE1, Q2, 2008)

2 (a) (i) $9 \div 330$✓ = 27mA✓

(ii) 9×0.027✓ = 0.25W✓

(b) (i) 155×10^{-3}✓ = 0.155s✓

(ii) $5RC = 0.78s$✓

(iii) $T = 10^{4} \times 0.47 \times 10^{-3}$✓ = 4.7s✓ $5RC = 23.5s$✓

Total – 10

Time Constant and Capacitors in Parallel (ELE1, Q2, 2005)

2 (a) (i) 22 + 47 = 69 µF✓

(ii) 69 x 0.200 =✓ 13.8 s✓

(3 marks)

(b) (i) 0.69 x 13.8 =✓ 9.5 s✓

(ii) 5 x 13.8 =✓ 69 s✓

(4 marks)

Total 7 marks

555 Monostable and Relay (ELE1, Q7, 2005 – ELE1, Q6, 2006)

7 (a) 1.1 x 680 k x 470 µF =✓ 350 s✓ (2 marks)

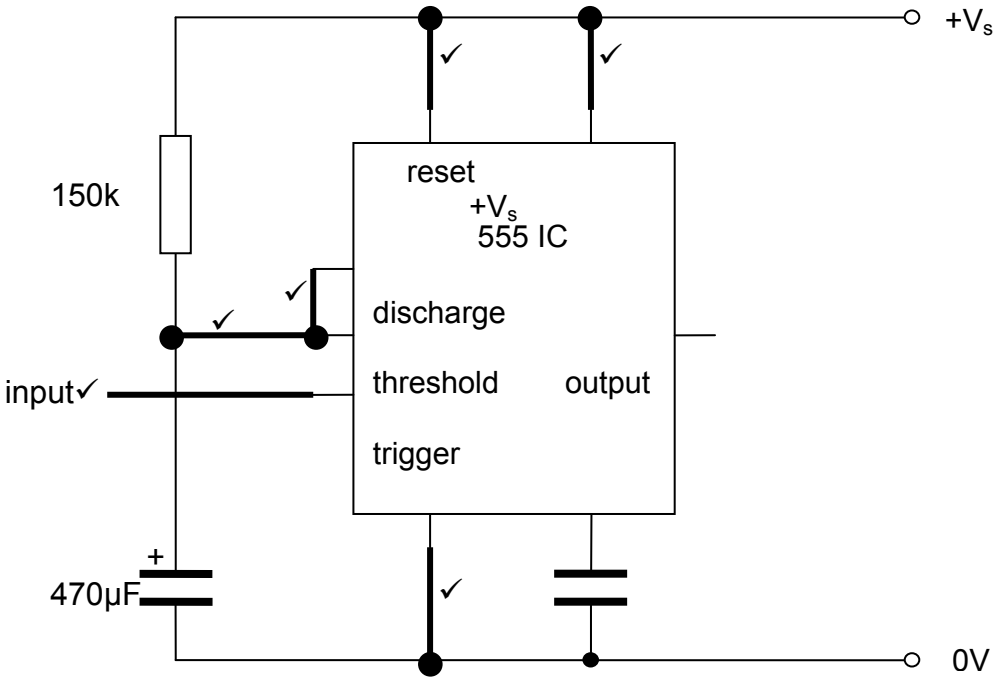
(b) negative going✓ (1 mark)

(c) NO✓ (1 mark)

(d) diode across coil in inverse parallel✓ (1 mark)

Total 5 marks

6 (a)



(6 marks)

(b) 1.1 RC = 1.1 x 1.5 x 10^5 x 4.7 x 10^{-4} ✓= 77.5s✓

(2 marks)

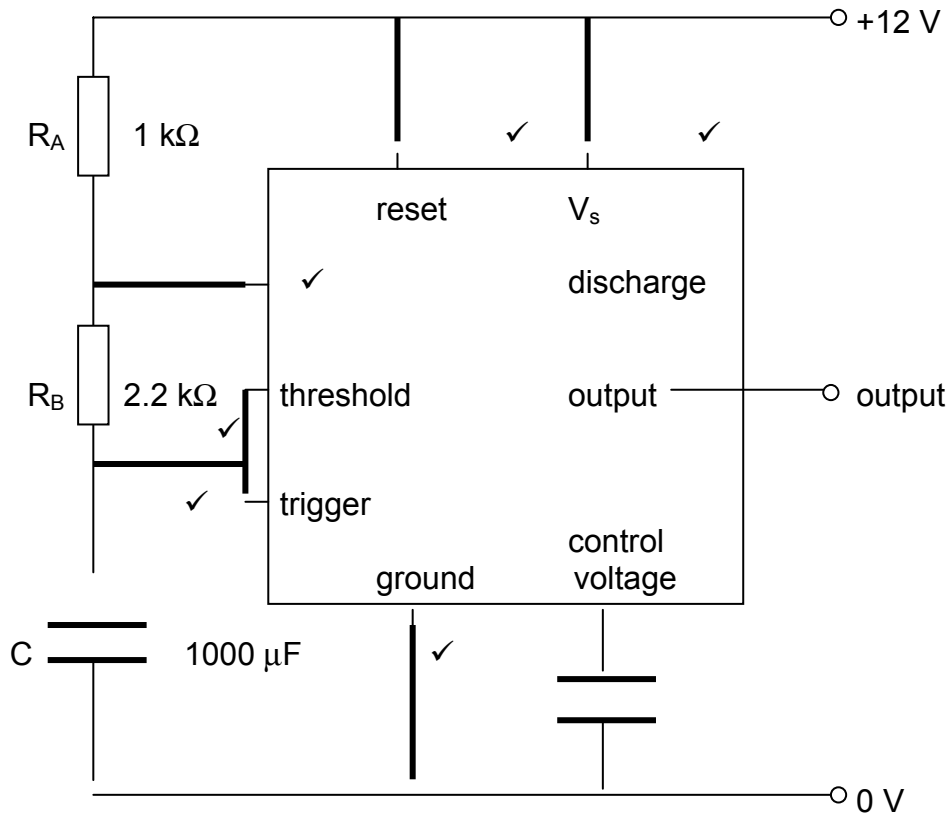
(c) COM✓ and NO✓ (any order)

(2 marks)

(question total 10 marks)

555 Astable (ELE1, Q4, 2005 – ELE1, Q5, 2007)

4 (a)



(6 marks)

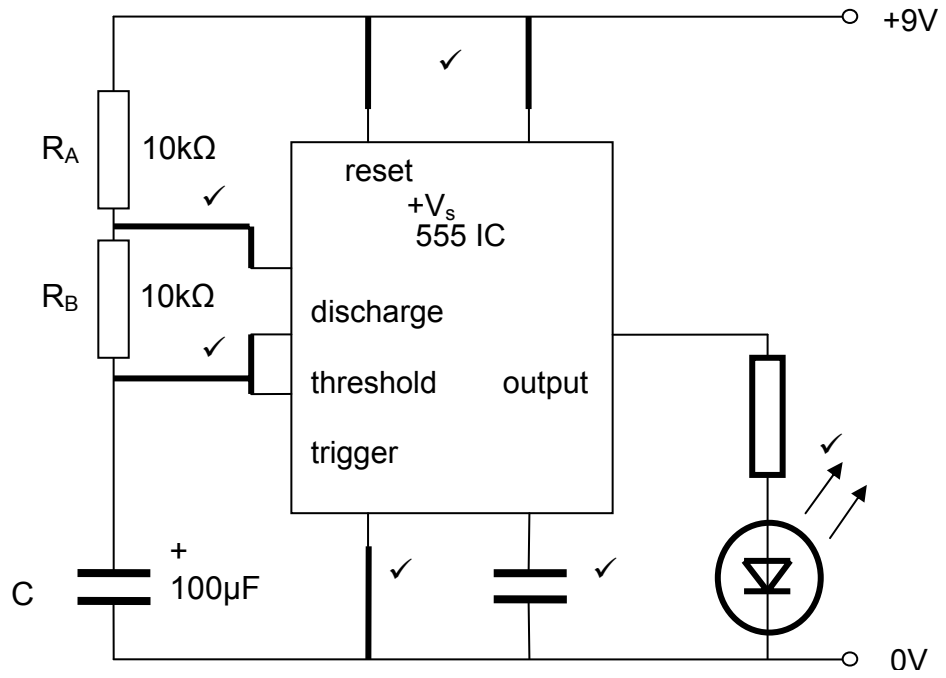
(b) (i) $0.7 \times 2.2 \times 10^3 \times 10^{-3} =$✓ 1.54 s✓

(ii) $0.7 \times 3.2 \times 10^3 \times 10^{-3} =$✓ 2.24 s✓ (4 marks)

Total 10 marks

5 (a) (i)

(ii)



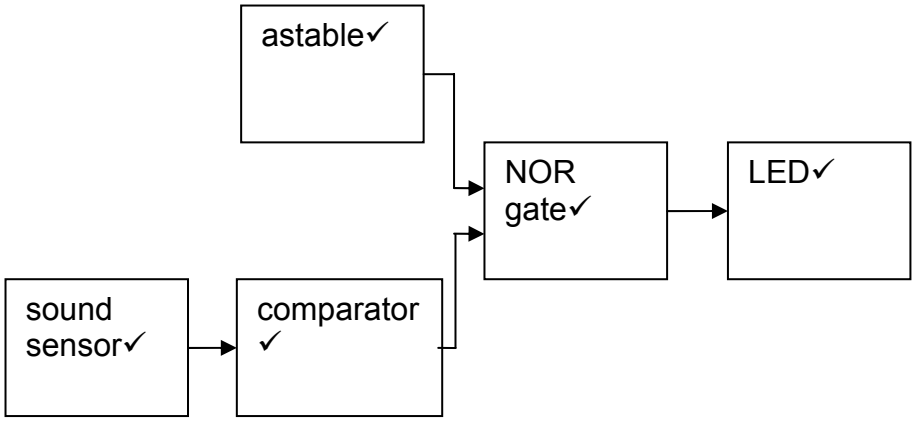
(6 marks)

(b) (i) $t_h = 0.7 \times 2 \times 10^4 \times 10^{-4} =$✓1.4s✓
(ii) $t_l = 0.7 \times 10^4 \times 10^{-4} =$✓ 0.7s✓
(iii) $f = 1.44 \div (3 \times 10^4 \times 10^{-4}) =$ ✓ 0.5Hz✓

(6 marks)
(Total 12 marks)

Comparitor and 555 Astable (ELE1, Q5, 2008)

5 (a)

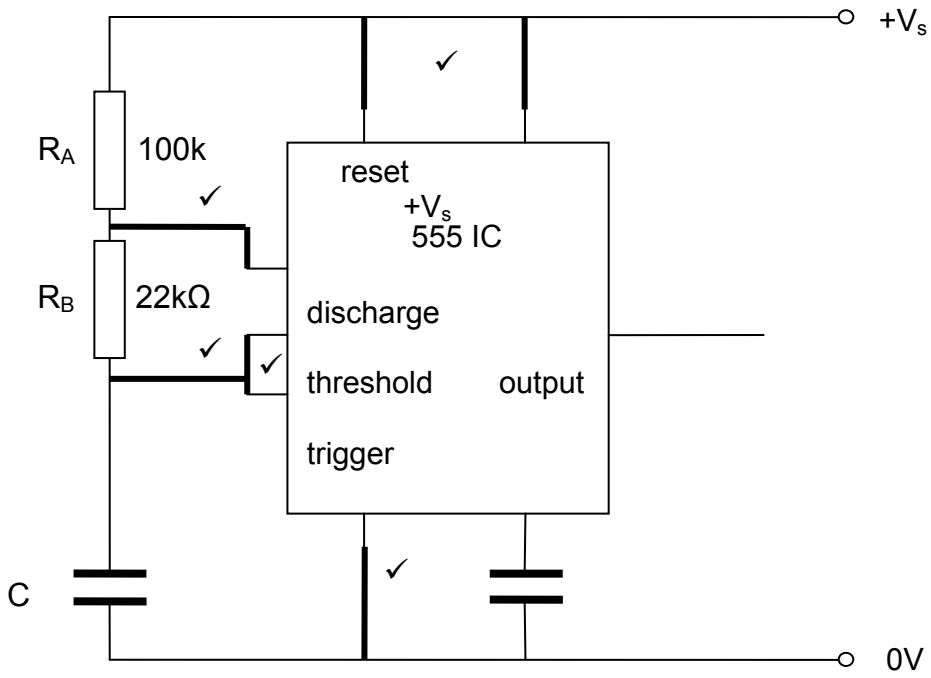


(b) (i) comparator✓

(ii) astable✓

(c) (i) (1 ÷ 1501) × 9V✓ = 6mV✓
(ii) 9V or high✓
(iii) 0V or low✓

(d) (i)



(ii) C = 1.44 ÷ 1.44 × 10^5 × 2Hz✓ = 5μF✓

Total – 18

Sheft Register (ELE2, Q6, 2005 – ELE2, Q6, 2008 – ELE2, Q6, 2007)

6 (a) On the rising edge of each clock pulse ✓
The data from a D-type flip-flop is stored in the next D-type flip-flop ✓
This data transfer occurs all of the way along the shift register ✓
New data applied to the input of the first flip-flop is taken into the shift register ✓

(4 marks)

(b) Removes multiple pulses due to contact bounce ✓

(1 mark)

(c) The D input of the first flip-flop goes to logic 1 ✓
The clock input goes to logic 1 and the data is shifted along the shift register ✓

(2 marks)

(d) The output of the five input AND gate must be logic 1 =>10001 ✓
The Q output of the last flip-flop must also be logic 1
=> smallest binary number is 100011 ✓

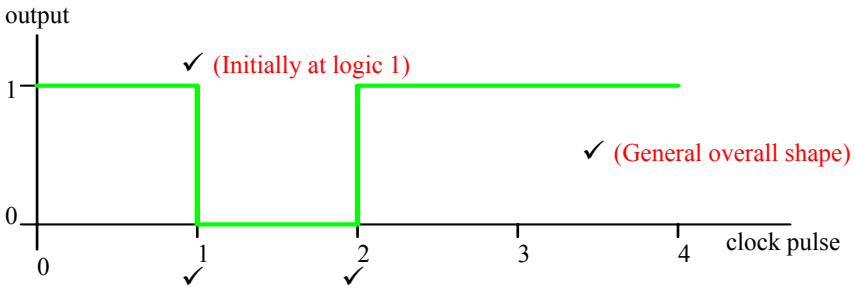
(2 marks)
Total 9 marks

6 (a) For each flip-flop Q becomes D ✓
On the rising edge of the clock pulse ✓
Since D is connected to the previous Q, data is moved along the shift register (on each clock pulse) ✓

(b) (i) Making S logic 0 will not set Q to 0
=> the shift register must be reset before the parallel data is loaded ✓

(ii) Logic 1 ✓

(c)



Total – 9

6 (a) (i) CKs all connected together, ✓
Resets all connected together, ✓
D to proceeding Q ✓
Input to D_A ✓

(ii) switch to $+V_s$, ✓
pull down resistor to 0V ✓

(6 marks)

(b) 12 => 1100 => C => appropriate symbol for C ✓
13 => 1101 => D => appropriate symbol for d ✓
15 => 1111 => F => appropriate symbol for F ✓
OR ✓ ✓ ✓

(3 marks)
(Total 9 marks)

NAND Gate Bistable (ELE2, Q1, 2006)

1 (a) (i) One input from gate 1 to output of gate 2, ✓
one input from gate 2 to output of gate 1 ✓
Pull up resistors on the two free inputs ✓

(3 marks)

(ii) Correct points labelled as outputs **Q** and $\overline{\mathbf{Q}}$ ✓
$\overline{\mathbf{SET}}$ on input opposite **Q** ✓
$\overline{\mathbf{RESET}}$ in input opposite $\overline{\mathbf{Q}}$ ✓

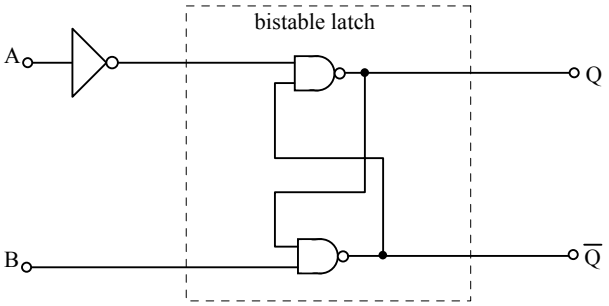
(3 marks)

(b) When the **SET** input is briefly taken to logic 0 ✓
The **Q** output will become logic 1 and the $\overline{\mathbf{Q}}$ output will become logic 0 ✓
When the **RESET** input is now briefly taken to logic 0, **Q** will become logic 0 and the $\overline{\mathbf{Q}}$ will become logic 1 ✓

(3 marks)
(question total 9 marks)

NAND Gate Bistable and MOSFET (ELE2, Q3, 2005)

3 (a)

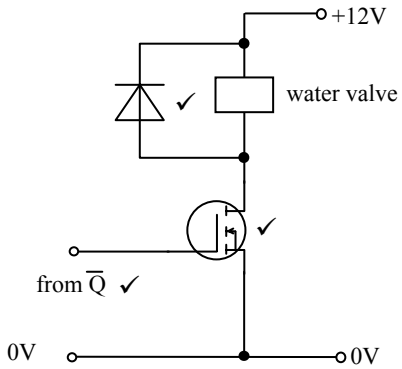


✓ ✓

(2 marks)

(b) (i) 0 ✓
(ii) 0 ✓
(iii) 1 ✓
(iv) 1 ✓ (4 marks)

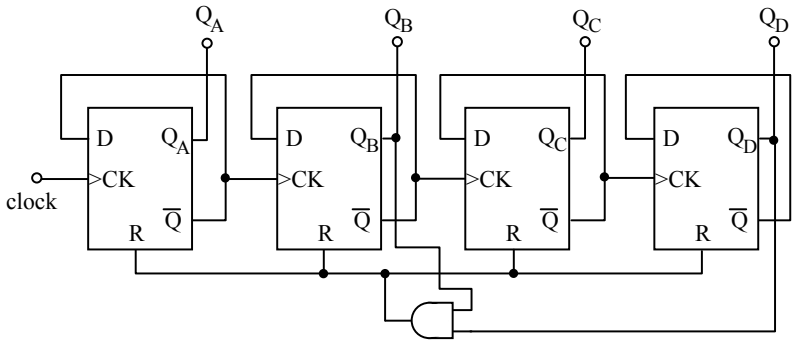
(c)



(3 marks)
Total 9 marks

Counter and Boolean (ELE2, Q5, 2005)

5 (a)



D to $\overline{\mathbf{Q}}$ ✓
All Resets joined together ✓
$\overline{\mathbf{Q}}$ to following **CK** ✓
Output of AND gate to Reset ✓
B and D to inputs of AND gate ✓

(4 marks)

(b) Binary values for when the heater is on:
0010, 0101, 0111, 1000 ✓
The counter outputs ANDed together to form the binary values which are then ORed ✓

(2 marks)

(c)

$$\overline{D}.\overline{C}.B.\overline{A} + \overline{D}.C.\overline{B}.A + \overline{D}.C.B.A + D.\overline{C}.\overline{B}.\overline{A}$$
$$= \overline{D}.\overline{C}.B.\overline{A} + D.\overline{C}.\overline{B}.\overline{A} + \overline{D}.C.A.\left(\overline{B} + B\right) \quad \checkmark\checkmark\checkmark$$
$$= \overline{C}.\overline{A}\left(\overline{D}.B + D.\overline{B}\right) + \overline{D}.C.A$$
$$= \overline{C}.\overline{A}\left(D \oplus B\right) + \overline{D}.C.A$$

(3 marks)
Total 9 marks

Counter (ELE2, Q1, 2007)

1 (a) **D** to $\overline{Q}$ ✓
$\overline{Q}$ to next clock ✓
C to AND gate input ✓
D to AND gate input ✓
AND output connected to all resets ✓

(max 4 marks)

(b) (i) Each term represents one line within the truth table for which the output is 1 ✓
Each letter within each term represents the logic state of the counter outputs ✓

(ii) Correct use of either Karnaugh Map of Boolean algebra ✓
At least one piece of simplification ✓
Simplification to $\overline{D}.C.A + D.\overline{C}.B$ ✓

(5 marks)
(Total 9 marks)

Non-Inverting Amplifier (ELE2, Q2, 2008)

2 (a) (i) $V = I \times R = 10^7 \times 2 \times 10^{-10}$ ✓
$= 2 \times 10^{-3}V$ ✓

(ii) $G_v = V_{out} / V_{in} = 200 \times 10^{-3} / 2 \times 10^{-3}$ ✓
$= 100$ ✓

(b) Very high impedance (resistance) input ✓
This will not shunt the 10MΩ resistor of the ionisation chamber so lowering the output voltage ✓

(c) (i) Inverting amp connection to junction of 10MΩ resistor and R ✓

(ii) $(Gv = 1 + Rf / R)$
$\Rightarrow 100 = 1 + 10^7 / R$ ✓
$\Rightarrow R = 10^7 / 99 = 101k\Omega$ ✓ **Total – 9**

Voltage Follower, Summing Amplifier, Inverting Amplifier (ELE2, Q6, 2006)

6 (a) (i) 1 ✓ *(1 mark)*

(ii) 1MΩ ✓ *(1 mark)*

(b) (i) -1 ✓ *(1 mark)*

(ii) amplitude x 10 ✓
inverted ✓ *(2 marks)*

(c) (i) inverting input terminal of op-amp ✓ *(1 mark)*

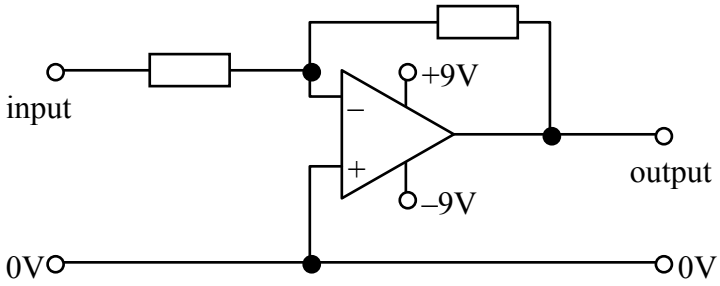
(ii) +0.7V ✓
-0.7V ✓ *(2 marks)*

(iii) volume (level) control ✓ *(1 mark)*

(question total 9 marks)

Inverting and Summing Amplifiers (ELE2, Q5, 2007)

5 (a) correctly connected inputs, ✓
feedback resistor in correct place, ✓
realistic values of R - accept between 1kΩ and 1MΩ, ✓
both Rs the same. ✓



(4 marks)

(b) (i) Any appropriate place associated with inverting input of op-amp ✓
(Accept if not X!)

(ii) Appropriate calculation leading to answer ✓
e.g. $-10^6 \left(\frac{v}{10^4} + \frac{v}{10^4} \right)$
Output voltage = (+)200*v* ✓

(3 marks)

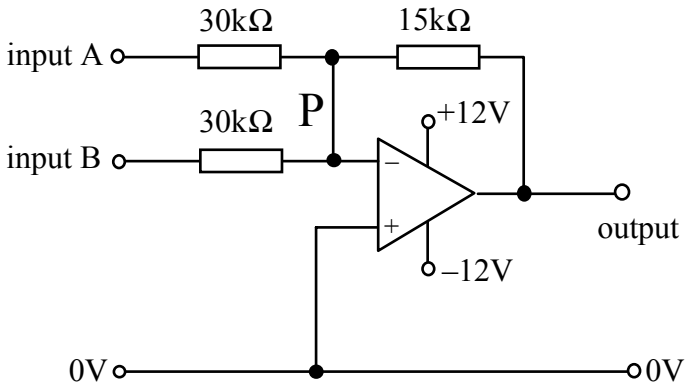
(c) (i) Calculation leading to answer of 1.99kg ✓

(ii) Resolution of meter is 0.01V
=> smallest change in weight is 0.01kg or 10g ✓

(2 marks)
(Total 9 marks)

Summing Amplifier (ELE2, Q4, 2005)

4 (a)



✓

(1 mark)

(b) $V_{out} = -R_f\{V_a/R_a + V_b/R_b\}$ ✓
$V_{out} = -15\{2/30 + 0/30\} = -1V$ ✓ (2 marks)

(c) $V_{out} = -15\{2/30 + 2/30\} = -2V$ ✓ (1 mark)

(d) (i) The magnitude of the signal is not altered ✓
The signal is inverted ✓

(ii) Signal 2 is inverted which makes the audio in phase with signal 1 ✓
The noise on signal 2 is inverted compared to that on signal 1 ✓
When added together the noise signals cancel ✓ (5 marks)

Total 9 marks

Power Amp (ELE2, Q4, 2008 – ELE2, Q7, 2007 – ELE2, Q7, 2005 – ELE2, Q4, 2006)

4 (a) Inverting amplifier with a voltage gain of 200 / 10 = 20 ✓
So with a 500mV input the output will be 10V ✓

(b) $P_{rms} = V_p^2 / 2 \times R = 10^2 / 2 \times 8 = 100 / 16$ ✓ = 6.25W ✓

(c) (i) Cross over distortion, when neither of the output transistors conducts at small (input) output voltages ✓

(ii) Diode **biasing** networks to **turn on** the output transistors ✓
Push-pull stage included in the (negative) feedback loop ✓

(d) Large surface area ✓
Dark, matt colour ✓
Good conductor of heat ✓ (max 2)

Total – 9

7 (a) (i) $G_v = V_{out} / V_{in} = 15 / 0.075 = 200$ ✓

(ii) $6 \times 10^5 = f \times G_v = f \times 200$
$\Rightarrow f = 6 \times 10^5 / 200 = 3000Hz$ ✓

(2 marks)

(b) (i) 1MΩ ✓
Assuming input impedance of capacitor is negligible
(or input impedance of op-amp is very large) ✓

(ii) Assume source followers have a voltage gain of 1 ✓
$G_v = 1 + R_f / R_1$ ✓
$200 = 1 + R_f / 10^4$ ✓
$R_f = 1.99 \times 10^6$ (allow 2MΩ) ✓

(6 marks)

(c) (i) X-over distortion is non-linearity in the characteristic of the amplifier ✓
when the signal changes from positive to negative or vice versa ✓

(ii) No - because the MOSFETs are biased into conduction ✓
(mention of 50mA drain current)
(because of the negative feedback loop)

(3 marks)

(d) (i) $P_{out} = V_s^2 / 2 \times R = 15^2 / 8$ ✓
$= 28.125W$ ✓

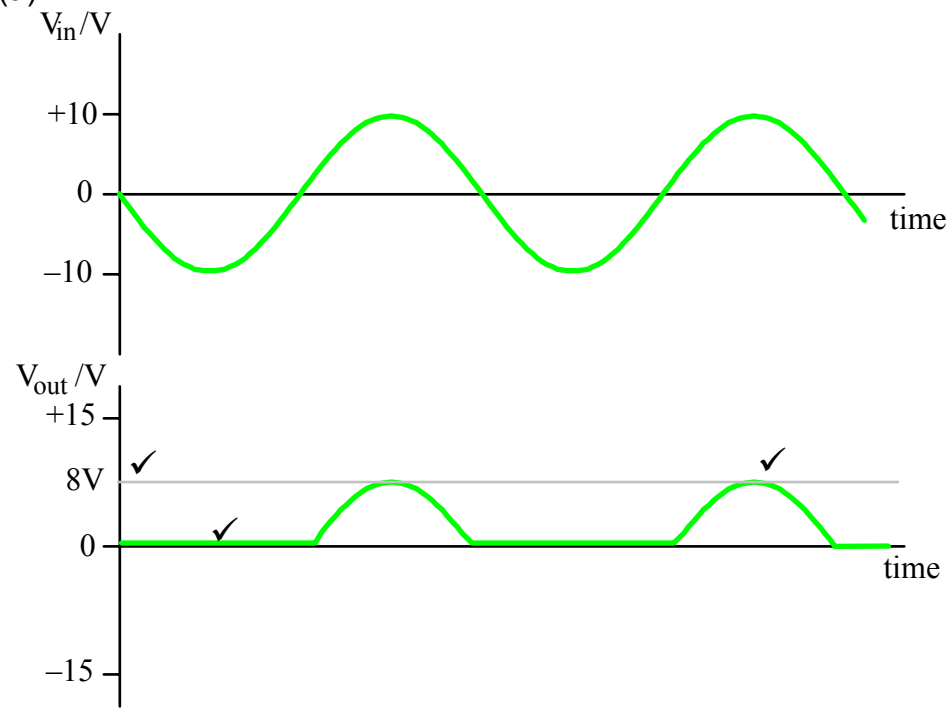
(ii) Output of op-amp does not reach saturation at the supply voltages ✓
MOSFETs have V_{gs} when conducting ✓

(4 marks)

(e) Dark colour (to aid radiation) ✓
Large surface area (to aid radiation and convection) ✓
Made of metal (to aid conduction) ✓
(fan (to assist convection) ✓)

(max 3 marks)
(Total 18 marks)

7 (a)



(3 marks)

(b) (i) Push Pull ✓

(ii) Inverting amplifier with G_V of –4.7 and source follower with G_V of ≈ 1 ✓

=> Overall G_V = –4.7 x 1 = –4.7 ✓ (3 marks)

(c) (i) Cross-over distortion ✓

(ii) When the input voltage is smaller than that needed ✓ to make either MOSFET conduct ✓

(iii) 0 Amps – V_{gs} is only 1.36V => MOSFETs are not conducting ✓ (4 marks)

(d) There needs to be approx 2V across each 1kΩ resistor ✓
So there must be 13V across (X) (Y) ✓
=> 2mA through 1kΩ resistor => (X) (Y) = 6.5kΩ ✓ (3 marks)

(e) Include MOSFETs into feedback loop ✓
by disconnecting 47kΩ resistor from op-amp output and connecting to MOSFET output ✓ (2 marks)

(f) $P = V_S^2/2R$ ✓
=> $P = 15^2/2 \times 4 = 28W$ ✓
If take into account V_{gs} of MOSFETs
ie $P = 13^2/ 2 \times 4 = 21W$ ✓ (3 marks)

Total 18 marks

4 (a) Push-pull. The signal is split into positive and negative going signals ✓
These are amplified separately and then recombined to recreate the amplified signal ✓

(2 marks)

(b) (i) Power supply voltage is not large enough ✓
(Gain too large)
(Saturation or clipping)

(1 mark)

(ii) Maximum output voltage is 15V ✓
Max power = V_P^2 / 2xR = 15^2 / 2x4 = 225 / 8 = 28W ✓

(2 marks)

(iii) Power = I^2 R => 28 = I^2.4 =>I = $\sqrt{7}$ = 2.65A ✓

(1 marks)

(c) rms voltage = 18 / 1.414 = 12.73V ✓
Power supplied = V_{rms} x I_{rms} = 12.73 x 2.65 = 33.7W ✓

(2 marks)

(d) Energy dissipated as heat in the output transistors ✓

(1 marks)
(question total 9 marks)

Op-Amp and Source Follower (ELE2, Q3, 2008)

3 (a) (i) On the line joining the MOSFET to the transmitter
(ii) (Source) follower (common drain amplifier) ✓

(b) (i) Voltage divider **OR** 12V in the ratio of 1 : 2 ✓
Calculation ✓
=> Voltage at non-inverting input is 8V
(ii) Negative feedback attempts to reduce the difference between the two inputs to zero.
=> In the absence of an input signal both inputs will be at 8V so the output must be at 8V ✓
(iii) Two volts appear across the gate to source of the MOSFET so there will be 6V across the rf amplifier ✓

(c) (i) G_v = -R_f / R_1 = -470 / 10 = (-)47 ✓
(ii) If input is 40mV, then op-amp output is 1.88V ✓
Assume G_v of source follower is 1 the voltage change across rf amplifier is also 1.88V ✓

Total – 9

MOSFET Source Follower / Constant Current Generator (ELE2, Q4, 2007)

4 (a) very large open loop voltage gain ✓
so there must only be a very small difference in inputs if output is not to be saturated ✓

(2 marks)

(b) If 200mA passes through battery it must also pass through R ✓
R = V / I => R = 5/0.2 = 25Ω ✓

(2 marks)

(c) (i) source follower (or equivalent) ✓

(ii) The op-amp will not supply such a large current ✓

(2 marks)

(d) As the battery voltage rises, the output of the op-amp will also rise ✓
so as to ensure that there is 200mA passing through the battery and R ✓
and so maintaining the 5V across R and hence 5V at its own input terminals ✓

(3 marks)

(Total 9 marks)

MOSFET Source Follower and Non-inverting Amplifier (ELE2, Q5, 2006)

5 (a) source follower ✓

(1 mark)

(b) The output voltage of the op-amp will be 0V and there will be a voltage drop of 0.7V across the diode, so making the gate of the MOSFET -0.7V

(1 mark)

(c) 2V ✓
The characteristic shows that a drain to source current only passes when Vgs is greater than 2V ✓

(2 marks)

(d) (i) positive parts of the output signal pass to the gate via the diode,
causing the capacitor to charge and so increasing the gate voltage ✓

(1 mark)

(ii) increases the brightness of the lamp ✓

(1 mark)

(iii) decreases the resistance of the LDR ✓

(1 mark)

(iv) decreases the voltage gain of the amplifier ✓

(1 mark)

(e) automatic volume control ✓

(1 mark)

(question total 9 marks)