Centre Number						Candidate Number				
Surname										
Other Names										
Candidate Signature										

For Examiner's Use	
Examiner's Initials	
Question	Mark
1	
2	
3	
4	
5	
6	
TOTAL	

General Certificate of Education
Advanced Subsidiary Examination
June 2014

Electronics ELEC2

Unit 2 Further Electronics

Wednesday 21 May 2014 9.00 am to 10.00 am

For this paper you must have:
- a pencil and ruler
- a calculator
- a Data Sheet (enclosed).

Time allowed
- 1 hour

Instructions
- Use black ink or black ball-point pen.
- Fill in the boxes at the top of this page.
- Answer **all** questions.
- You must answer the questions in the spaces provided. Do not write outside the box around each page or on blank pages.
- Do all rough work in this book. Cross through any work you do not want to be marked.

Information
- The marks for questions are shown in brackets.
- The maximum mark for this paper is 67.

Answer **all** questions in the spaces provided.

1 A student is experimenting with an ultrasound microphone which operates at a frequency of $40\ \text{kHz}$. The microphone produces a maximum output amplitude of $40\ \text{mV}$ and has a very large output resistance (greater than $10\ \text{M}\Omega$). The student needs to amplify the microphone output to give a signal of $4\ \text{V}$ amplitude.

1 (a) Calculate the voltage gain needed from the amplifier.

[2 marks]

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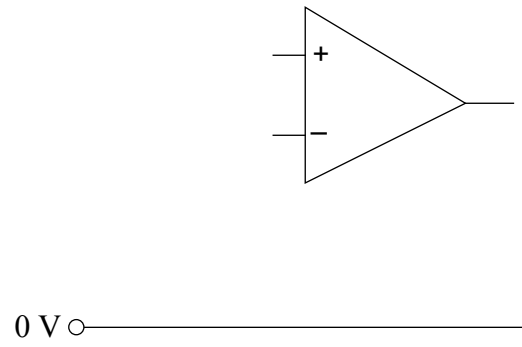
1 (b) Complete the circuit diagram of a suitable op-amp based amplifier in **Figure 1**. Include suitable component values.

[4 marks]

Figure 1



1 (c) When the student tests the amplifier he finds that with an input voltage of $40\ \text{mV}$ amplitude, the output is only $1\ \text{V}$ amplitude. The student consults the op-amp data sheet and finds that the gain-bandwidth product of the op-amp is $10^6\ \text{Hz}$.

1 (c) (i) Explain the meaning of the term **gain-bandwidth product**.

[1 mark]

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1 (c) (ii) Show, using a calculation, why the output of the amplifier is only 1 V.

[2 marks]

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1 (c) (iii) Explain how the student can solve the problem by adding a second op-amp circuit.

[2 marks]

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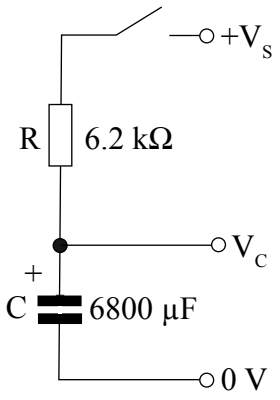
Turn over for the next question

2 A resistor and uncharged capacitor are connected in series as in **Figure 2**.

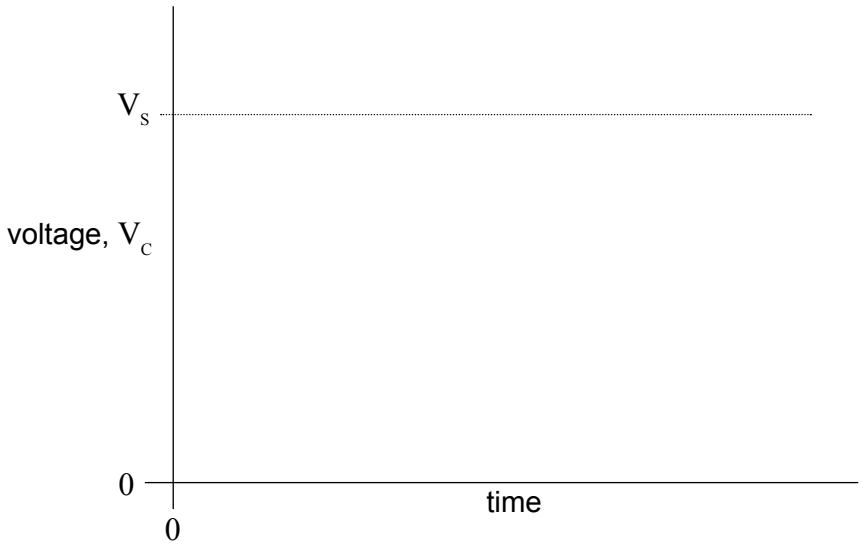
Figure 2



2 (a) If the switch is closed at time $t = 0$, sketch on the axes in **Figure 3** how the voltage across the capacitor, V_C, varies with time.

[2 marks]

Figure 3



2 (b) Calculate the time taken for V_C to be equal to $V_S/2$.

[2 marks]

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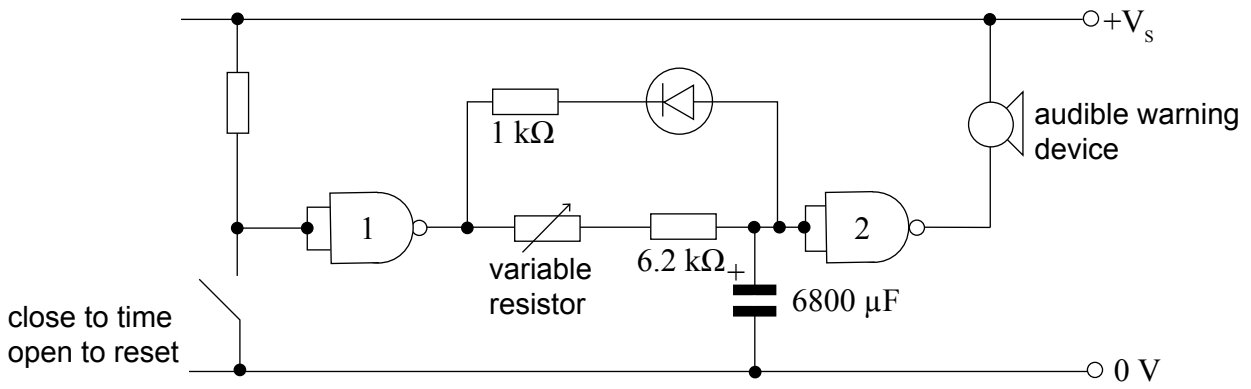
2 (c) A student decides to use this RC timing circuit as the basis for a kitchen timer project. **Figure 4** shows the circuit used.

Figure 4



The student wants the maximum time to be about 1 hour. Assuming that the logic gates switch at $V_s/2$, calculate a suitable value for the variable resistor.

[2 marks]

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2 (d) When constructed, timings up to a few minutes are accurate but become increasingly too long, until at the maximum setting of the variable resistor, the timer never sounds the audible warning device.

An extract from the data sheet for the capacitor is shown opposite.
Explain the likely cause of the timing problem.

Capacitance 6800 µF /± 20%

Rated voltage 16 V

Leakage current <50 µA @ 20°C

[3 marks]

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2 (e) When the switch is opened, the timer resets.
Describe what happens during this process.

[2 marks]

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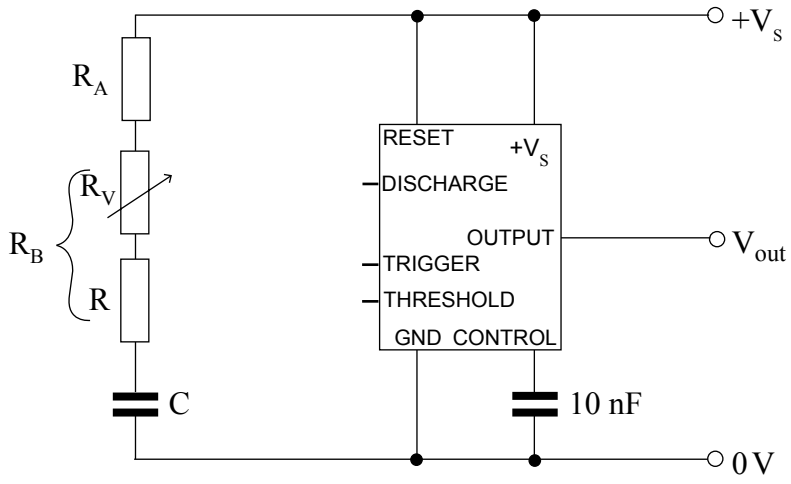
3 A project needs a subsystem which will produce a pulse output in the range 10 Hz to 200 Hz. The subsystem is to be based on a 555 astable.

3 (a) **Figure 5** shows a partially drawn 555 astable circuit diagram.
Add the **three** missing connections.

[3 marks]

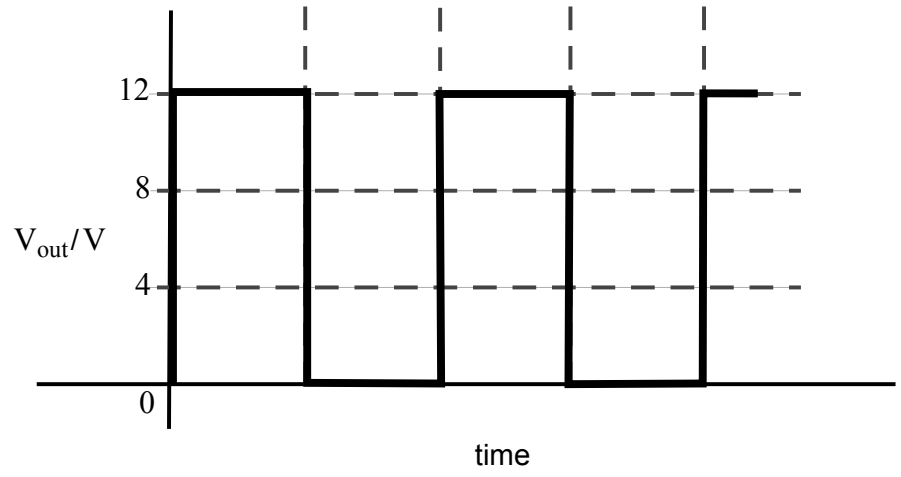
Figure 5



3 (b) **Figure 6** shows how the output voltage, V_{out}, varies with time.
Sketch onto the graph how the voltage across the capacitor varies with time.

[3 marks]

Figure 6



3 (c) If the frequency is 200 Hz, C = 100 nF and R_A = 1 kΩ, show that the value of the fixed resistor, which is part of R_B, is approximately 36 kΩ.

[3 marks]

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3 (d) Calculate a suitable value for R_V so that when set to its maximum value the frequency of the pulses is approximately 10 Hz.

[2 marks]

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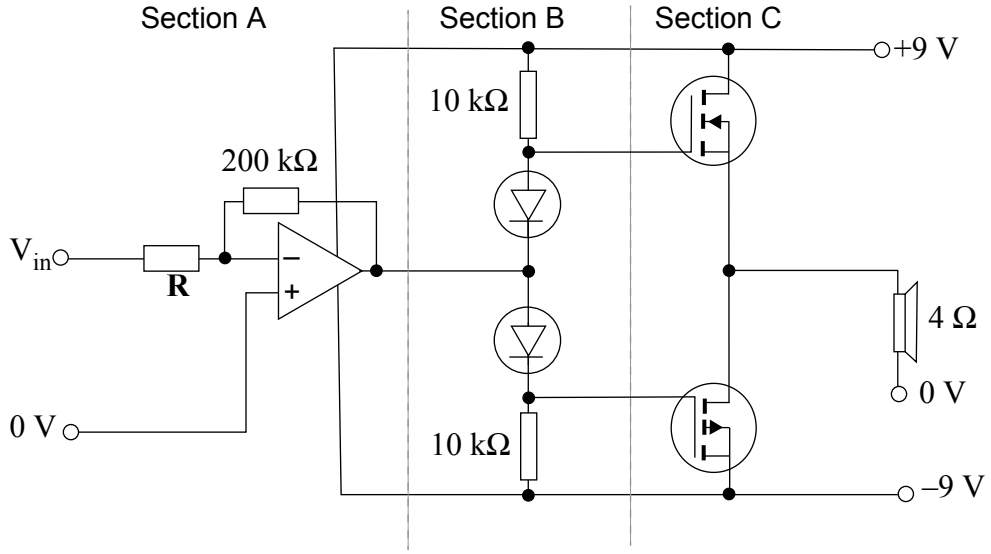
Turn over for the next question

4 **Figure 7** shows the circuit diagram for a power amplifier. The power amplifier is required to have an overall voltage gain of at least 5 and a power output of 10 W into a 4 Ω loudspeaker.

Figure 7



4 (a) (i) Put a tick in the box that best describes the function of Section B.

[1 mark]

Provides voltage gain. ☐

Biases the MOSFETs. ☐

Provides power gain. ☐

Sets the voltage gain of the amplifier. ☐

4 (a) (ii) Put a tick in the box that best describes the function of Section C.

[1 mark]

Provides voltage gain. ☐

Biases the MOSFETs. ☐

Provides power gain. ☐

Sets the voltage gain of the amplifier. ☐

4 (b) (i) Calculate a value for **R** which will give Section A a voltage gain of 5.

[2 marks]

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4 (b) (ii) Explain why the voltage gain of the **overall** circuit is less than 5.

[2 marks]

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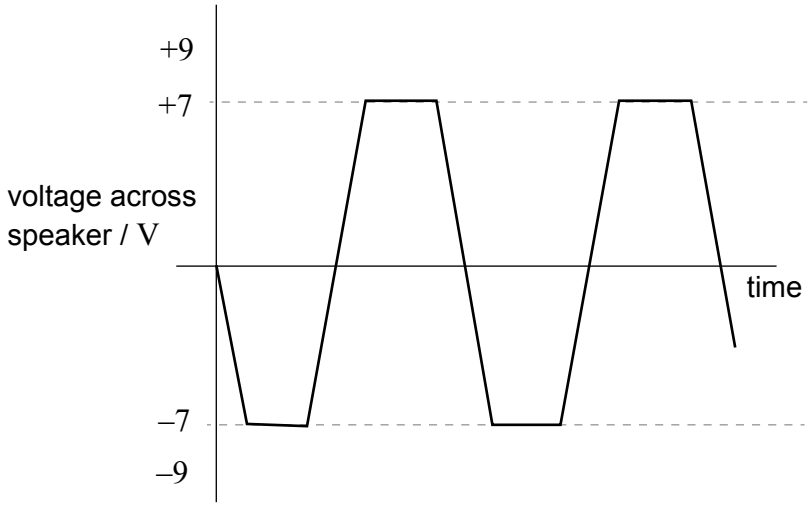
Question 4 continues on the next page

4 (c) A sine wave of amplitude $1.8\ \text{V}$ is fed into the amplifier and the voltage across the loudspeaker is shown in **Figure 8**.

Figure 8



4 (c) (i) Put a tick in the box that best explains why the voltage across the speaker does **not** reach $\pm 9\ \text{V}$.

[1 mark]

The input signal voltage to the amplifier is too small. ☐

The op-amp output does not saturate at the supply voltages. ☐

The loudspeaker has a resistance that is too large. ☐

The op-amp does not have sufficient voltage gain. ☐

4 (c) (ii) Estimate the maximum undistorted output power of the amplifier.

[3 marks]

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4 (c) (iii) Put a tick in the box that best describes how to increase the undistorted output power of the amplifier.

[1 mark]

Decrease the input signal voltage. ☐

Decrease the power supply voltage. ☐

Increase the power supply voltage. ☐

Increase the loudspeaker resistance. ☐

11

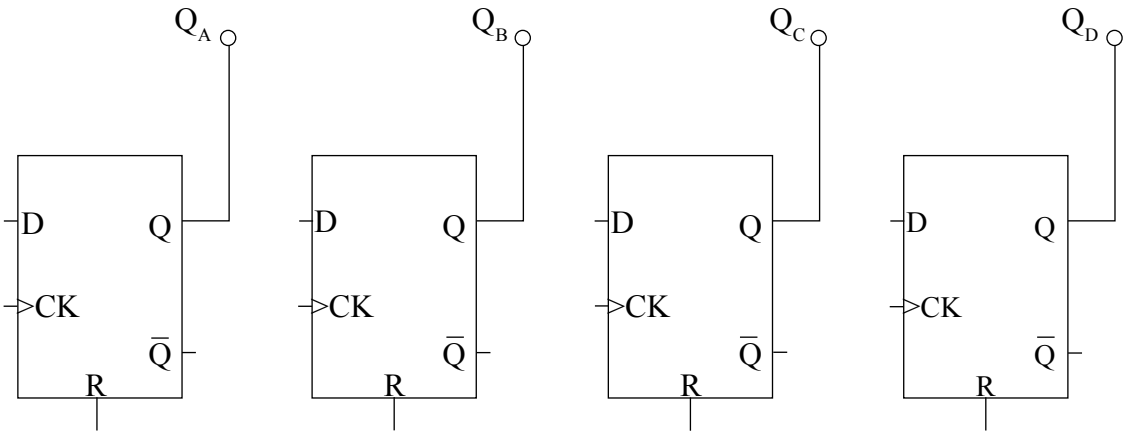
Turn over for the next question

5 An industrial process requires chemicals to be exposed to an intense light which then reduces over time to zero. A control system for the light uses a 4-bit down counter and a 4-input summing amplifier.

5 (a) Complete the circuit diagram for a 4-bit down counter in **Figure 9**.
Label the clock input.

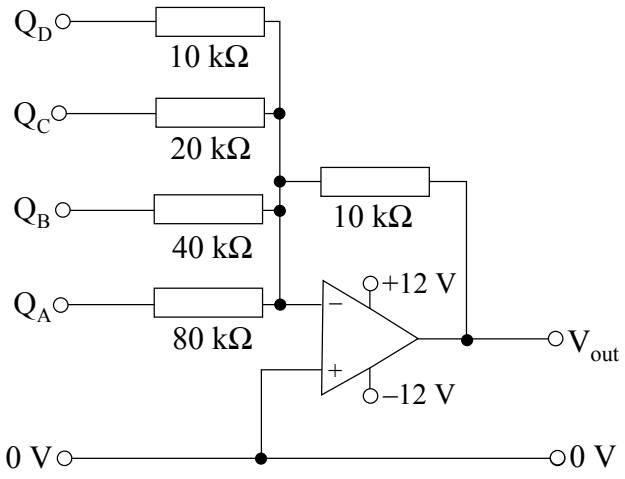
[4 marks]

Figure 9



5 (b) **Figure 10** shows the circuit diagram for the summing amplifier.

Figure 10



Assume that a logic 1 output from the counter is +5 V and a logic 0 is 0 V. Calculate the output from the summing amplifier when the counter has reached a count of 1011_2.

[3 marks]

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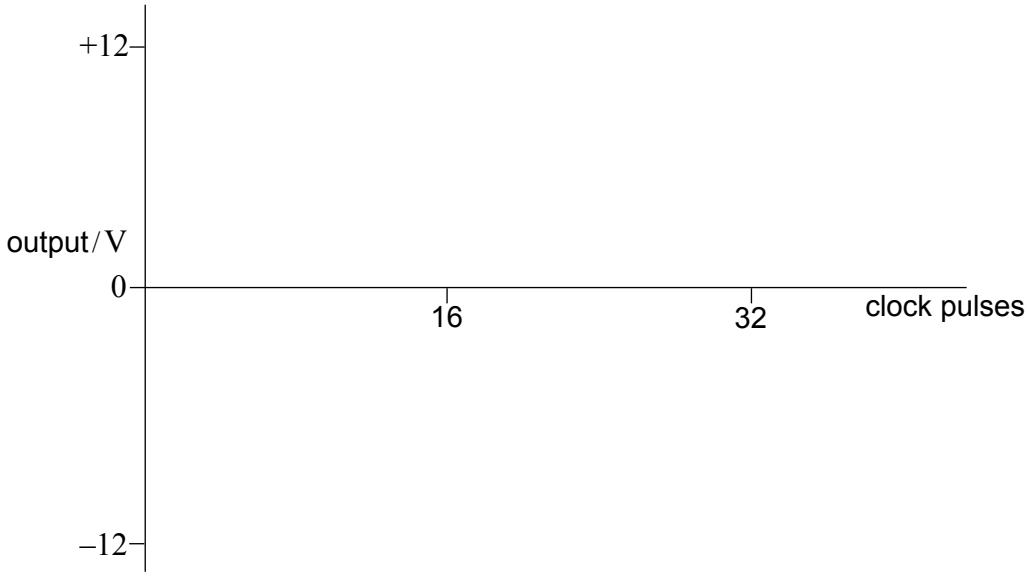
5 (c) The counter is reset to 0000.
Sketch a graph on **Figure 11** to show the output of the summing amplifier for an input of 32 clock pulses to the counter.

[4 marks]

Figure 11

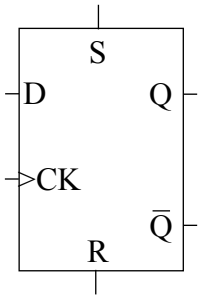


11

Turn over for the next question

6 **Figure 12** shows the symbol for a D-type flip-flop.

Figure 12



6 (a) Describe the operation of a D-type flip-flop.

[3 marks]

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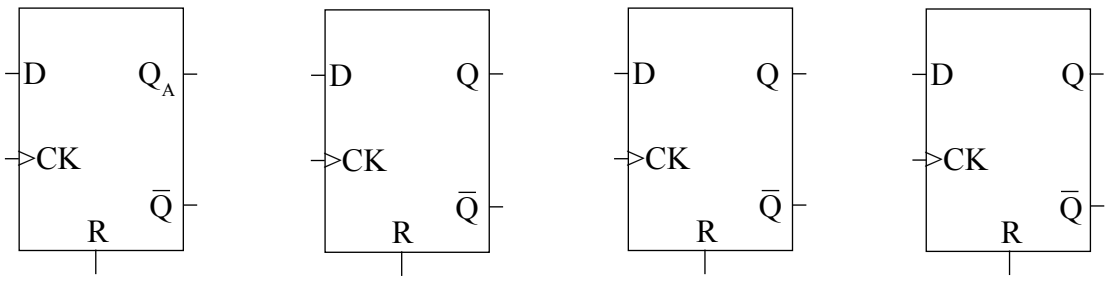
6 (b) Complete the circuit diagram for a 4-bit shift register in **Figure 13**.
Label the serial data input and the clock input.

[4 marks]

Figure 13



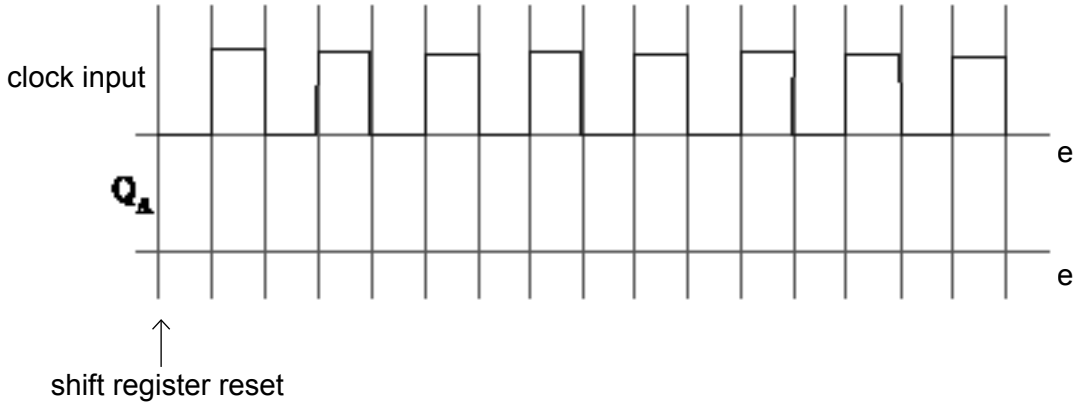
6 (c) Add logic gate(s) to **Figure 13** so that when all of the Q outputs of the shift register are logic 0, then the serial data input is a logic 1.

[3 marks]

6 (d) With the logic gate(s) added, the shift register is reset.
Show on the axes of **Figure 14** how Q_A changes for 8 clock pulses.

[2 marks]

Figure 14



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END OF QUESTIONS

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