# A-LEVEL
# ELECTRONICS

## Introductory Electronics ELEC1
## Mark scheme

2430
June 2014

Version: 1.0 Final

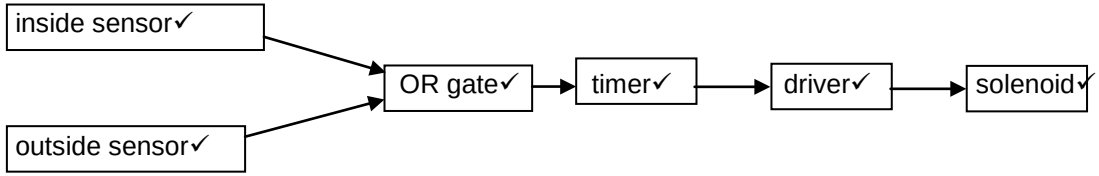
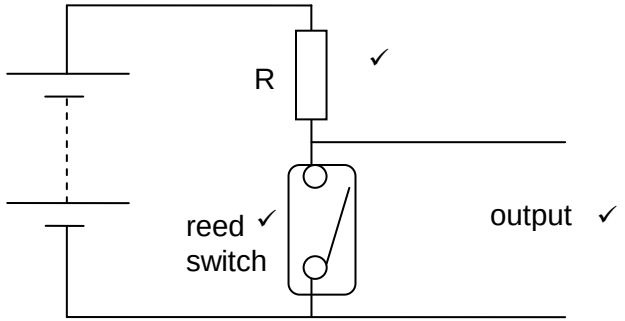
Mark schemes are prepared by the Lead Assessment Writer and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation events which all associates participate in and is the scheme which was used by them in this examination. The standardisation process ensures that the mark scheme covers the students' responses to questions and that every associate understands and applies it in the same correct way. As preparation for standardisation each associate analyses a number of students' scripts: alternative answers not already covered by the mark scheme are discussed and legislated for. If, after the standardisation process, associates encounter unusual answers which have not been raised they are required to refer these to the Lead Assessment Writer.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of students' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

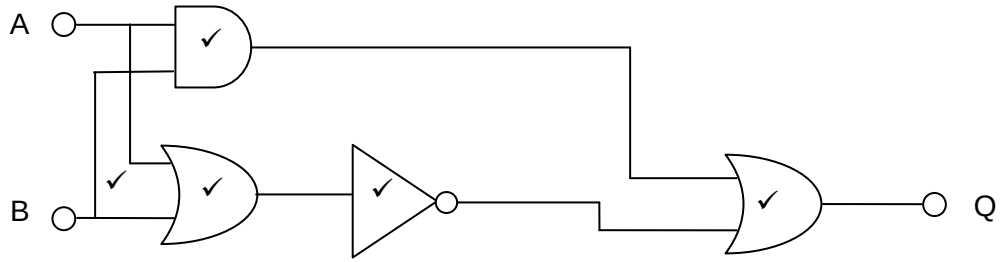
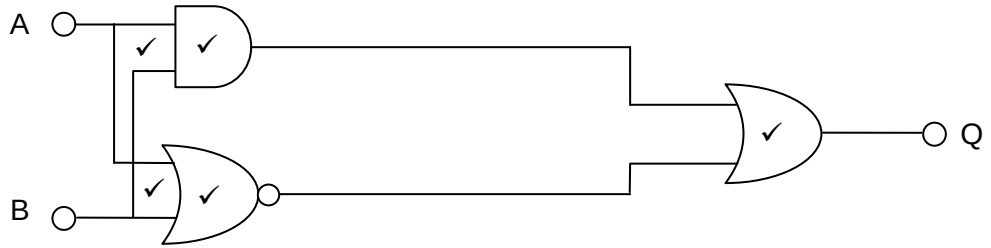
Further copies of this Mark Scheme are available from aqa.org.uk

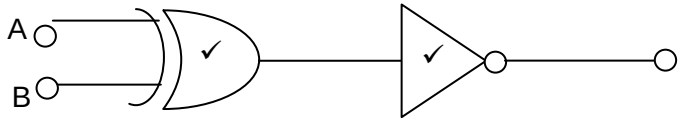
**COMPONENT NUMBER:** ELEC1

**COMPONENT NAME:** Introductory Electronics

| Question | Part | Sub part | Marking Guidance | Mark | Comments |
|---|---|---|---|---|---|
| 1 | (a) | |  (**Allow** part circuit diagram) | 6 | NOR gate acceptable, as well as OR gate. |
| 1 | (b) | |  | 3 | |
| 1 | (c) | | MOSFET or bipolar transistor✓ | 1 | |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | (a) | | | **A** | **B** | **A . B** | **A + B** | $\overline{\mathbf{A + B}}$ | **Q** | | 5 | | |
| | | | | 0 | 0 | **0** | **0** | **1** | **1** | | | | |
| | | | | 0 | 1 | **0** | **1** | **0** | **0** | | | | |
| | | | | 1 | 0 | **0** | **1** | **0** | **0** | | | | |
| | | | | 1 | 1 | **1** | **1** | **0** | **1** | | | | |
| | | | | | | ✓ | ✓ | ✓ | ✓✓ | | | | |

| | | | | | |
|---|---|---|---|---|---|
| 2 | (b) | |  | 5 | |
| | | |  | 5 | Common alternative answer. |

| | | | | | |
|---|---|---|---|---|---|
| 2 | (c) | | **Example**<br>  | 2 | **Accept** an EXNOR gate for 2 marks |

| | | | | | |
|---|---|---|---|---|---|
| 3 | (a) | (i) | power socket connections✓<br>resistor from i/p to Zener diode ✓<br>0V line complete✓<br>Zener diode (symbol & reverse bias)✓ | 4 | |
| 3 | (a) | (ii) | for a resistor, voltage drop depends on current✓<br>a zener diode breaks down at a specified voltage✓ | 2 | |
| 3 | (b) | (i) | 10.9 – 4.7 = 6.2V✓ | 1 | |
| 3 | (b) | (ii) | 90 +10 = 100mA✓ | 1 | |
| 3 | (b) | (iii) | 6.2/0.1 = 62Ω✓✓ | 2 | |
| 3 | (c) | (i) | 14.4 – 4.7 = 9.7V✓ | 1 | |
| 3 | (c) | (ii) | 9.7/62 = 156mA✓ | 1 | |
| 3 | (c) | (iii) | 9.7 x 0.156 = 1.5W✓✓ | 2 | |

| | | | | | |
|---|---|---|---|---|---|
| 4 | (a) | (i) | transistor symbol✓<br>collector✓<br>base✓<br>emitter✓ | 4 | |
| 4 | (a) | (ii) | diode✓<br>position✓ | 2 | |
| 4 | (b) | (i) | 100mA✓ | 1 | |
| 4 | (b) | (ii) | 100/40 = 2.5mA✓ | 1 | |
| 4 | (b) | (iii) | (5.2 – 0.7)✓/0.0025 = 1.8kΩ✓ | 2 | |
| 5 | (a) | | comparator✓ | 1 | |
| 5 | (b) | | inverting input✓ | 1 | |
| 5 | (c) | | appropriate formula(e) ✓<br>correct substitution ✓ | 2 | |
| 5 | (d) | (i) | Because 3.8V is lower than 4.8V ✓<br>so op-amp o/p will be low/0V✓ | 2 | |
| 5 | (d) | (ii) | 3.5m ±0.1m✓ | 1 | |

| | | | | | |
|---|---|---|---|---|---|
| 5 | (e) | | Any 3 of:<br>Op-amp has saturated✓<br>o/p > 0V ✓<br>enough to power alarm ✓<br>compare real op-amp/ideal op-amp ✓ | 3 | |

| | | | | | |
|---|---|---|---|---|---|
| 6 | (a) | | <table><tr><td>3</td><td>5</td></tr><tr><td>a, b, c, d, g</td><td>a, c, d, f, g</td></tr></table><br>(tick in third box down) ✓ | 1 | |

| | | | | | |
|---|---|---|---|---|---|
| 6 | (b) | | 0110000 ✓<br>1101101 ✓<br>0110011 ✓ | 3 | |

| | | | | | |
|---|---|---|---|---|---|
| 6 | (c) | | e = Xbar.Y.Zbar ✓ {accept Y.(X+Y) Bracket bar }<br>g = X ⊕ Y ✓ ✓ (accept Xbar.Y + X.Ybar ) | 3 | |

| | | | | | |
|---|---|---|---|---|---|
| 6 | (d) | | EX-OR ✓ | 1 | |

| | | | | | |
|---|---|---|---|---|---|
| 6 | (e) | | invert Y ✓<br>NAND gate with two inputs,any one inverted✓<br>Final inverter made from NAND gate✓ | 3 | |