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**General Certificate of Education
June 2010**

ELECTRONICS

ELEC1

Unit 1 Introductory Electronics

Mark Scheme

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1	(a)	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th> <th>B</th> <th>\bar{A}</th> <th>\bar{B}</th> <th>$A \cdot B$</th> <th>$\bar{A} \cdot \bar{B}$</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p style="text-align: center; margin-top: 10px;"> ✓ ✓ ✓ ✓ ✓ </p>	A	B	\bar{A}	\bar{B}	$A \cdot B$	$\bar{A} \cdot \bar{B}$	Q	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	5
	A	B	\bar{A}	\bar{B}	$A \cdot B$	$\bar{A} \cdot \bar{B}$	Q																															
	0	0	1	1	0	1	1																															
0	1	1	0	0	0	0																																
1	0	0	1	0	0	0																																
1	1	0	0	1	0	1																																
(b)		5																																				
(c)	EXNOR ✓	1																																				

Total Mark: 11

2	(a)		7
	(b)	(i) driver ✓	1
	(b)	(ii) comparator ✓	1
	(b)	(iii) temperature sensor ✓	1
	(c)	(i) $25 + 450 = 475\text{mA}$ ✓	1
	(c)	(ii) $12\text{V} \times 475\text{mA}$ ✓ $= 5.7\text{W}$ ✓	2

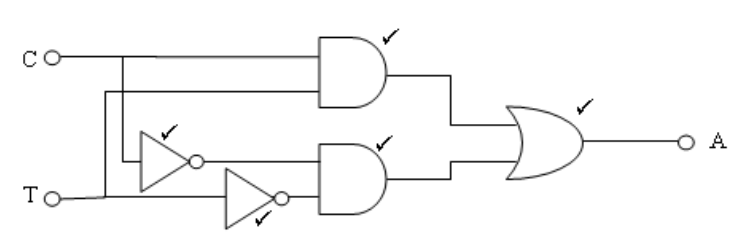
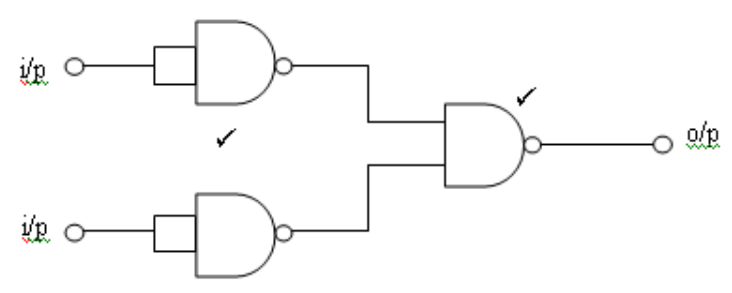
Total Mark: 13

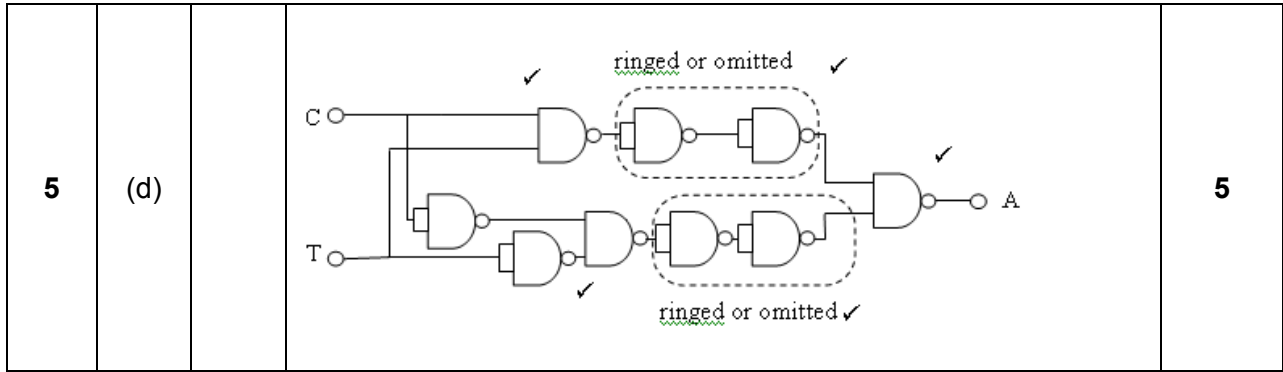
3	(a)	(i)	$9 - 1.7 = 7.3V$ ✓	1
	(a)	(ii)	$7.3 \div 0.02 = 365\Omega$ ✓	2
	(a)	(iii)	390Ω ✓	1
	(a)	(iv)	$7.3 \div 390 = 18.7 \text{ mA}$ ✓	2
	(a)	(v)	$30 + (5 \times 18.7) = 123.5 \text{ mA}$ ✓	1
	(a)	(vi)	not suitable, it will quickly become discharged✓	1
	(b)	(i)	$18.7 \div 3 = 6.2 \text{ mA}$ ✓	1
	(b)	(ii)	brightness reduces the more LEDs that are on✓ not suitable, should be the same brightness regardless✓	2

Total Mark: 11

4	(a)	MOSFET symbol✓ drain label✓ source label✓ gate label✓	4
	(b)	diode across coil✓ diode orientation✓	2
	(c)	normally closed✓ common✓ normally open✓	3

Total Mark: 9

5	(a)	$A = C.T + \overline{C.T}$ ✓	3
	(b)	 <p>The diagram shows a logic circuit with two inputs, C and T. Input C is connected to two AND gates. The top AND gate has both inputs as C. The bottom AND gate has input C and the output of a NOT gate connected to T. The outputs of these two AND gates are connected to an OR gate, which produces output A. Checkmarks are present on the AND gates and the OR gate.</p>	5
	(c)	 <p>The diagram shows a logic circuit with two inputs, i/p, connected to two AND gates. The outputs of these two AND gates are connected to a third AND gate, which produces output o/p. Checkmarks are present on the two input AND gates.</p>	2



Total Mark: 15

6	(a)		Choice of 20kΩ✓ pot div calculation✓ 8V✓	3
	(b)		upper half the value of lower✓ in range 1kΩ to 10kΩ✓ preferred values 1kΩ and 2kΩ, or 1.8kΩ and 3.6kΩ etc✓	3
	(c)	(i)	+12V or high✓	1
	(c)	(ii)	0V or low✓	1

Total Mark: 8