AQA

ASSESSMENT and
QUALIFICATIONS
ALLIANCE

General Certificate of Education

Electronics 5431/6431

ELE2 Further Electronics

Mark Scheme

*2006 examination – June series*

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation meeting attended by all examiners and is the scheme which was used by them in this examination. The standardisation meeting ensures that the mark scheme covers the candidates' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for the standardisation meeting each examiner analyses a number of candidates' scripts: alternative answers not already covered by the mark scheme are discussed at the meeting and legislated for. If, after this meeting, examiners encounter unusual answers which have not been discussed at the meeting they are required to refer these to the Principal Examiner.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of candidates' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

Unit ELE2 – Further Electronics

1 (a) (i) One input from gate 1 to output of gate 2, ✓
one input from gate 2 to output of gate 1 ✓
Pull up resistors on the two free inputs ✓

(3 marks)

(ii) Correct points labelled as outputs **Q** and **$\overline{Q}$** ✓
SET on input opposite **Q** ✓
RESET in input opposite **$\overline{Q}$** ✓

(3 marks)

(b) When the **SET** input is briefly taken to log<u>ic</u> 0 ✓
The **Q** output will become logic 1 and the **$\overline{Q}$** output will become logic 0 ✓
When the **RESET** input is now briefly taken to logic 0, **Q** will become logic
0 and the **$\overline{Q}$** will become logic 1 ✓

(3 marks)
(question total 9 marks)

2 (a) $Gv = V_{out}/V_{in} = 1.0 / 0.2 = 5$ ✓

(1 mark)

(b)

✓✓
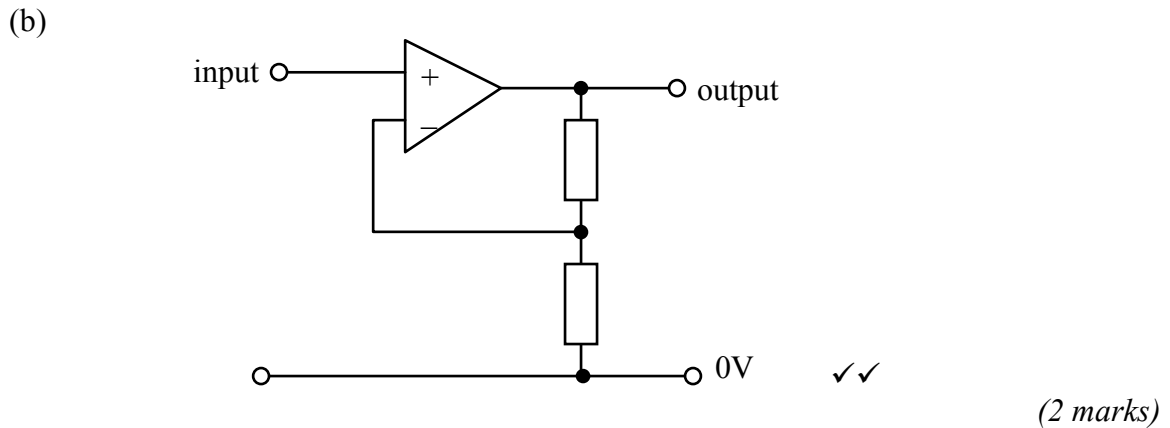
(2 marks)

(c) $Gv = 1 + R_f / R_1 \Rightarrow 5 = 1 + 240 / R_1$ ✓
$R_1 = 240 / 4 = 60k\Omega$ ✓

(2 marks)

(d) (i) Low pass filter allows low frequencies to pass and attenuates high
frequencies ✓

(1 mark)

(ii) (The frequency) at which $V_{out} / V_{in} = 0.71$ (accept 0.5) ✓
($X_c = R_f$)

(1 mark)

(iii) $f = 1 / (2 \pi R C) \Rightarrow f = 1 / 2 \pi \, 240 \, 10^3 \, 82 \, 10^{-12} = 8.087kHz$ ✓✓

(2 marks)
(question total 9 marks)

3 (a) (i) To hold the input at logic 1 ✓

(1 mark)

(ii) input must go low ✓
to less than half of supply voltage ✓

(2 marks)

(b) When input of gate 1 goes low output of gate 1 goes high ✓
This starts to charge capacitor through 1MΩ resistor and so makes
input of gate 2 high. ✓
The output of gate 2 goes low, which is fed back to gate 1 so keeping its
output high ✓
Capacitor charges through 1MΩ resistor until input voltage to gate 2 is
below half of the supply voltage ✓
The output of gate 2 goes high, making output of gate 1 low, circuit resets ✓

(4 max)

(c) $T \approx R\,C \implies 30 \approx 10^6\,C \implies C = 30\mu F$ ✓✓

(2 marks)
(question total 9 marks)

4 (a) Push-pull. The signal is split into positive and negative going signals ✓
These are amplified separately and then recombined to recreate the amplified
signal ✓

(2 marks)

(b) (i) Power supply voltage is not large enough ✓
(Gain too large)
(Saturation or clipping)

(1 mark)

(ii) Maximum output voltage is 15V ✓
Max power $= V_P^2 / 2xR = 15^2 / 2x4 = 225 / 8 = 28W$ ✓

(2 marks)

(iii) Power $= I^2 R \implies 28 = I^2.4 \implies I = \sqrt{7} = 2.65A$ ✓

(1 marks)

(c) rms voltage $= 18 / 1.414 = 12.73V$ ✓
Power supplied $= V_{rms} \times I_{rms} = 12.73 \times 2.65 = 33.7W$ ✓

(2 marks)

(d) Energy dissipated as heat in the output transistors ✓

(1 marks)
(question total 9 marks)

5   (a)   source follower ✓

(1 mark)

(b)   The output voltage of the op-amp will be 0V and there will be a voltage
drop of 0.7V across the diode, so making the gate of the MOSFET -0.7V

(1 mark)

(c)   2V ✓
The characteristic shows that a drain to source current only passes when
Vgs is greater than 2V ✓

(2 marks)

(d)   (i)   positive parts of the output signal pass to the gate via the diode,
causing the capacitor to charge and so increasing the gate voltage ✓

(1 mark)

(ii)   increases the brightness of the lamp ✓

(1 mark)

(iii)   decreases the resistance of the LDR ✓

(1 mark)

(iv)   decreases the voltage gain of the amplifier ✓

(1 mark)

(e)   automatic volume control ✓

(1 mark)
(question total 9 marks)

6   (a)   (i)   1 ✓

(1 mark)

(ii)   1MΩ ✓

(1 mark)

(b)   (i)   -1 ✓

(1 mark)

(ii)   amplitude x 10 ✓
inverted ✓

(2 marks)

(c)   (i)   inverting input terminal of op-amp ✓

(1 mark)

(ii)   +0.7V ✓
-0.7V ✓

(2 marks)

(iii)   volume (level) control ✓

(1 mark)
(question total 9 marks)

7   (a)   (i)   When an input to a NAND gate is 0, the output is 1 so the astable circuit cannot toggle. ✓
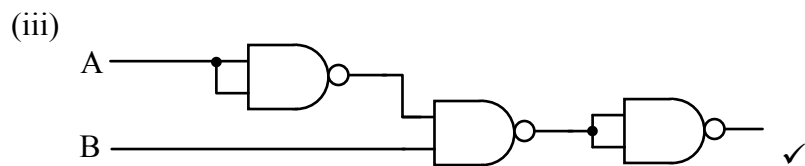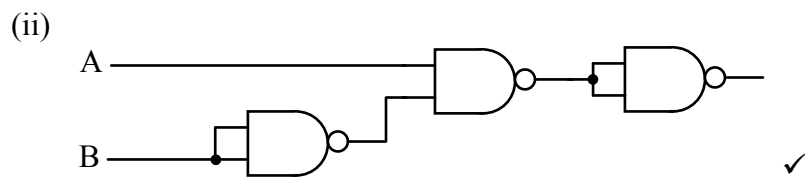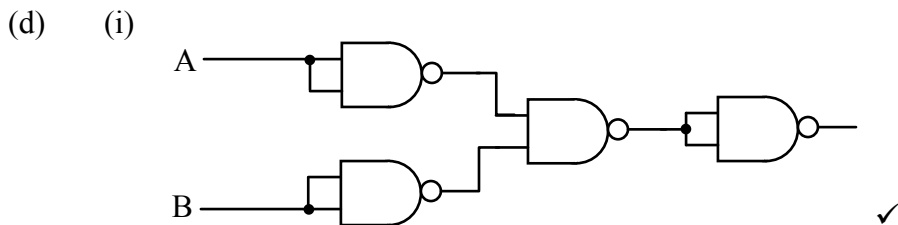
(1 mark)

          (ii)   When the input to first NAND gate goes high ✓
Output of first NAND gate goes low, output of astable goes high ✓
Capacitor discharges and charges in opposite direction ✓
Until voltage at input to first NAND gate $<+V_S/2$ ✓
Output of astable switches state ✓
Capacitor charges in opposite direction ✓
Process repeats as long as switch pressed ✓

(5 max)

          (iii) $f = 1 / 2\,R\,C\ = 1 / 2\ 10^6\ 10^{-7}$ ✓
$=> f = 5Hz$ ✓

(2 marks)

   (b)   (i)   D-type ff symbol ✓
D to **Q̄** connection to make toggle ✓
Clock to previous **Q** connection for up-counter ✓

(3 marks)

          (ii)   Rising edge of the clock pulse ✓

(1 mark)

   (c)   (i) $\mathbf{\underline{A} \bullet \overline{B}}$ ✓
        (ii) $\mathbf{A \bullet B}$ ✓
        (iii) $\mathbf{A \bullet B}$ ✓

(3 marks)

   (d)   (i)

          (ii)

          (iii)

(3 marks)
(question total 18 marks)