



General Certificate of Education

Electronics 5431/6431

(ELE4) Electronic Control Systems

Mark Scheme

2005 examination – June series

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation meeting attended by all examiners and is the scheme which was used by them in this examination. The standardisation meeting ensures that the mark scheme covers the candidates' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for the standardisation meeting each examiner analyses a number of candidates' scripts: alternative answers not already covered by the mark scheme are discussed at the meeting and legislated for. If, after this meeting, examiners encounter unusual answers which have not been discussed at the meeting they are required to refer these to the Principal Examiner.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of candidates' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

ELE4 – Electronic Control Systems

- 1**
- (a) To keep all parts of the system synchronised ✓ (1 mark)
- (b) Data has to travel to and from the processor along the data bus ✓ (1 mark)
- (c) (i) processor ✓
(ii) ROM ✓
(iii) RAM ✓
(iv) processor ✓ (4 marks)
- (d) Data bus uses 8 bits i.e. 1 byte at a time
Address bus has 2^{12} different addresses \Rightarrow 4096 bytes can be addressed ✓ (1 mark)
- (e) Memory mapping I/O ports places I/O ports in memory locations ✓
so the amount of locations available for memory is reduced ✓ (2 marks)
- Total 9 marks**

- 2**
- (a) ANN - many simple processors, PC - few complex processors ✓
ANN - no single memory location, PCs - single memory location ✓
(any other valid answer) (2 marks)
- (b) PC better at direct calculations - eg accounts ✓
ANN better at predictive problems - eg weather forecasting ✓
(any other valid answer) (2 marks)
- (c) $T \approx R \times C = 10^4 \times 10^{-8} = 0.1\text{ms}$ ✓ ✓ (2 marks)
- (d) (i) Nothing (- input to monostable $> V_S/2$) ✓
(ii) Nothing (-input to monostable $= V_S/2$) ✓
(iii) Monostable triggers (- input to monostable $< V_S/2$) ✓ (3 marks)
- Total 9 marks**

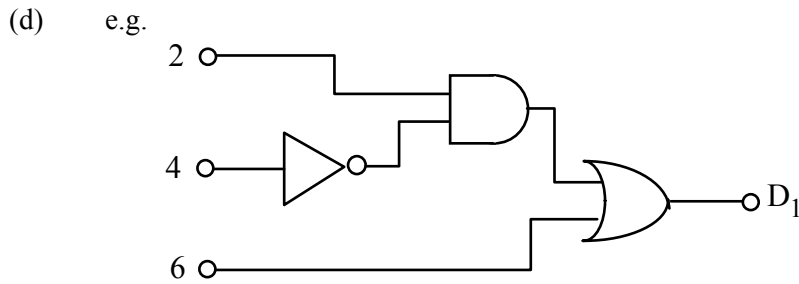
3 (a) Flash ADC - very fast ✓
Flash ADC - expensive ✓ (2 marks)

(b) (i) 5/8V (0.625V) ✓
(ii) comparator ✓
(iii) $2^{12}-1 = 4095$ ✓ (3 marks)

(c)

D ₂	D ₁	D ₀	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

✓ ✓
(2 marks)



✓ ✓

(2 marks)

Total 9 marks

4 (a) (i) label ✓
(ii) **&H379** ✓
(iii) masks all bits other than D₆ and D₇ ✓
(iv) sensors connected to D₆ and D₇ ✓ (4 marks)

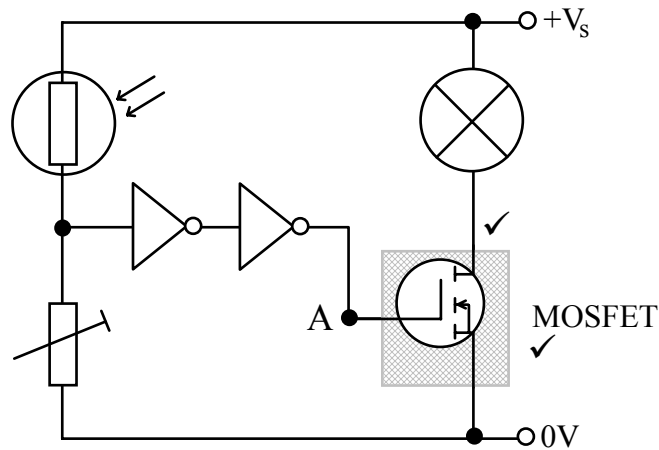
(b) (i) polling - continuously checks the state of the port ✓
(ii) Interrupt - when data is ready an interrupt is generated and the computer leaves its current task and reads the data from the port ✓ ✓ (3 marks)

- (c) (i) A value for **T%** ✓
 (ii) generates a delay ✓ (and allows the program to end when the Esc key is pressed) (2 marks)

Total 9 marks

- 5** (a) An open loop system does not have any feedback ✓ so it is unable to monitor its own output unlike a closed system which can ✓ (2 marks)

- (b) (i)



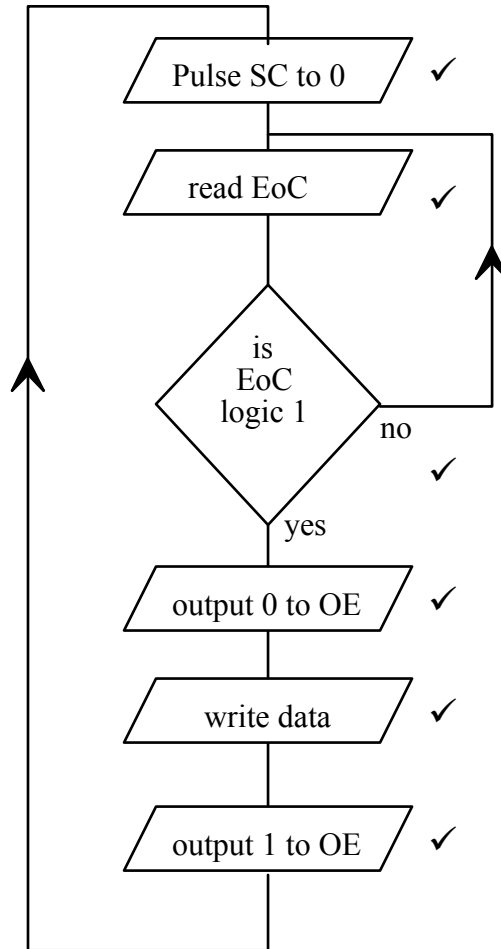
- (ii) When the LDR is illuminated it has a low resistance ✓ so input to first NOT gate is a logic 1 => point A is logic 1 ✓ (4 marks)

- (c) (i) positive feedback ✓
 (ii) light from the lamp falls onto the LDR which keeps its resistance low ✓ this keeps point A at logic 1 and the lamp lit ✓ (3 marks)

Total 9 marks

- 6** (a) (i) A tristate buffer has three possible output states, logic 1,0 and disconnected (high impedance) ✓
 (ii) To prevent bus contentions between the microprocessor system and ADC (to enable the microprocessor to select when the data from the ADC is applied to the data bus) ✓
 (iii) When the ADC is writing to the data bus ✓ (3 marks)

(b) e.g.



(4 marks)

(c) e.g. speed of computer; the program; the number of bits etc ✓✓

(2 marks)

Total 9 marks

7

(a) voltage across R = 12 – 1.5 = 10.5V ✓
 maximum current is 20mA => R = 10.5 / 0.02 = 525Ω ✓
 => suitable R = 560Ω ✓

(3 marks)

(b) (i) The inverting input of the op-amp is a virtual earth ✓
 The 6μA passes through the 1MΩ resistor
 => the output will be 6V ✓

(ii) Current in the dark is 0.1μA.
 Output voltage is $10^{-7} \times 10^6 = 0.1V$ ✓

(3 marks)

(c) eliminates multiple (false) triggering ✓
 by having two distinct switching levels ✓

(2 marks)

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- (d) (i) output low => 10k Ω resistor in parallel with 10k Ω resistor of voltage divider
combined resistance = 5k Ω ✓
lower voltage = $(12 \times 5) / (20 + 5) = 2.4\text{V}$ ✓
- (ii) output high => 100k Ω resistor in parallel with 20k Ω resistor of voltage divider => combined resistance = 16.67k Ω ✓
upper voltage = $(12 \times 10) / (26.67) = 4.5\text{V}$ ✓ (4 marks)
- (e) (i) A stepper motor has a set of stator coils and a permanent magnet armature.
When adjacent coils are sequentially energised the armature turns through a defined angle ✓ ✓
- (ii) Answer should include:
discussion of control electronics needed for conventional motor (photo sensor, pulse generator reference signal, phase comparator, error amplifier, buffer) ✓
discussion of control electronics needed for stepper motor (pulse generator, counter, decoder, buffer per coil) ✓
less electronics needed for stepper motor ✓
speed of rotation more constant with stepper motor because the speed is only dependent upon the speed the pulses are applied to the coils (so long as load is not too great or the pulses too fast) ✓
etc (6 marks)

Total 18 marks