Version : 1.0

ASSESSMENT and QUALIFICATIONS ALLIANCE

General Certificate of Education

Electronics 5431/6431

(ELE2) Further Electronics

Mark Scheme

2005 examination – June series

Mark schemes are prepared by the Principal Examiner and considered, together with the relevant questions, by a panel of subject teachers. This mark scheme includes any amendments made at the standardisation meeting attended by all examiners and is the scheme which was used by them in this examination. The standardisation meeting ensures that the mark scheme covers the candidates' responses to questions and that every examiner understands and applies it in the same correct way. As preparation for the standardisation meeting each examiner analyses a number of candidates' scripts: alternative answers not already covered by the mark scheme are discussed at the meeting and legislated for. If, after this meeting, examiners encounter unusual answers which have not been discussed at the meeting they are required to refer these to the Principal Examiner.

It must be stressed that a mark scheme is a working document, in many cases further developed and expanded on the basis of candidates' reactions to a particular paper. Assumptions about future mark schemes on the basis of one year's document should be avoided; whilst the guiding principles of assessment remain constant, details will change, depending on the content of a particular examination paper.

ELE2 – Further Electronics

1 (a) A negative going signal that decreases below 2.5V ✓ (1 mark)

(b) Negative going pulse makes output of gate 1 go high, ✓
This makes input of gate 2 high, and output low, ✓
Capacitor charges through resistor, ✓
Until voltage at input of gate 2 is below half of the supply voltage, ✓
Output of gate 2 goes high ✓
Monostable resets ✓ (4 marks)

(c) $T \approx R\,C \Rightarrow T \approx 10^{-8}\ 10^{4} = 0.1\text{ms}$ ✓ ✓ (2 marks)

(d) Maximum frequency is when the monostable retriggers immediately it has reset ✓
Since period of monostable is 0.1ms => max frequency is ≈ 10kHz ✓ (2 marks)

Total 9 marks

2 (a) (i) Low pass filter - a filter that allows low frequencies to pass through with little attenuation, while high frequencies are attenuated ✓ (1 mark)

(ii) break point frequency - the frequency at which the output voltage is equal to 0.71 of its max value. ✓ (1 mark)

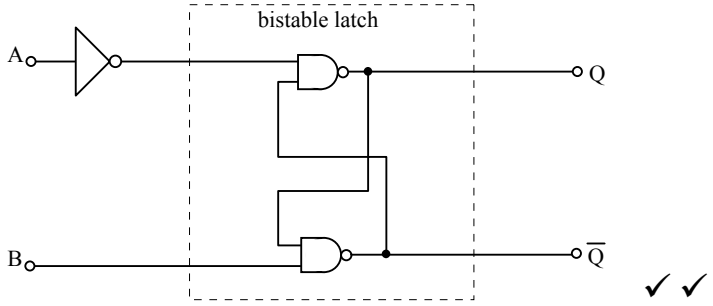
(b) (i) (non-inverting amplifier. At low frequencies ignore C)
$\Rightarrow G_V = 1 + 390/10 = 40$ ✓ ✓ (2 marks)

(ii) At the cut off frequency $X_c = R_f = 390\text{k}\Omega$ ✓
$C = 1/2\pi fR = 1/2\ \pi\ 2500\ 39000 = 163\text{pF}$ ✓ ✓ (3 marks)

(c) 10^6 = frequency x voltage gain => voltage gain = 10^6 / frequency. ✓
voltage gain = 10^6 / 2.5 x 10^3 = 400 ✓ (2 marks)

Total 9 marks

3 (a)



✓ ✓

(2 marks)

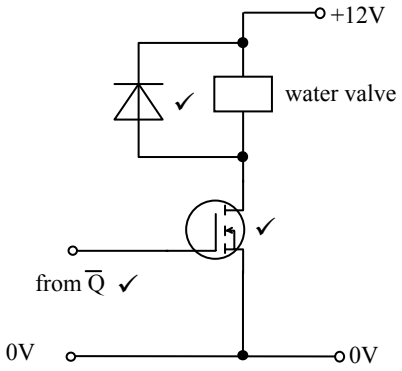
(b) (i) 0 ✓

(ii) 0 ✓

(iii) 1 ✓

(iv) 1 ✓ (4 marks)

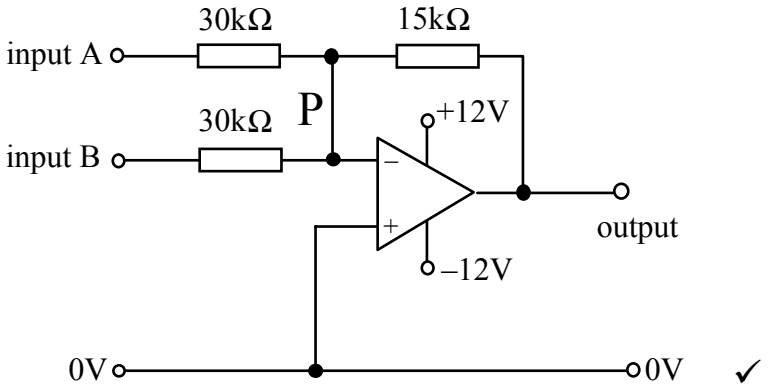
(c)



(3 marks)

Total 9 marks

4 (a)



✓

(1 mark)

(b) $V_{out} = -R_f\{V_a/R_a + V_b/R_b\}$ ✓

$V_{out} = -15\{2/30 + 0/30\} = -1V$ ✓ (2 marks)

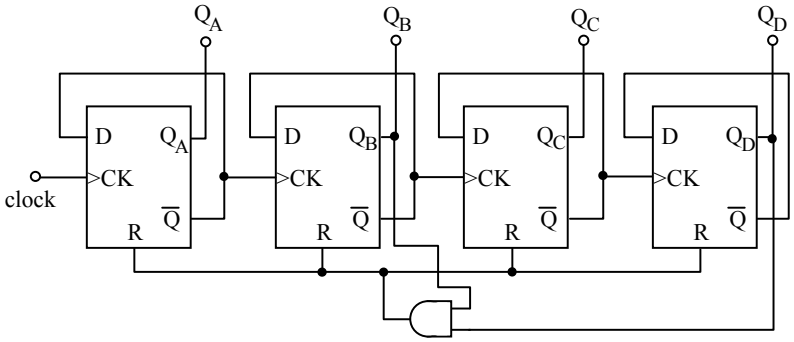
(c) $V_{out} = -15\{2/30 + 2/30\} = -2V$ ✓ (1 mark)

(d) (i) The magnitude of the signal is not altered ✓
The signal is inverted ✓

(ii) Signal 2 is inverted which makes the audio in phase with signal 1 ✓
The noise on signal 2 is inverted compared to that on signal 1 ✓
When added together the noise signals cancel ✓ (5 marks)

Total 9 marks

5 (a)



D to $\overline{\mathbf{Q}}$ ✓
All Resets joined together ✓
$\overline{\mathbf{Q}}$ to following **CK** ✓
Output of AND gate to Reset ✓
B and D to inputs of AND gate ✓ (4 marks)

(b) Binary values for when the heater is on:
0010, 0101, 0111, 1000 ✓
The counter outputs ANDed together to form the binary values which are then ORed ✓ (2 marks)

(c)

$$\overline{\mathbf{D}}.\overline{\mathbf{C}}.\mathbf{B}.\overline{\mathbf{A}} + \overline{\mathbf{D}}.\mathbf{C}.\overline{\mathbf{B}}.\mathbf{A} + \overline{\mathbf{D}}.\mathbf{C}.\mathbf{B}.\mathbf{A} + \mathbf{D}.\overline{\mathbf{C}}.\overline{\mathbf{B}}.\overline{\mathbf{A}}$$
$$= \overline{\mathbf{D}}.\overline{\mathbf{C}}.\mathbf{B}.\overline{\mathbf{A}} + \mathbf{D}.\overline{\mathbf{C}}.\overline{\mathbf{B}}.\overline{\mathbf{A}} + \overline{\mathbf{D}}.\mathbf{C}.\mathbf{A}.\left(\overline{\mathbf{B}} + \mathbf{B}\right) \quad ✓✓✓$$
$$= \overline{\mathbf{C}}.\overline{\mathbf{A}}\left(\overline{\mathbf{D}}.\mathbf{B} + \mathbf{D}.\overline{\mathbf{B}}\right) + \overline{\mathbf{D}}.\mathbf{C}.\mathbf{A}$$
$$= \overline{\mathbf{C}}.\overline{\mathbf{A}}\left(\mathbf{D} \oplus \mathbf{B}\right) + \overline{\mathbf{D}}.\mathbf{C}.\mathbf{A}$$

(3 marks)

Total 9 marks

6 (a) On the rising edge of each clock pulse ✓
The data from a D-type flip-flop is stored in the next D-type flip-flop ✓
This data transfer occurs all of the way along the shift register ✓
New data applied to the input of the first flip-flop is taken into the shift register ✓ (4 marks)

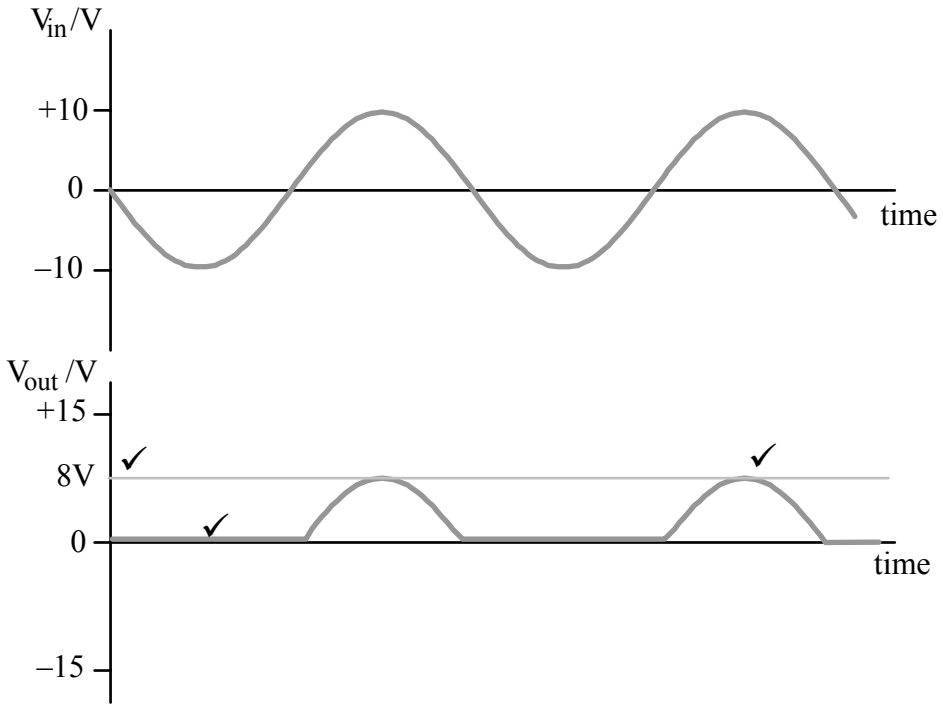
(b) Removes multiple pulses due to contact bounce ✓ (1 mark)

(c) The D input of the first flip-flop goes to logic 1 ✓
The clock input goes to logic 1 and the data is shifted along the shift register ✓ (2 marks)

(d) The output of the five input AND gate must be logic 1 =>10001 ✓
The Q output of the last flip-flop must also be logic 1
=> smallest binary number is 100011 ✓ (2 marks)

Total 9 marks

7 (a)



(3 marks)

(b) (i) Push Pull ✓

(ii) Inverting amplifier with G_V of –4.7 and source follower with G_V of ≈ 1 ✓
=> Overall G_V = –4.7 x 1 = –4.7 ✓ (3 marks)

(c) (i) Cross-over distortion ✓

(ii) When the input voltage is smaller than that needed ✓ to make either MOSFET conduct ✓

(iii) 0 Amps – V_{gs} is only 1.36V => MOSFETs are not conducting ✓ (4 marks)

(d) There needs to be approx 2V across each 1kΩ resistor ✓
So there must be 13V across (X) (Y) ✓
=> 2mA through 1kΩ resistor => (X) (Y) = 6.5kΩ ✓ (3 marks)

(e) Include MOSFETs into feedback loop ✓
by disconnecting 47kΩ resistor from op-amp output and connecting to MOSFET output ✓ (2 marks)

(f) $P = V_S^2/2R$ ✓
=> $P = 15^2/2 \times 4 = 28W$ ✓
If take into account V_{gs} of MOSFETs ie $P = 13^2/2 \times 4 = 21W$ ✓ (3 marks)

Total 18 marks