GCE 2004
June Series

ASSESSMENT and QUALIFICATIONS ALLIANCE

Mark Scheme

Electronics
5431/6431 (ELE2)

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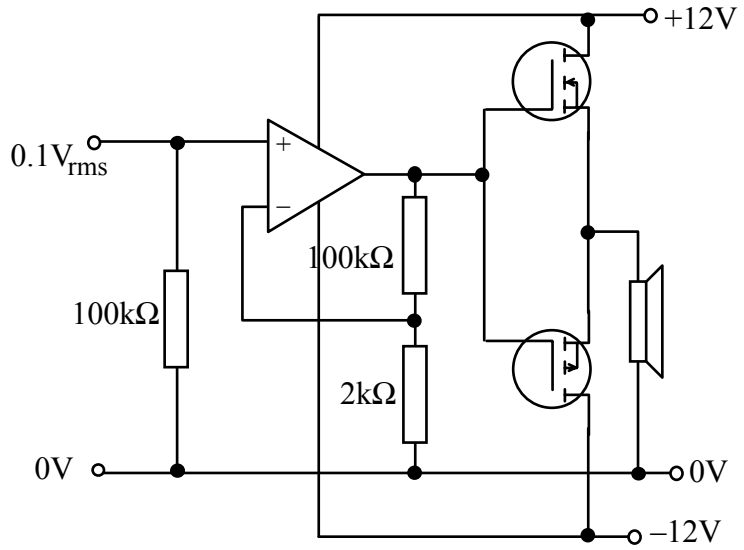
ELE2 – Further Electronics

1

(a) Non-inverting amp => $G_V = 51$ ✓
=> $V_{out} = 0.1 \times 51 = 5.1V$ ✓ (2 marks)

(b)



n and p-channel MOSFETs in correct orientation and position ✓
gates connected together and to op-amp output ✓
speaker from joined sources to 0V ✓ (3 marks)

(c) (i) Cross over distortion ✓ (1 mark)

(ii) The MOSFETs are very non-linear at small values of V_{gs} ✓
so as signal crosses 0V, it is not amplified as much by the MOSFETs ✓
(or other suitable explanation) (2 marks)

(iii) Bias the MOSFETs into conduction (or equivalent) ✓ (1 mark)
(apply negative feedback to MOSFETs)

(Total 9)

2

(a) (i) Non-inverting amplifier ✓
$G_V = 1 + R_f / R_l = 1 + 100/10$ ✓
$G_V = 11$ ✓ (3 marks)

(ii) $G_V = 1$ ✓ (1 mark)

(iii) 200kΩ ✓ (1 mark)

(b) non-inverting input of op-amp to 0V ✓
resistor from each input circuit to inverting input of op-amp ✓ (2 marks)

(c) Gv of summing amp = 110/11 = 10 ✓
=> input resistors of summing amp = 470/10 = 47kΩ ✓ (2 marks)

(Total 9)

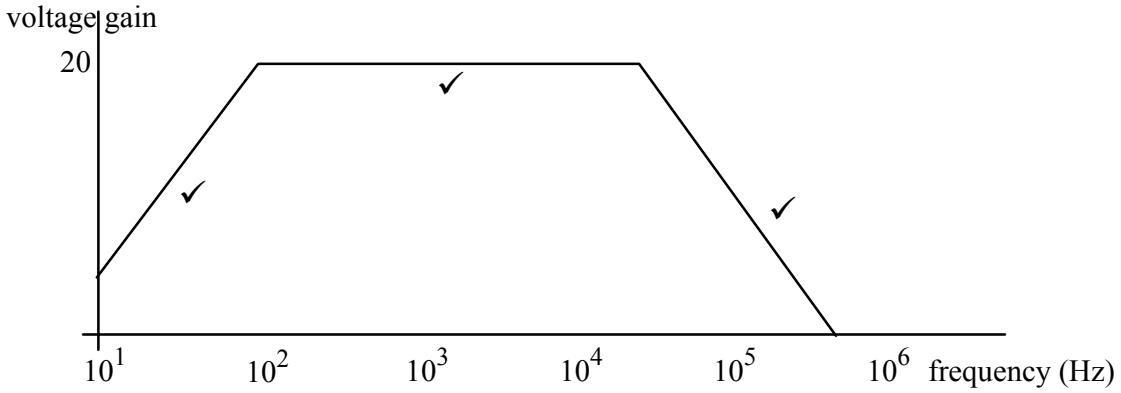
3

(a) (i) Inverting amp => $G_V = -R_f / R_1$ ✓
=> Gv = –300/15 = –20 ✓ (2 marks)

(ii) Output signal is inverted ✓
Amplitude is increased ✓ (2 marks)

(b) $X_C = 1/2\pi fC = 1/6.28 \times 32 \times 0.33 \times 10^{-6}$ ✓
$X_C = 15.1k\Omega$ ✓ (2 marks)

(c) At low frequency, half gain at 32Hz.
At high frequency, gain decreases above 25kHz ($5x10^5/20$)



(3 marks)

(Total 9)

4

(a) (i) op-amp compares output voltage with zener voltage ✓
op-amp adjusts gate voltage to MOSFET to compensate for any difference ✓ (2 marks)

(ii) MOSFET function - source follower (or equivalent) ✓
(voltage follower, power amplifier, current amplifier, buffer amplifier) (1 mark)

(b) (i) 3A ✓ (1 mark)

(ii) 14 - 5 = 9V ✓ (1 mark)

(iii) Max power = V x I = 9 x 3 = 27(W) ✓ (1 mark)

(c) Matt black, metal, large surface area ✓ ✓ ✓ (3 marks)

(Total 9)

5

(a) (i) Negative going pulse makes output of gate A go high, ✓
This makes input of gate B high, and output low, ✓
Capacitor charges through resistor, ✓
Until voltage at input of gate B is below half of the supply voltage, ✓
Output of gate B goes high, ✓
Monostable resets. ✓ (max 5)

(ii) $T \approx R.C \Rightarrow C = T/R = 0.01/500000$ ✓
C = 20nF ✓ (2 marks)

(b) $T \approx 2.R.C = 2 \times 10^{-7} \times 10^{4} = 2ms$ ✓ ✓ (2 marks)

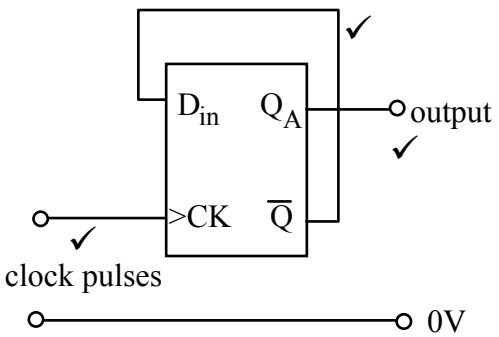
(Total 9)

6

(a) Shift register ✓ (1 mark)

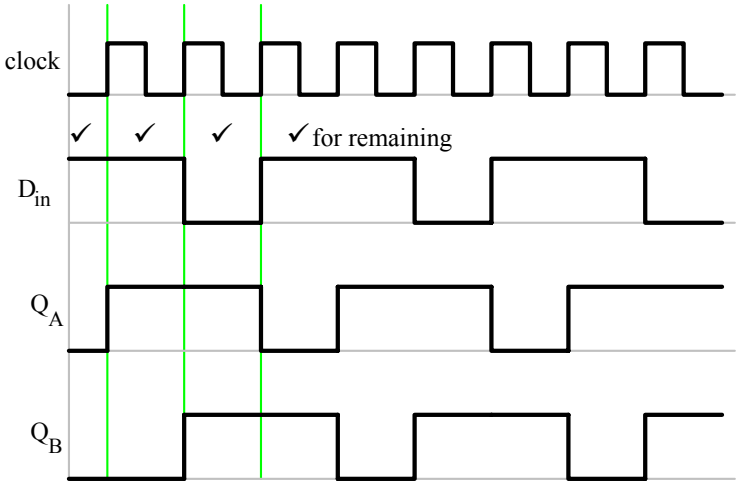
(b) NOT gate or inverter ✓ (1 mark)

(c)



(3 marks)

(d)



(4 marks)

(Total 9)

7

(a) **D** to $\overline{\mathbf{Q}}$ ✓
All Resets joined together ✓
$\overline{\mathbf{Q}}$ to following **CK** ✓
Output of **AND** gate to Reset ✓
C and D to inputs of **AND** gate ✓ (5 marks)

(b)

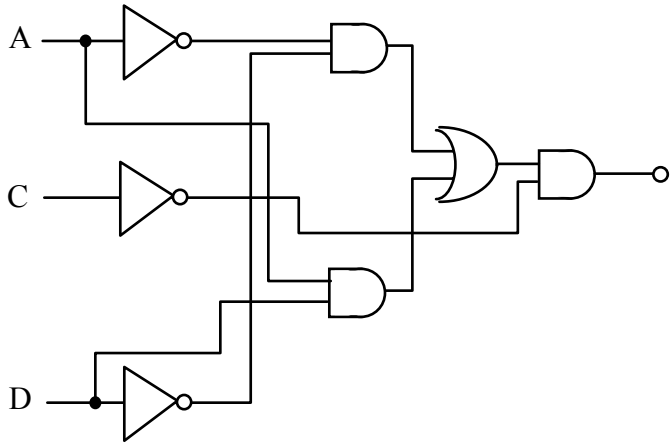
Hours	**D**	**C**	**B**	**A**
first	0	0	0	0
third	0	0	1	0
tenth	1	0	0	1
last	1	0	1	1

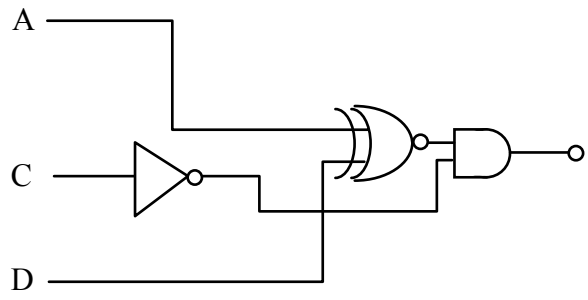
✓ ✓ ✓ ✓ (-1 per error) (4 marks)

(c) $\mathbf{H = \overline{D}.\overline{C}.\overline{B}.\overline{A} + \overline{D}.\overline{C}.B.\overline{A} + D.\overline{C}.\overline{B}.A + D.\overline{C}.B.A}$ ✓ ✓ (-1 per error) (2 marks)

(d) Simplification leading to
$\mathbf{H = \overline{C}.(\overline{D}.\overline{A} + D.A)}$ ✓ ✓ ✓ ✓ (4 marks)

(e) Examples:





✓ ✓ ✓

(3 marks)

(Total 18)

(Paper Total 72)