ASSESSMENT and QUALIFICATIONS ALLIANCE

Mark scheme June 2002

GCE

Electronics

Unit ELE2

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Further Electronics

1) (a) $T \approx RC$

$T \approx 10^6 \times 10^{-4}$ ✓ $= 100s$ ✓ (2)

(b) When the switch is opened, the input to gate X goes low ✓
The output of X goes high ✓
Capacitor charges and so makes the input to Y high ✓
This makes the output of Y low which keeps the input to X low, so sustaining the timing period ✓
The capacitor charges until voltage at input of Y $<+V_S/2$ ✓
Output of Y goes high ✓
If magnetic door switch is closed the monostable resets ✓ (max 5)

(c) (i) NAND gate Z functions as a NOT gate ✓
(1)

(ii) The MOSFET functions as a Buffer ✓
(1)
(9)

2) (a) Bandwidth is the range of frequencies over which the power output is greater than half of the maximum power output. OR
Bandwidth is the range of frequencies over which the voltage output is greater than 70% of the maximum voltage output. ✓ ✓
(2)

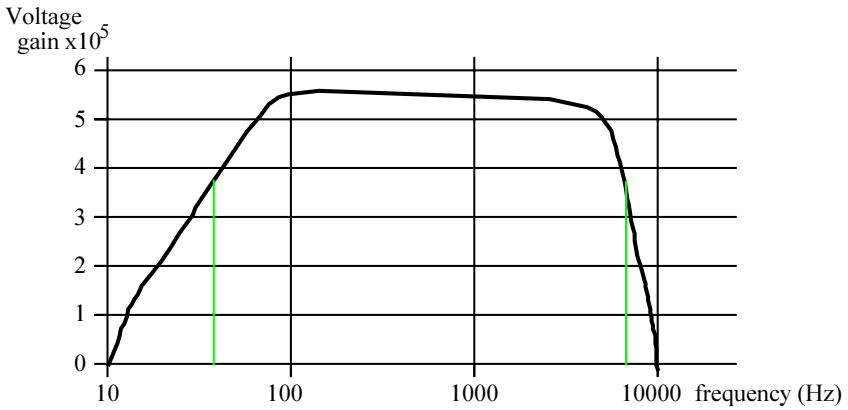
(b) $G_V = 2.5 / 5 \times 10^{-6} = 500000$ ✓
(1)

(c) (i) $G_V = 10^6 / 3000 = 333$ ✓
(1)

(ii) No. $= \log(5\times10^5) / \log(333) = 2.26$
$\Rightarrow$ No. $= 3$ ✓ ✓
(2)

(d) Current through $R_1 = 5 / 10^6 = 5\mu V$ ✓
$\Rightarrow R_2 = 1(\Omega)$ ✓
(2)

(e)



30 - 50Hz to 6 -7kHz ✓ ✓ (2)
(10)

3) (a) (i) Any point directly connected to the inverting input of the op-amp ✓

(1)

(ii) Summing amplifier ✓

(1)

(iii) 300kΩ ✓

(1)

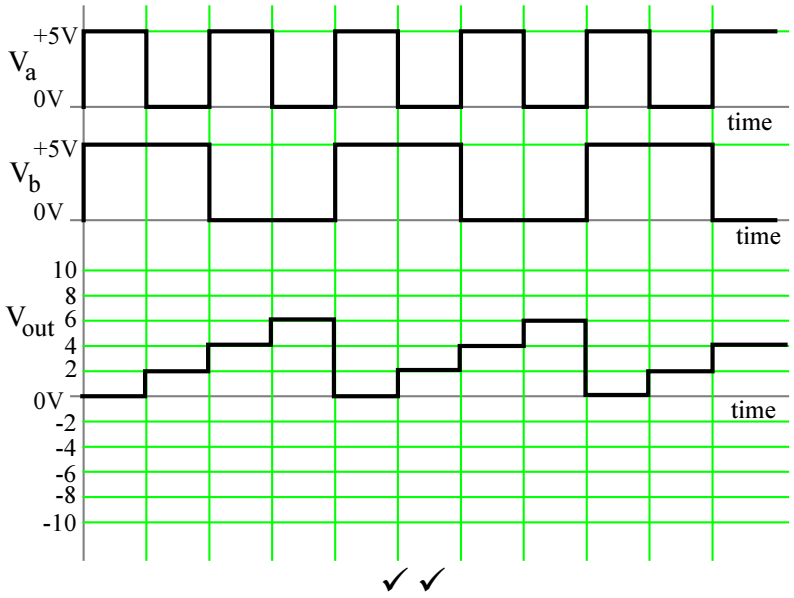
(b) $$V_{out} = -R_f\left\{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right\} = -120\left\{\frac{0}{300}+\frac{0}{150}+\frac{-12}{240}\right\} = +6V$$ ✓ ✓

(2)

(c) $$V_{out} = -R_f\left\{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right\} = -120\left\{\frac{0}{300}+\frac{5}{150}+\frac{-12}{240}\right\} = +2V$$ ✓ ✓

(2)

(d)



✓ ✓

(2)

(9)

4) (a) **D** to $\overline{\mathbf{Q}}$ ✓

Input to **CK**, other **CK** inputs from $\overline{\mathbf{Q}}$ ✓

All three **Q** outputs to the AND gate ✓

Output of AND gate to all **R** inputs joined together ✓

(4)

(b) Any direct division by two gives a mark to space ratio of 1:1. Dividing by seven and then two divides by 14, but with a 1:1 mark to space ratio output. ✓ ✓

Dividing by 14 directly would lead to a uneven mark to space ratio (of 3:4) ✓

(max 2)

(c) (i) The period of a 2MHz signal is 0.5 s ✓

(1)

(ii) The derived signal has a smaller period than the reference signal and so is therefore at a higher frequency. ✓ ✓

(2)

(d) On the rising edge of the clock pulse (reference signal) the state of D is transferred to the Q output ✓

This occurs when the derived signal is high, so the output of Q will be logic 1 ✓ (2)

(11)

5) (a) 7, E ✓ ✓

(2)

(b) For G to be illuminated, each possible state of the D, C, B, and A inputs for which Green is illuminated must be logic 1. ✓
This is achieved by **ANDing** them together ✓
and then **ORing** together each of these separate states ✓

(3)

(c) Any valid simplification leading to the answer
eg examination of the expression shows that the state of A is irrelevant.

$$\Rightarrow G = \overline{D} \cdot \overline{C} \cdot \overline{B} + \overline{D} \cdot \overline{C} \cdot B + \overline{D} \cdot C \cdot \overline{B}$$
$$\Rightarrow G = \overline{D} \cdot \overline{C} + \overline{D} \cdot C \cdot \overline{B} = \overline{D}\left(\overline{C} + C \cdot \overline{B}\right)$$
$$\Rightarrow G = \overline{D} \cdot \overline{B \cdot C}$$ ✓ ✓ ✓

(3)
(8)

6) (a) (i) On the rising edge of each clock pulse ✓
The data from a D-type flip-flop is stored in the next D-type flip-flop ✓
This data transfer occurs all of the way along the shift register ✓
Data from the output of the last flip-flop is lost ✓
New data applied to the input of the first flip-flop is taken into the shift register ✓

(max 3)

(ii) Can be used to transfer serial data to parallel and vice versa OR a delay ✓

(1)

(b)

Q_A	Q_B	Q_C	Q_D	D input of first flip-flop
0	0	0	0	1
1	0	0	0	1
1	1	0	0	1
1	1	1	0	0
0	**1**	**1**	**1**	**1**
1	0	1	1	1
1	1	0	1	0
0	1	1	0	0
0	0	1	1	1
1	0	0	1	0
0	1	0	0	1
1	**0**	**1**	**0**	**0**
0	1	0	1	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	1

✓ ✓ ✓

(3)
(7)

7) (a) (i) Reactance of C_3, calculation, answer **79.6(Ω)** ✓ ✓

(2)

(ii) 2000μF or greater up to 10mF ✓
Reactance should be less than or equal to the resistance of speaker at low frequencies ✓

(2)

(b) (i) Voltage gain of MOSFET source follower is ≈<1 ✓

(1)

(ii) Assume reactance of capacitor C_2 is negligable ✓
Recognise non-inverting amplifier ✓
Answer +11 ✓

(3)

(iii) Half of supply voltage = 6.6V ✓
G_V = 6.6 / 0.2 = 33 ✓

(2)

(iv) Decrease 47kΩ (to 14kΩ) ✓
(OR increase R_f (to 1.41MΩ)

(1)

(c) (i) Connect ammeter in series with amplifier with no signal input ✓
Expect a current greater than 20mA (but less than 100mA) ✓

(2)

(ii) Disconnect 470kΩ feedback resistor from output of op-amp and connect to junction of the MOSFET sources ✓ ✓

(2)

(d) Made of metal to aid good conduction of heat, ✓
Large surface area to aid convection and radiation ✓
Painted black to aid radiation ✓
Good thermal contact with MOSFET ✓

(max 3)
(18)